TRANSLINEAR CURRENT MODE CIRCUITS IN SUBHTRESHOLD MOS

TRANSLINEAR CIRCUITS IN SUBTHRESHOLD MOS

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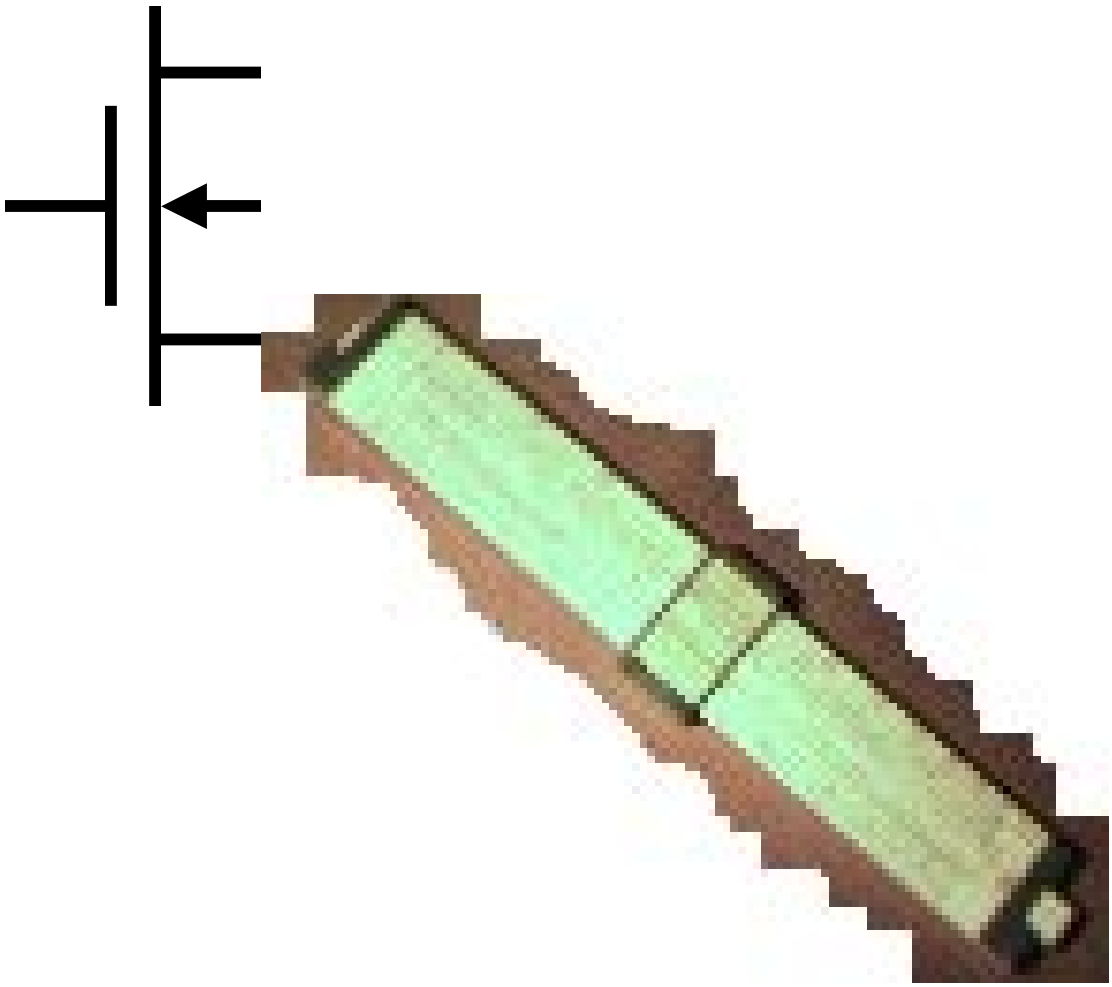
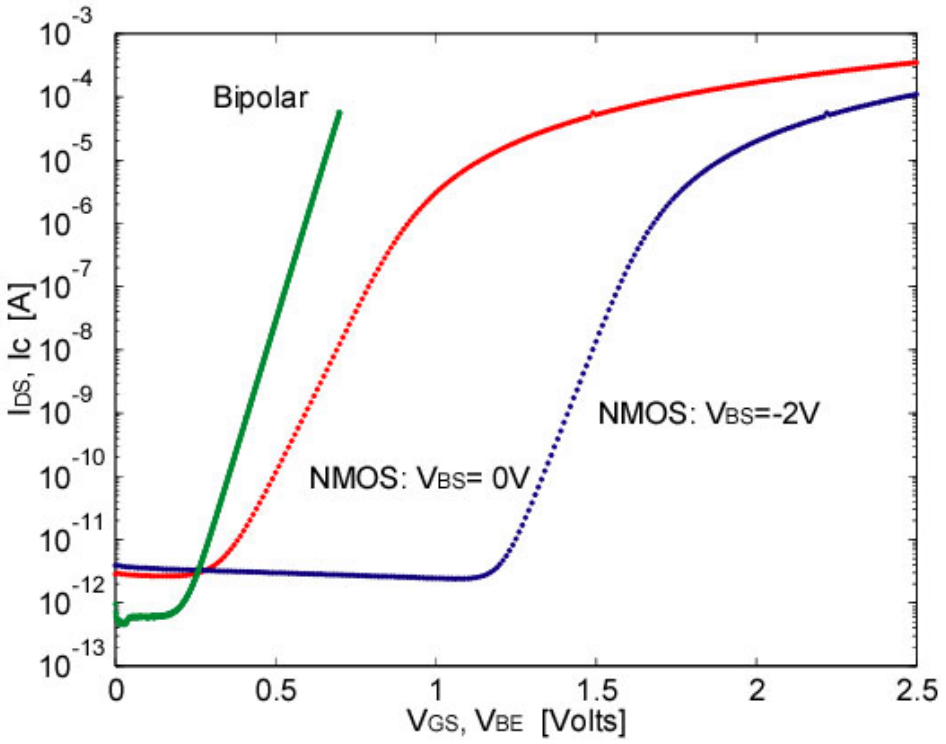


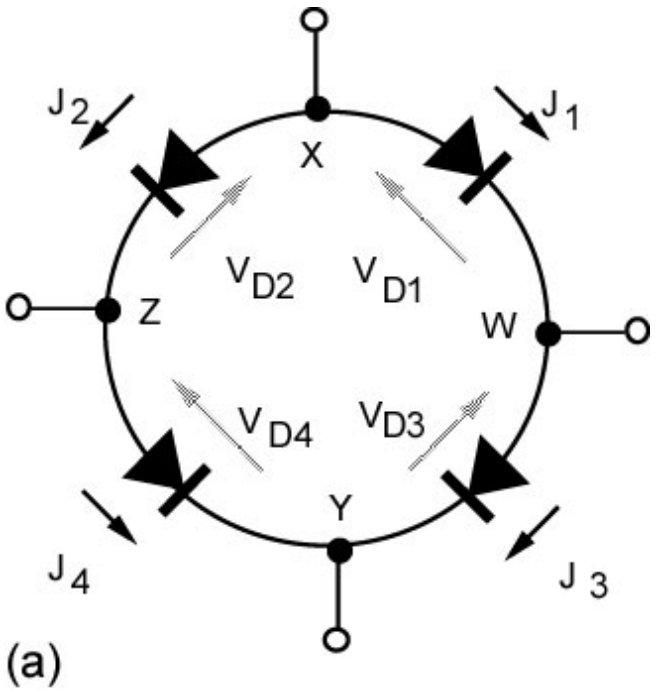
TRANSLINEAR ELEMENTS

- A translinear element is a physical device whose transconductance and current are linearly related i.e. the current is exponentially dependent on the controlling voltage
- Two terminal: pn junctions (diodes)
- Three terminal: the controlling voltage must exhibit true diode behavior.
  - Bipolar junction transistors: YES
  - MOS transistors in subthreshold: YES ….BUT ….



TRANSLINEAR PRINCIPLE

“ In a closed loop containing an equal number of oppositely connected Tranlinear elements, the product of the current densities in the clockwise (CW) direction is equal to the product for elements in the counter-clockwise (CCW) direction.”



Conservation of energy or (KVL)

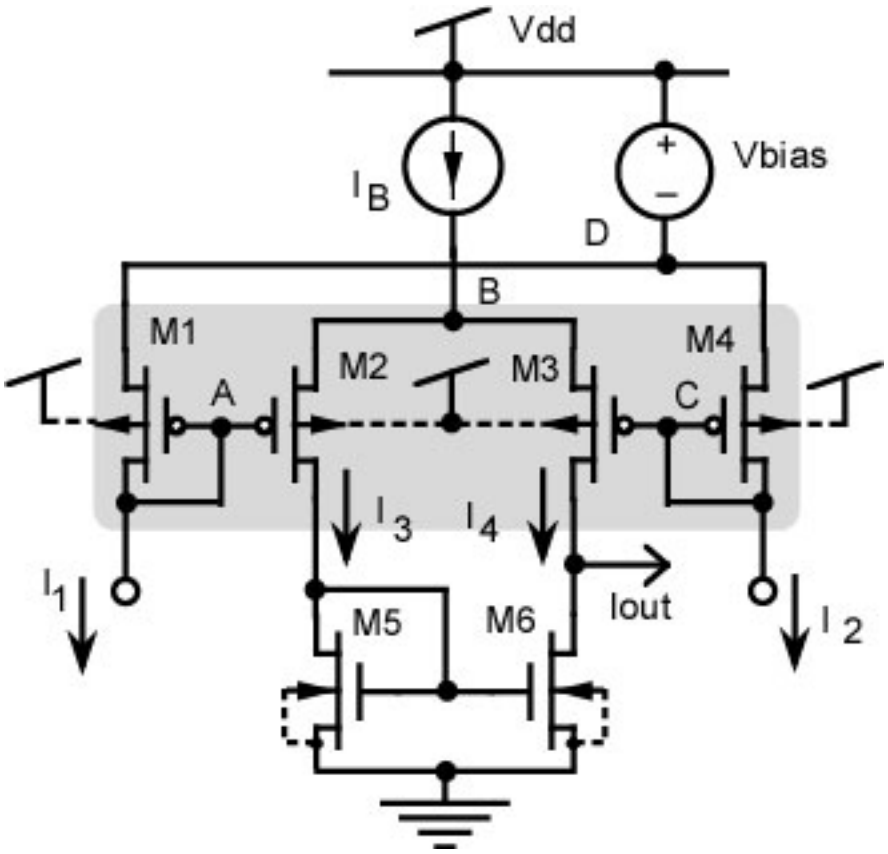
$$\sum_{i=1}^{i=N/2} V_{D(2i-1)} - \sum_{i=1}^{i=N/2} V_{D(2i)} = 0$$

Turns into this in the special case of loops with diode-like elements

$$\frac{\prod_{CCW} J}{\prod_{CW} J} = 1$$

Barrie Gilbert, Translinear circuits: a proposed classification, *Electronics Letters,* vol. 11, no. 1, pp. 14-16, 1975

MOS GILBERT GAIN CELL



V_{bias} must be such that I_B statys in saturation i.e. V_{dd}-V_B > 4 V_t

Loop: A-B-C-D-A $$I_1 I_4 = I_3 I_2 \rightarrow \frac{I_3}{I_1} = \frac{I_4}{I_2}$$

From algebra: $$\frac{I_3 - I_4}{I_1 - I_2} = \frac{I_3 + I_4}{I_1 + I_2}$$

Rearranging terms

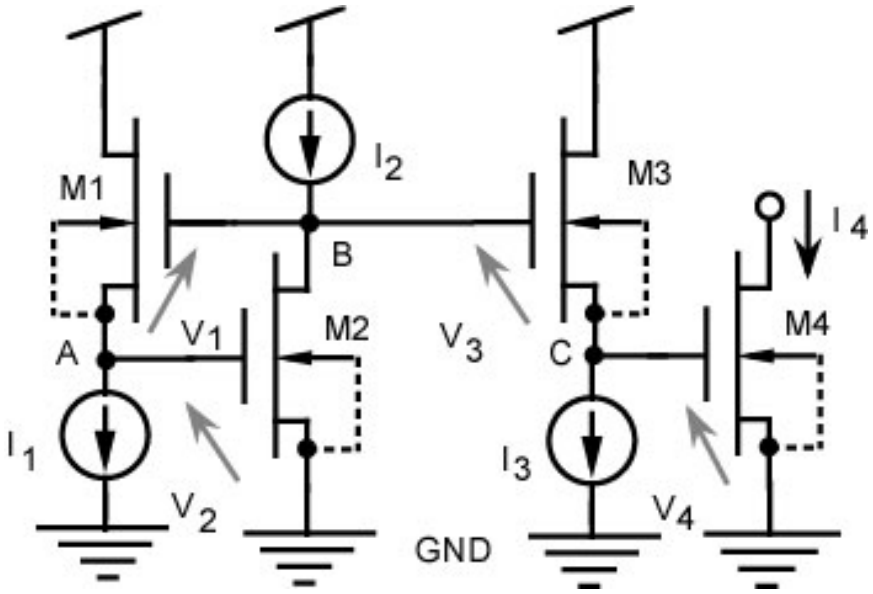
$$I_{out} = I_B \left(\frac{I_1 - I_2}{I_1 + I_2} \right)$$

Where

$$I_B \equiv I_3 + I_4$$

$$I_{OUT} \equiv I_3 - I_4$$

1Q LOG-ANTILOG MOS MULTIPLIER



All transistors have source connected to local substrate - well devices- and therefore

$$V_{SB} = 0$$

$$V_1 + V_2 - V_3 - V_4 = 0$$

$$\frac{V_t}{\kappa}\left(\ln\left(\frac{I_1}{S I_0}\right) + \ln\left(\frac{I_2}{S I_0}\right) - \ln\left(\frac{I_3}{S I_0}\right) - \ln\left(\frac{I_4}{S I_0}\right)\right) = 0$$

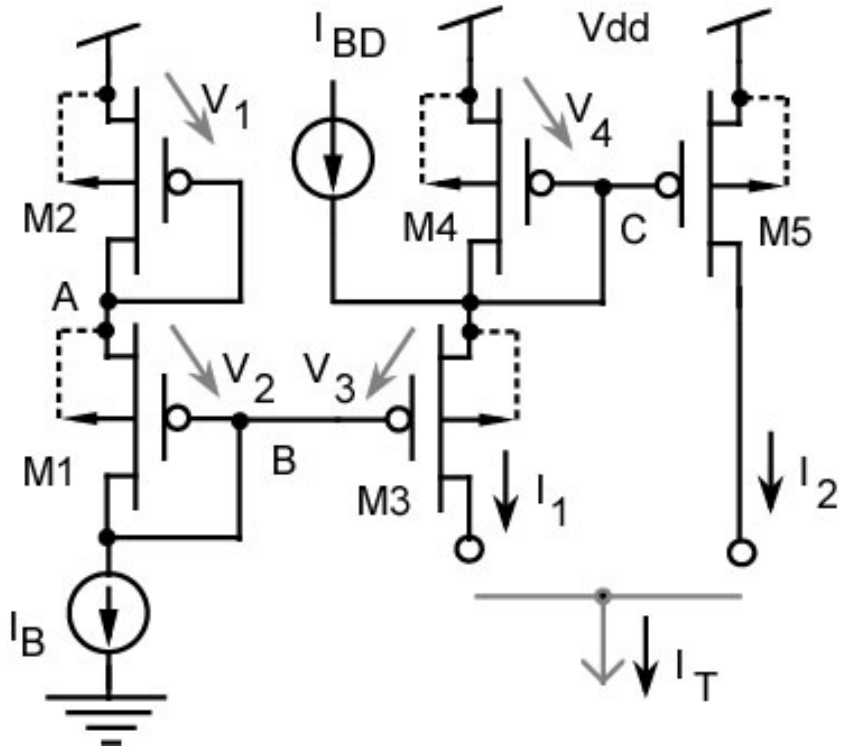
$$\ln\left(\frac{I_1 I_2}{S I_0}\right) = \ln\left(\frac{I_3 I_4}{S I_0}\right)$$

$$I_4 = \frac{I_1\ I_2}{I_3}$$

$$I_1\ I_2 = I_3\ I_4$$

Or we can derive the above by inspection using the translinear principle

ABSOLUTE VALUE CIRCUIT



$$V_{SB} = 0$$

Loop: Vdd-A-B-C-Vdd $\quad I_B = I_1 I_{DS4} = I_1 (I_1 - I_{BD})$

Loop: Vdd-C-Vdd $\quad I_2 = I_1 - I_{BD}$

Solving for I_1 and I_2

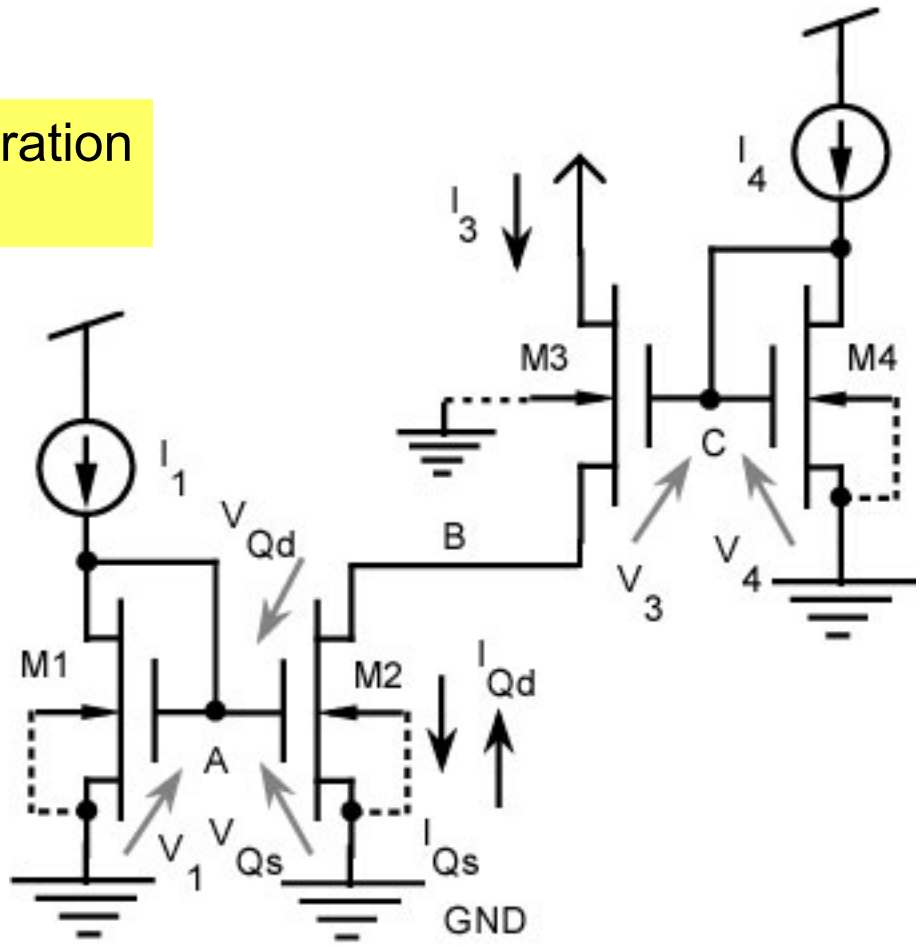
$$I_1 = \frac{1}{2}\left(I_{BD} + \sqrt{4I_B^2 + I_{BD}^2}\right) \qquad I_{BD} > 0$$

$$I_2 = \frac{1}{2}\left(-I_{BD} + \sqrt{4I_B^2 + I_{BD}^2}\right) \qquad I_{BD} < 0$$

$$I_T \equiv I_1 + I_2 \cong |I_{BD}| \qquad I_{BD} >> I_B$$

1Q CURRENT MULTIPLIER/DIVIDER

M1, M3, M4: Saturation
M2: Ohmic



$$I_3 = \frac{I_1 I_4}{I_1 + I_4}$$

Loop1; GND-A-GND $I_1 = I_{Q_s}$

Loop2; GND-A-B-C-GND $I_1 I_3 = I_4 I_{Q_d}$

Current in M3 and M2: $I_3 = I_{DS3} = I_{DS2} = I_{Q_s} - I_{Q_d}$

Solving the above we get I_3 as a function of I_4 and I_1

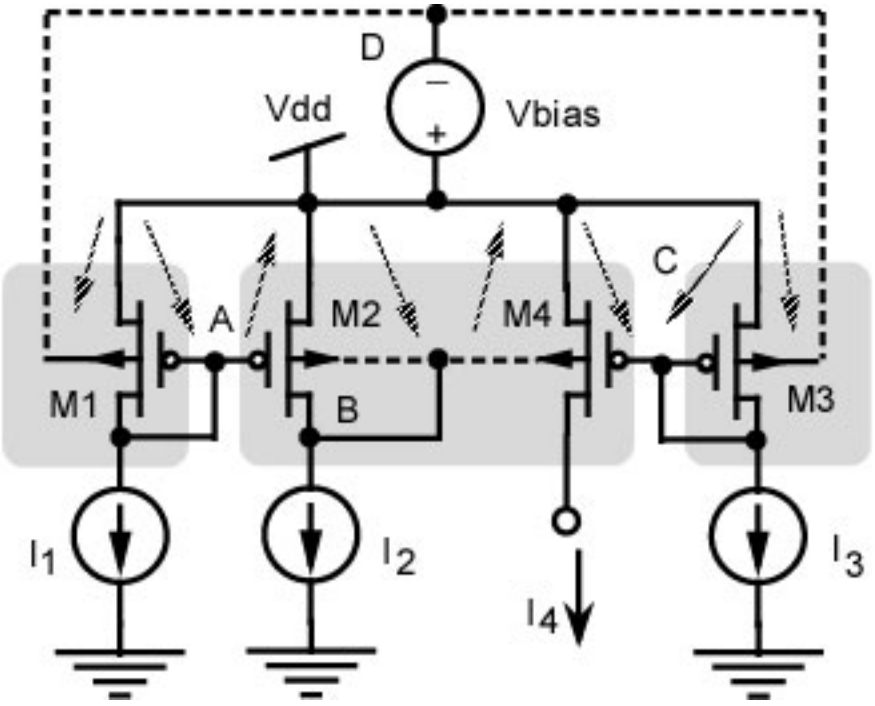
ψ Psi-currents

$$\left.\begin{array}{l} \iota_G \\ \iota_B \end{array}\right\}$$ Dimensioneless currents

$$I_D \equiv S I_0 \, \iota_G^{\kappa} \, \iota_B^{(1-\kappa)}$$

Psi currents are hypothetical currents in the device if the gate and backgate could control the current without the capacitive potential divider i.e. have access to the surface potential ψ directly.

1Q MOS Backgate Multiplier



From loops:
Vdd-A-Vdd
Vdd-C-Vdd
Vdd-B-Vdd
Vdd-D-Vdd

$$\iota_{G1} = \iota_{G2}$$

$$\iota_{G4} = \iota_{G3}$$

$$\iota_{B2} = \iota_{B4}$$

$$\iota_{B3} = \iota_{B1}$$

From psi-current definitions:

$$I_1 = I_{DS1} = SI_{n0}\, \iota_{G1}^{\kappa_1}\, \iota_{B1}^{(1-\kappa_1)}$$

$$I_2 = I_{DS2} = SI_{n0}\, \iota_{G2}^{\kappa_2}\, \iota_{B2}^{(1-\kappa_2)}$$

$$I_3 = I_{DS3} = SI_{n0}\, \iota_{G3}^{\kappa_3}\, \iota_{B3}^{(1-\kappa_3)}$$

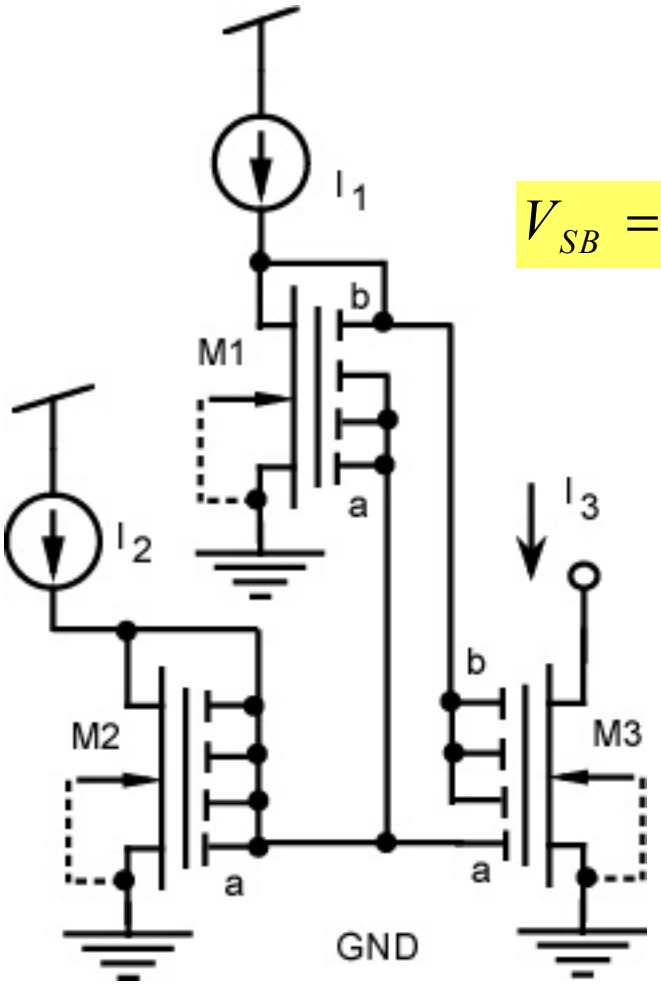
$$I_4 = I_{DS4} = SI_{n0}\, \iota_{G4}^{\kappa_4}\, \iota_{B4}^{(1-\kappa_4)}$$

Solving the eight equations:

$$I_1 I_4 = I_2 I_3 \rightarrow I_4 = \frac{I_2 I_3}{I_1}$$

All gates and substrate voltages must be at about the same voltage so that kappa is the same for all transistors

FGMOS POWER LAW CIRCUIT



$V_{SB} = 0$

From three translinear loops

$$\iota_{3a} = \iota_{2a}$$

$$\iota_{3a} = \iota_{1a}$$

$$\iota_{3b} = \iota_{1b}$$

From *psi-current* definitions

$$I_1 = I_{DS1} = SS_{Q1}\, I_{n0}\, \iota_{1a}^{3\kappa_1/4}\, \iota_{1b}^{\kappa_1/4}$$

$$I_2 = I_{DS2} = SS_{Q2}\, I_{n0}\, \iota_{2a}^{\kappa_2}$$

$$I_3 = I_{DS3} = SS_{Q3}\, I_{n0}\, \iota_{3a}^{\kappa_3/4}\, \iota_{3b}^{3\kappa_3/4}$$

$$I_{DS} \equiv SS_Q\, \iota_B^{(1-\kappa)} \prod_{j=1}^{j=N} \iota_{Gj}^{\kappa/N}$$

$$S_Q \equiv \exp\left(\frac{Q_{FG}}{Q_0}\right)$$

$$Q_{FG} = 0 \rightarrow S_Q = 1$$

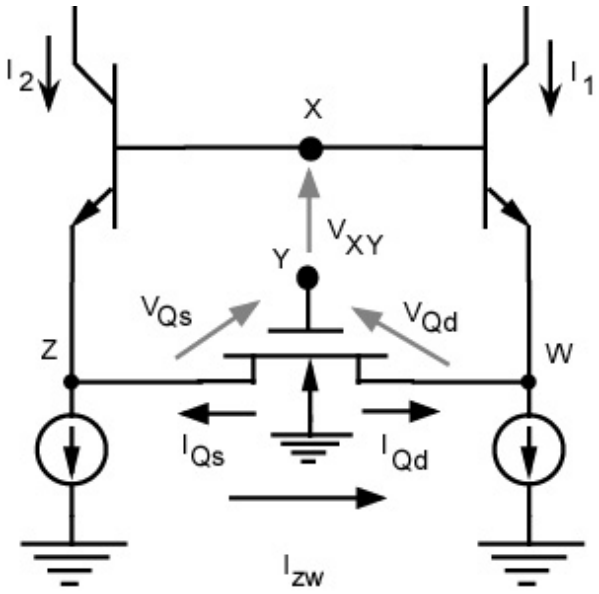
Solving the above

$$I_3 = \frac{I_1^3}{I_2^2}$$

Assuming $\kappa_1 = \kappa_2 = \kappa_3$

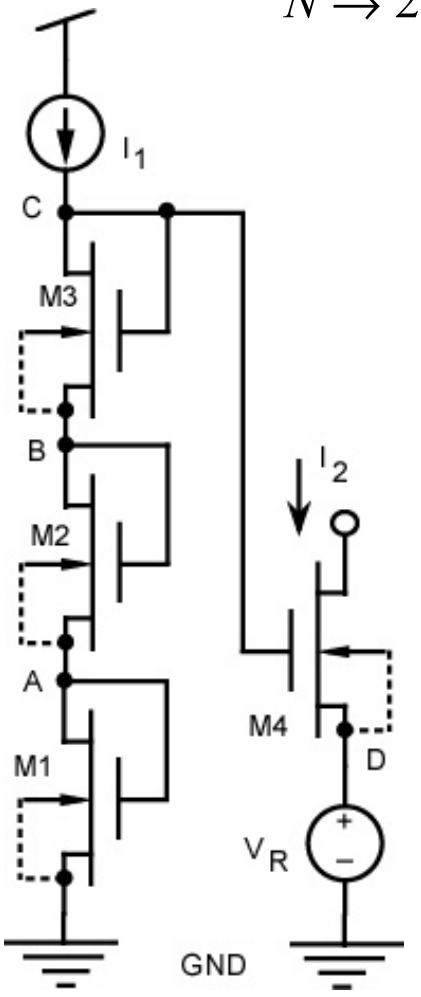
TRANSLINEAR NETWORKS

Translinear Networks: Extension/special case where the loops include voltage sources



$$\frac{I_2 I_4 I_6 \cdots I_N}{I_1 I_3 I_5 \cdots I_{N-1}} = \Gamma \exp^{V/V_t}$$

$$N \rightarrow 2,4,6 \cdots$$



$$\frac{\prod_{CCW} J}{\prod_{CW} J} = \Gamma \exp^{V/V_t}$$

$$I_2 = \frac{I_1^3}{\Gamma \exp^{V_R/V_t}}$$