Lab 4: Subthreshold MOS Characteristics and Model Parameter Extraction

Analog Integrated Circuit Design Laboratory

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The objectives of this lab are:

1. To review MOS transistor concepts and introduce subthreshold MOS behavior.
2. To obtain the current voltage characteristics of an nMOS device and a pMOS device when operating in subthreshold region using the automated data acquisition system.
3. To extract SPICE simulation parameters from the data.

1 Introduction

MOS circuits operating in the subthreshold region are particularly suited for systems where power dissipation is a very important consideration. Inside your electronic watches there is sophisticated circuitry whose operation depends on MOS subthreshold characteristics. A typical watch today has about 100,000 transistors, most of them operating in subthreshold. With an increased interest in low power devices and mobile technologies, subthreshold MOS operation is becoming more and more important. Other devices critical to our every day activities such as cardiac pacemakers and hearing aids also use MOS transistors in subthreshold.

1.1 Current-Voltage Relationships

For nMOS devices in subthreshold, with bias voltages referenced to source with $V_S = 0$ and ignoring Early effects, the drain current is given by

$$I_D = I_{no}\ \ exp((1-\kappa_n)qV_{BS}/kT)\ \ exp(\kappa_n qV_{GS}/kT)\ \ (1-e^{-qV_{DS}/kT}) \tag{1}$$

if $V_B = V_S = 0$

$$I_D = I_{no}\ \ exp(\kappa_n qV_{GS}/kT)\ \ (1-e^{-qV_{DS}/kT}) \tag{2}$$

and if $V_{DS} \geq 4(kT/q)$

$$I_D = I_{no}\ \ exp(\kappa_n qV_{GS}/kT) \tag{3}$$

However, real devices in saturation do not behave like ideal current sources but they show a dependence on V_{DS}. This can be taken into account by adding another term in the model equation so that $(1-e^{-qV_{DS}/kT})$ becomes $(1-e^{-qV_{DS}/kT}+V_{DS}/V_O)$. The parameter V_O is the Early voltage. (Notice that drain conductance in subthreshold is by convention expressed in terms of the Early voltage V_O, rather than in terms of the parameter λ in above threshold.)

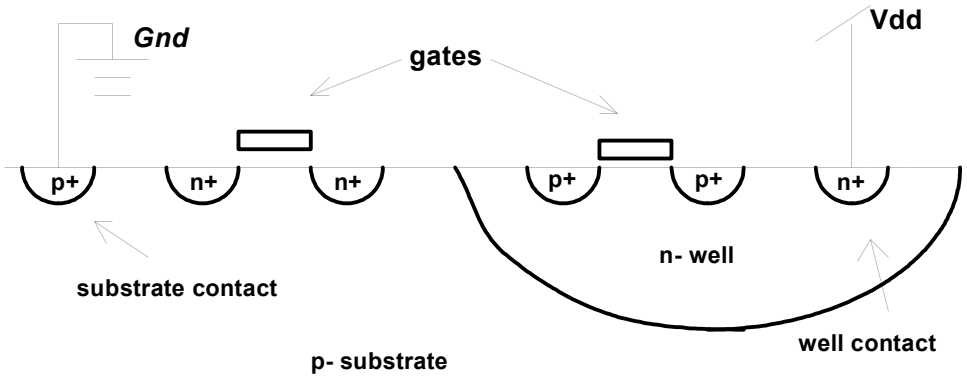

Figure 1: A cross section through an n-well chip.

1.2 n-Well and p-Well Processes

Native transistors are transistors that lie direcly in the substrate. The well transistors are transistors that lie directly in the well. The classchips are fabricated in an n-well process (p-substrate). The native transistors have n-type sources and drains, and the well transistors have p-type sources and drains. The channels formed by the native transistors in the p-type substrate will be n-channels. A vertical section through the silicon with both native and well transistors is shown below.

2 Prelab

1. What is the relationship between the Early voltage V_O in the subthreshold model and the parameter λ in the above threshold model?

2. Calculate, and compare the transconductance g_m of the nMOS transistor above threshold and in subthreshold. The transconductance g_m is defined as the partial derivative of the drain current I_d to the gate-to-source voltage V_{gs}, all other terminals being kept at a constant voltage.

3. Sketch the cross section of a p-well chip, with one nMOS transistor (MN) and one pMOS transistor (MP). Label the two transistors and all their terminals, as well as your substrate and well contacts. Should the well voltage be higher or lower than the substrate voltage for proper operation?

3 Laboratory Work

Warning: We are going to use MOS devices throughout our experiments. The thin oxide between the gate and the channel of the device has a dielectric breakdown voltage in the range of 10-20 Volts. Thus great care should be taken in handling the *pop2u* chip.

Keep the devices in their storage tubing or on your bread-board when not used. You should also follow some rules so that your body capacitance gets discharged before handling the devices. For example *before* handling any component you should touch something that is grounded such as the grounding lead in your power supply module or the oscilloscope case. As you have probably noticed, the ICs that we will use in the class come in special conductive medium (the plastic tubes are indeed conductive) or special conductive black foam.

Never walk around the lab holding your devices. Static charge is accumulated by friction between your shoes and the floor. Once your chip is placed on the breadboard and you have made connections, there is no danger from electrostatic discharge.

3.1 Subthreshold Output Characteristics of an nMOS device

Obtain the output characteristics for one of the larger nMOS transistors on the *pop2um* chip. The output characteristics are a set of I_{ds} vs V_{ds} curves for different values of the gate-source voltage V_{gs}. For this experiment set $V_{bs} = 0$ by shorting the source and the substrate (or well) contacts. Run the experiments for $V_{gs} = 0.6, 0.625$ and 0.650 Volts. The value for V_{ds} should be varied from 0 to 3 Volts at 0.01 Volt intervals. **Hint:** You will need to experiment with the resistor in this lab. Start with a small value and increase it until you get a measurable signal.

Plot your data so that you get something like the data last week. Save your matlab workspace on your diskette.

3.2 Subthreshold Transfer Characteristics of an nMOS device

Obtain the transfer characteristics for one of the larger transistors on the *pop2um* chip. The transfer characteristics are a set of I_{ds} vs V_{gs} curves for different values of the substrate-source voltage V_{bs}. For this experiment set $V_{ds} = 3$ Volts. Run the experiments for $V_{bs} = 0, -1$ Volts. The value for V_{gs} should be varied from 0.4 to 1 Volts at 0.01 Volt intervals. This is going to be tricky! Note that the currents in the transistor are changing exponentially in voltage, much like the currents in the diode. You will have to use several resistors to measure the currents over such a wide dynamic range.

Plot your data to make sure you are getting something worth saving and then save your matlab workspace on your diskette. *Hint:* a linear scale on both the x and y axes is not a good idea for this plot, because of the large dynamic range in currents.

3.3 Subthreshold Characteristics of a pMOS device

Repeat the above experiments (output and transfer characteristics) for one of the larger pMOS transistors. Again, be careful about the polarity of voltages.

4 Post-Lab Work and Reporting

As usual, do all postlab work on your own, using the data that you have saved on your own diskette.

1. Plot your data for the output characteristics of the two transistors.
2. Show the saturation point on the curves (the drain-to-source voltage at which saturation is reached) and determine its value (in mV).
3. Using similar procedures to those employed in laboratory assignment 3, determine the Early parameter V_O for both transistors. When extracting parameters show all the relevant equations, plots and briefly describe how you got your answers.
4. Plot your data for the transfer characteristics of the two transistors.
5. Assuming that the device behaviour in subthreshold is described by the simple exponential forms as given in the above model, determine from the data the two parameters κ and I_o, for both transistors.
6. What is the geometry of your DUT (Device Under Test)?

5 Next Week

Laboratory 5: Layout of Basic CMOS Amplifiers and Logic Circuits