

Lab 3: Above Threshold MOS Characteristics and Model Parameter Extraction

Analog Integrated Circuit Design Laboratory

December 18, 2000

The objectives of this lab are:

1. To become acquainted with the *pop2um* chip, a transistor test array chip in $2\ \mu\text{m}$ BiCMOS technology designed specifically for this course, that contains a variety of MOS.
2. To obtain the current voltage characteristics of nMOS and pMOS devices using the automated data acquisition system.
3. To extract SPICE simulation parameters from the data.

1 Introduction

Computer Aided Design tools are widely used today by electrical engineers to prototype their circuits. One such program is SPICE and its accuracy in simulating complex circuits depends on the models used, as well as on the values for various parameters that are given in the models. We have already used models of a diode (1N4148), an nMOS transistor (NMOS), and a pMOS transistor (PMOS) in earlier simulation lab assignments. In this lab we will experimentally determine realistic model parameters for the devices found in an MOS transistor array that will be used throughout the course. We begin with above threshold operation; the region where most of digital VLSI circuits and systems operate.

1.1 Defining Terms: A review

The following is a summary of important terms, definitions, and related equations. Note that the definitions marked 'n-channel' are also valid for p-channel if one reverses the polarity of voltages and interchanges the n- and p-doped regions.

- **substrate:** The silicon slab onto which the integrated circuits and circuit elements are built. It is usually lightly doped so that it has extra, lightly-bound electrons (negative carriers: n^- substrate), or holes in the valence shell (positive carriers: p^- substrate).
- **well:** Section of chip which is doped opposite to that of the rest of the substrate.
- **channel:** Region between drain and source of transistor. The potential in this region is controlled by the gate voltage and determines current flow.
- **n-channel:** Transistor which uses electrons as carriers. The drain and source are negatively doped.
- **p-channel:** Transistor which uses holes as carriers. The drain and source are positively doped.

- **above threshold:** (n-channel) Operation of the MOS transistor where the gate voltage exceeds the threshold voltage. The gate is positive with respect to substrate to the extent that the channel has lots of carriers of the opposite type (electrons) and conducts between drain and source. The channel has effectively become an n-type region, like drain and source. I_D is quadratic in V_{GS} .
- **subthreshold:** (n-channel) Operation of the MOS transistor where gate voltage is below the threshold voltage, in the absence of channel inversion. Current in the channel flows by diffusion (governed by Boltzman statistics) and is relatively small (typically picoamps to nanoamps for a square device); I_D is exponential in V_{GS} over several orders of magnitude in current.
- **saturation:** I_D is approximately constant for a given V_{DS} and V_{GS} . The device behaves like a current source. In the *subthreshold* region, this happens at approximately $V_{DS} \geq 4(kT/q)$.

1.2 MOS Transistor Model Parameters Above Threshold

The Shichman-Hodges model for the nMOS transistor has the following form for the drain current I_D as a function of gate-to-source voltage V_{GS} and drain-to-source voltage V_{DS} :

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad (1)$$

which is valid in above threshold operation (for V_{GS} sufficiently large, $V_{GS} > V_T$), and in saturation (for V_{DS} sufficiently large, $V_{DS} > V_{GS} - V_T$). The parameters W and L are determined by the geometry of the layout, and are given. The threshold voltage V_T varies with the and bulk-to-source voltage V_{BS} as:

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) . \quad (2)$$

The parameter ϕ is the flat-band surface potential, and its value is typically approximated as 0.6 Volts, since its precise value does not seem to be critical. The process parameters to be extracted from the measurements are then the transconductance parameter K' , the zero-bulk threshold voltage V_{T0} , the bulk coefficient γ , and the Early effect λ . The equations for the pMOS transistor are similar, except for the appropriate sign reversals (See the equations in Sedra and Smith, or Geiger, Allen and Strader). The values for the pMOS process parameters are different from those of their nMOS equivalents, because of differences in mobility, doping profile, etc. Typically, K'_n for an nMOS transistor is a factor 2.5 larger than K'_p for a pMOS transistor in the same process.

1.3 The *pop2um* Chip

We will use the *pop2um* chip throughout the course to measure and characterize MOS transistors and test single circuits composed of them. The *pop2um* chip contains several isolated nMOS and pMOS transistors, as well as inter-connected transistors that will be useful for constructing simple circuits in future labs. The pin diagram of the chip is shown in the "pop2um.pdf" file.

2 Prelab Assignment

2.1 *pop2um* Study:

1. Download the *pop2um.tdb* file, and load it into L-Edit in the computer lab. (Note that the file is large and therefore the student version of LEDIT may not handle it.)
2. Familiarize yourself with the chip, from observing the pin diagram in correspondence with the array of cells in *pop2um.tdb*.

3. Figure out how to configure the inputs of the chip and how to connect the chip to your instrumentation hardware to do the measurements in the experiments below. Find the pins for source, drain, gate, bulk, GND, and Vdd (5V), and determine what voltage to apply to all of the input pins. (There may be more than one solution, since there are several identical transistors on this chip!)

2.2 Parameter Extraction:

It will be useful to read Section 3.1.4 in the Geiger, Allen and Strader book. It describes possible procedures to perform the experiments and extract the parameters for this week's laboratory assignment.

1. Show that the parameter λ can be obtained from linear regression on data of I_{DS} as a function of V_{DS} , for constant V_{GS} and V_{BS} . Sketch roughly how the data will look like, and in which region the regression will yield valid results.
2. Show that the parameters K' and V_{T0} can be obtained from linear regression on (square root transformed) data of $\sqrt{I_{DS}}$ as a function of V_{GS} , for constant V_{DS} , and for zero V_{BS} . Sketch roughly how the data will look like (accounting for the square root of current), and in which region the regression will yield valid results.
3. *Bonus* (10 % extra credit): Show that the parameter γ can be obtained from linear regression of (transformed) data obtained using the previous procedure but for different (non-zero) values for V_{BS} . You may assume that an estimate for ϕ is given. Sketch the procedure graphically.

2.3 Parameter Extraction:

1. Prepare (and print out) a MATLAB script `sweep(Vmin, Vmax, n, Vfixed)` to measure an output current I_{out} as a function of an input voltage, V_{in} , swept between V_{min} and V_{max} in $nsteps$ equidistant steps, while keeping the second voltage constant at a level V_{fixed} . Assume you are using one of the A/D channels (with your "home-brewed" ammeter) for I_{out} , and both D/A channels for V_{in} and V_{fixed} . You will be able to use this routine to do the above measurements, as well as other ones in future labs.
2. Based on a typical value of $K' = 25 \times 10^{-6} \text{ A/V}^2$ for nMOS transistors, estimate the range of resistance values R that you will need to do the current measurements using your "home-brewed" ammeter.

3 Laboratory Work

Warning: We are going to use MOS devices on the chips throughout our experiments. The thin oxide between the gate and the channel of the device has a dielectric breakdown voltage in the range of 10-20 Volts. Thus great care should be taken in handling the chips.

The following additional precaution procedures if followed should decrease the possibility of damaging your devices.

Keep the devices in their storage tubing or on your bread-board when not used. You should also follow some rules so that your body capacitance gets discharged before handling the devices. For example, *before* handling any component, you should touch something that is grounded such as the grounding lead in your power supply module or the oscilloscope case. As you have probably noticed, the I.C's that we will use in the class come in special conductive medium (the plastic tubes are indeed conductive) or special conductive foam (black).

Never walk around the lab holding your devices. Static charge is accumulated by friction between your shoes and the floor. Once your chip is placed on the breadboard and you have made connections, there is no danger from electrostatic discharge.

3.1 Review of General Laboratory Procedures

Use your own customized wiring (twisted pairs or triplets) for all your connections to the instruments. Keep a consistent color code for the GND, V+ and V- as well as for inputs and outputs. Your breadboard layouts should be neat. Double check all the wiring, and have one of the T.A.'s or the instructor verify again, before applying power. Your operational amplifiers that are used in the instrumentation are very sensitive to wrong power supply polarity. Do not hesitate to ask one of us if you are in doubt about something. We will not mind any questions regardless how "stupid" you may think they are, but we will not easily forget irresponsible actions that blow chips or that cause malfunctioning instrumentation equipment.

3.2 Output Characteristics of an nMOS device

Obtain the output characteristics for one of the larger nMOS transistors on the *pop2um* chip. The output characteristics are a set of I_{DS} vs V_{DS} curves for different constant values of the gate-source voltage V_{GS} . For this experiment set $V_{BS} = 0$ by shorting the source and the substrate (or well) contacts. Run the experiments for $V_{GS} = 1, 2, 3, 4$ and 5 Volts. The value for V_{DS} should be varied from 0 to 5 Volts at 0.1 Volt intervals. With this range of voltages, you can expect currents in the hundreds of microamps range.

Don't forget to connect the substrate to GND! Plot your data, and extract a value for λ using the procedure derived in the prelab. Save your matlab workspace on your diskette.

3.3 Transfer Characteristics of an nMOS device

Obtain the transfer characteristics for one of the large transistors on the *edl2* chip. The transfer characteristics are a set of I_{DS} vs V_{GS} curves for different values of the substrate-source voltage V_{BS} , at constant V_{DS} . For this experiment set $V_{DS} = 5$ Volts. Run the experiments for $V_{BS} = 0, -1, -2$ and -3 Volts. The value for V_{GS} should be varied from 0 to 5 Volts at 0.1 Volt intervals. With this range of voltages you can again expect currents in the hundreds of microamps range.

Plot your data to make sure you are getting something worth saving and then save your matlab workspace on your diskette.

3.4 Output and Transfer Characteristics of a pMOS device

Repeat the two experiments for one of the large pMOS devices on the *pop2um* chip. Be careful about the polarity of voltages and currents for the pMOS transistor in comparison with the nMOS transistor! Make sure to connect the bulk voltage (well contact, see *pop2um.pdf*) at all times.

4 Post-Lab Work and Reporting

As usual, one copy of the lab report is due per group one week after the lab session. Include all relevant plots and printouts, and label all diagrams appropriately. Provide a *brief* explanation of how you obtained your answers.

1. Plot the data for the output characteristics of the nMOS and pMOS transistors.
2. Plot the data for the transfer characteristics of the nMOS and pMOS transistors.
3. What is the geometry (W and L sizes) of your DUT (Device Under Test), in the case of nMOS and pMOS?
4. Using the procedures outlined in the prelab, estimate from the saved data the parameters K' , V_{TO} , γ , and λ for both nMOS and pMOS. For the estimate of γ , you may assume $\phi \approx 0.6$ V. (Bonus, 10 %: also obtain an estimate for ϕ directly from your measurements.)

5 Next Week

Laboratory 5: Subthreshold MOS Characteristics