Digital Integrated Circuits – A Design Perspective 2/e

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Chapter 5

Design Project: Optimizing a Inverter Chain with Fanout
Goal: Minimize Extra Delay for Given Energy Reduction

Background Information

You are given technology parameters that are essential in propagation delay analysis. These parameters are extracted by curve fitting simulated results of an inverter delay in our 0.25μm technology, as shown in Fig. 1.

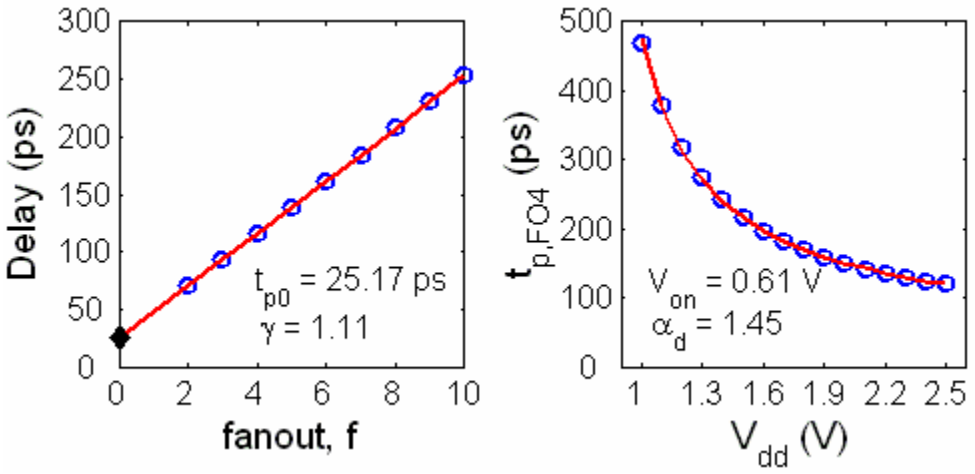

Figure 1: Extraction of delay parameters: (a) t_{p0}, γ, (b) V_{on}, α_d. (W_p/W_n=2μ/1μ, L=0.25μ)

All parameters are extracted using the same test circuit as that given in Hw 5/Prob 4. (on a side note, values of t_{p0} and γ shown in Fig. 1 is the solution to this homework problem!) Parameters t_{p0} and γ will aid in calculation of the gate delay as given by:

$$t_p = t_{p0} \cdot \left(1 + \frac{f}{\gamma}\right) \tag{1}$$

where t_{p0} is the intrinsic delay of an inverter, ***f*** is the fanout, and $\gamma = C_{intrinsic}/C_{gate}$ is the ratio of the input intrinsic to the input gate capacitance.

Parameters V_{on} and α_d are intrinsically related, but not equal to the transistor threshold voltage and velocity saturation index. They are simply fitting parameters that provide the most accurate model of a FO4 inverter delay over a range of supply voltages. Fanout of four is chosen for calibration simply because it is the most typical fanout found in well-designed digital circuits. It also represents good average fanout, so we will use the same parameters for all other fanouts that we are going to encounter in this design project. Relationship between the propagation delay of a FO4 inverter and the power supply V_{dd} is given by:

$$t_p = K_d \cdot \frac{V_{dd}}{(V_{dd} - V_{on})^{\alpha_d}} \qquad (2)$$

where K_d is another fitting parameter, but it is not crucial for our problem setup. It lumps some technology parameters including linearized delay capacitance (similar to the one you had to determine in Hw 4/Prob 4). You will find equation (2) useful in V_{dd}-based optimizations.

Phase 1: Circuit Optimization (1 week)

You have to optimize circuit given in Fig. 2:

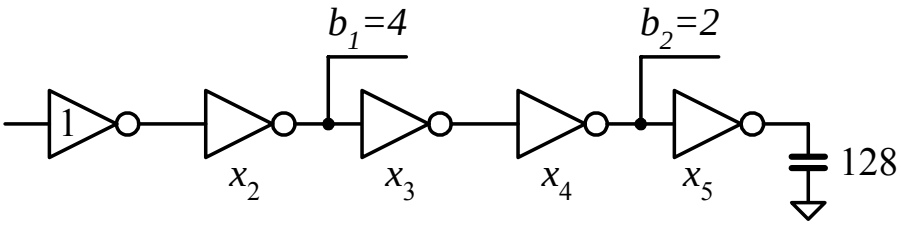

Figure 2: Some group-specific inverter-based topology.

First, find sizes x_2-x_5 of all gates to achieve minimum delay D_{min} from the input to output. What is the value of D_{min} normalized to t_{p0}? What is the energy E_{ref} that corresponds to the minimum delay? For energy calculation, assume $V_{DD} = V_{DD}^{nom} = 2.5V$. Express E_{ref} in terms of energy required to drive the input gate capacitance $C_{gate} = 1$ (call this number "1", it is simply a reference case, you do not need value in fF in your calculations) of the first gate in the chain. Now, you obtained reference point (D_{min}, E_{ref}) for your optimizations.

Assume now that you have to reduce energy by x% {choose from -20%, -30% and -40%}. For the newly specified energy, perform following three optimizations in order to minimize delay penalty of the reference design.

a) Gate size (W) optimization

What are the new sizes of all the gates x_2-x_5?

What is the achieved percent delay penalty, $DP_W = 100(D_W/D_{min} - 1)$?

b) Supply voltage (Vdd) optimization

What is the value of the new supply voltage, V_{DD}^{opt}?

What is the achieved percent delay penalty, $DP_{Vdd} = 100(D_{Vdd}/D_{min} - 1)$?

c) Combined size and supply voltage (W-Vdd) optimization

What are the new sizes of all the gates x_2-x_5?

What is the value of the new supply voltage, V_{DD}^{opt}?

What is the achieved percent delay penalty, $DP_{W\text{-}Vdd} = 100(D_{W\text{-}Vdd}/D_{min} - 1)$?

Clearly show your design methodology and summarize all results in following Table:

Summary of results from Phase-1: D_{min} (t_{p0}) = E_{ref} =

Opt. case	DP (%)	V_{DD}^{opt}	x_2	x_3	x_4	x_5
Reference	0%	2.5V				
W		2.5V				
Vdd						
W-Vdd						

Phase 2: Verification in HSPICE (1/2 week)

Using HSPICE, verify results of your optimizations from Phase-1.

a) Obtain reference point (D_{min}, E_{ref}) in HSPICE. Is it different from what you expected? (*Hint-1*: C_D and C_E from Prob 4/Hw 4 could help, but don't blame everything on them!) (*Hint-2*: To determine energy dissipated in driving the input gate capacitance in HSPICE verification, you may want to use some of the results from background section and/or use HSPICE to estimate this energy)

b) Using parameters (gate size, V_{DD}^{opt}) from Phase-1, report achieved energy reduction ER and achieved delay penalty DP for all three optimization cases. Normalize numbers relative to the reference case (D_{min}, E_{ref}) obtained by HSPICE in part (a) of Phase-2. Comment your results.

Summary of results from Phase-2:

Reference	D_{min} (ps)		E_{ref} ($E_{in\text{-}1st\ stage}$)	
	HSPICE	**Phase-1**	**HSPICE**	**Phase-1**
Verification	**ER (%)**		**DP (%)**	
	HSPICE	**Phase-1**	**HSPICE**	**Phase-1**
W				x%
Vdd				x%
W-Vdd				x%

Phase 3: MAX Layout (1/2 week)

Layout the last two stages of circuit in Fig. 2 when sized for D_{min}. Do not layout branching gate at the output of the 4th stage. The objective is to minimize area and achieve aspect ratio as close to 1 as possible. Report following numbers (layout must be DRC-error-free!):

a) Total layout area

b) Layout aspect ratio

Summary of results from Phase-3:

Total layout area (μm^2)	Aspect ratio