Digital Integrated Circuits – A Design Perspective 2/e

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Chapter 5

Design Project: Optimizing a Clock Driver

1. Clock Drivers – Background

The clock is one of the most important signals on a chip. It ensures that all events are properly ordered, and that the data reaches equilibrium state before being passed to the next stage. Later in the semester, we will learn the distribution of the clock over a complete chip is a complex topic, and one of the main challenges in the design of today's high-performance processors.
In this project, we address one aspect of the clock-distribution problem, namely the buffer design. Since the clock is connected to a large number of components, its load is huge. The typical load consists of the clock distribution wires, and the clock inputs of the registers. Clock drivers and buffers have to be inserted between the clock source (we assume in this case that the clock is generated off-chip), and the load to ensure that the clock signal at the register inputs has sharp rise and fall times, and that the latency between input- and output is within bounds. Most importantly, it is crucial that the clock arrives at approximately the same time at all the register inputs. The differential in the arrival time of the clock signals at the register inputs is called the skew. We will see later in the semester that the clock skew is one of the important performance-limiting factors. The goal of the project is to design a set of clock buffers so that the skew to all the flip-flops is bounded.

1.1. High level structure

The high-level block diagram of the chip we are designing is shown in Figure 1.

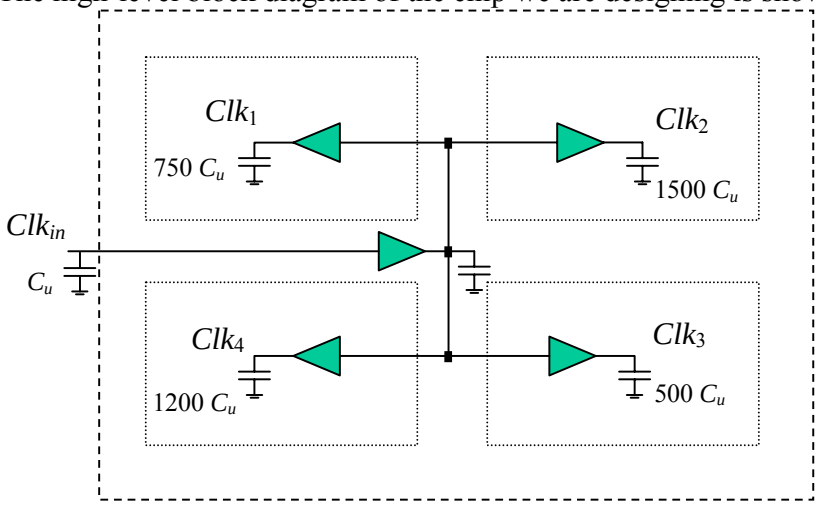

Figure 1. Clock distribution diagram

An external clock (Clk_{in}) is routed to the center of the chip, where the first buffer is located. The chip itself is divided into four quadrants. The buffered clock is distributed to each of the quadrants, where a second buffer stage is inserted, which drives the final loads (as annotated on the Figure as a function of the unit capacitance *Cu*, which is the input capacitance of the first buffer, and is equal to the input capacitance of a minimum-sized inverter (This means that the first stage of the first buffer MUST be a minimum-sized inverter). As each of the quadrants differs in complexity, the load it presents varies. Observe that each gray "buffer" box represents a chain of inverters.
Our goal is to design the different buffers (number of stages, device sizes) such that a number of specifications are met:

- The number of inversions between the input clock signal and the load MUST be even.
- The rise and fall times of all clock signals (Clk_1 – Clk_4, as well as the intermediate clock signal) are constrained.
- The clock skew (this is the difference in propagation delays) between the final clock signals (Clk_1 – Clk_4) is bounded.
- Energy dissipation of the clock distribution system is minimized.

In this project, we **ignore the wiring capacitance** (which is an important component of any real clock distribution system), and ignore the delay of the wires as well.

2. Implementation and Constraints

The goal is to derive the transistor schematics of the buffers, so that the design constraints are met. We will also **layout one of the buffers** (the one driving Clk_2), and compare its actual performance with the one predicted from the schematics.

The constraints are as follows:

- t_{rise} and t_{fall} < 1000 psec
- t_{skew} < 50 psec

The following design parameters are also given:

- V_{supply} = 2.5 V
- t_{rise} and t_{fall} of Clk_{in} = 0.5 nsec

The prime goal is to design the buffers such that the overall energy dissipation of the buffers is minimized.

The project is to be **done in pairs**.

2.1. TECHNOLOGY: The design is to be implemented in a 0.25 μm CMOS process with 4 metal layers. The SPICE technology is in the g25.mod file.

2.2. PERFORMANCE METRICS: The propagation delay for static designs is defined as the time interval between the 50% transition point of the inputs and the 50% point of the worst-case output signal. Make sure you pick the worst-case condition and state EXPLICITLY in your report what that condition is.

2.3. **RISE AND FALL TIMES**: All rise and fall times are defined between the 10% to 90% points.

2.4. **ENERGY CONSUMPTION:** The energy consumption is defined as the total energy drawn from the supply during a single clock period (this is, a 0->1 and a 1->0 transition of Clk_{in})

2.5. **AREA**: The area is defined as the smallest rectangular box that can be drawn around the design of your buffer.

3. Simulation

Analyze the circuit by using SPICE. Your simulation result should prove that your design meets the required specs. A simulation diagram detailing power dissipation should also be produced.

3. Layout

Your layout should obey all design rules. Important is that sufficient well and substrate contacts are included. At least one well/substrate contacts should be placed within 25 μm distance of any diffusion region. Also make sure to size the power rails appropriately, so that they can carry the peak current drawn from the buffer. The rule to use here is that the current density should not exceed 1 mA/μm. Make sure that you layout wide transistors appropriately – this is use finger-structures.

5. Report

The quality of your report is as important as the quality of your design. One must sell the design by justifying the design decisions and by providing all the vital information. Be sure to emphasize relevant information and to eliminate unnecessary material. **Organization, conciseness, and completeness are of paramount importance.** Do not repeat information we already know. Use the templates provided on the web-page (in Framemaker, Word, and PDF formats). E-mail the electronic submission of your report as a Framemaker, Word, or PDF file to the instructors. Make sure to fill in the cover-page and **use the correct units**.

4.1 Report Format

Your report should discuss your overall design philosophy and the important design decisions made at the logic and circuit level. Discuss why your approach reduces energy, while meeting the performance specifications. Provide your estimates of the results, and describe how you arrived at them. Include schematics and highlight the important elements. Describe why the final results deviate from the initial estimates.

Prove that your results are accurate by providing the crucial plots (don't forget to mention the input patterns used to obtain those plots). The total report should not contain more than four pages. You are not allowed to add any other sheets. The organization of the report should be based on the following outline:

Coversheet (use standard form) – and fill in important results

Page 1: Executive summary, overall design decisions, and motivations. Discuss the methodology

Page 2: Transistor diagrams, annotated with transistor sizes.

Page 3: Timing and energy simulations – These should clearly demonstrate that your claimed results are true. Discuss the deviations between pre- and post layout results.

Page 4: Layout of the buffer. Discuss the deviations between pre- and post-layout.

Lastly, you are required to e-mail the SPICE INPUT DECK used to analyze the energy. Remember, a good report is like a good layout: it should perform its function (convey information) in the smallest possible area with the least delay and energy (to the reader) possible.