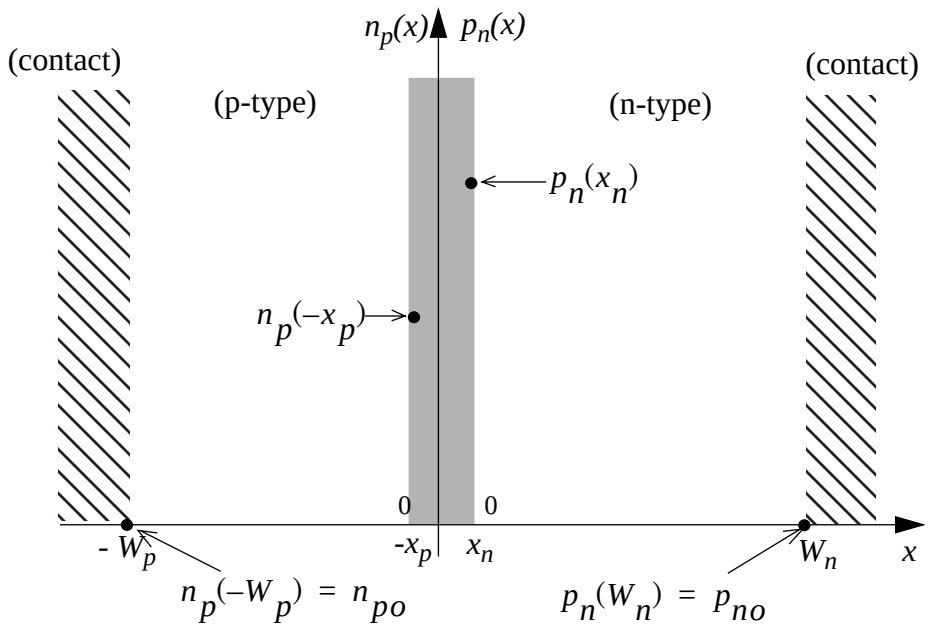
Carrier Concentrations under Forward Bias

- Apply the Law of the Junction at the edges of the depletion region



- Numerical values: $N_a = 10^{18}$ cm^{-3}, $N_d = 10^{17}$ cm^{-3}

  V_D = 0.72 V = 720 mV, V_{th} = 26 mV (warm room) ... example values; note that V_D must be known precisely to substitute into exp[V_D/V_{th}].

$$n_p(-x_p) = 10^2 \text{ cm}^{-3} \exp[720/26] = 10^{14} \text{ cm}^{-3}$$

$$p_n(x_n) = 10^3 \text{ cm}^{-3} \exp[720/26] = 10^{15} \text{ cm}^{-3}$$

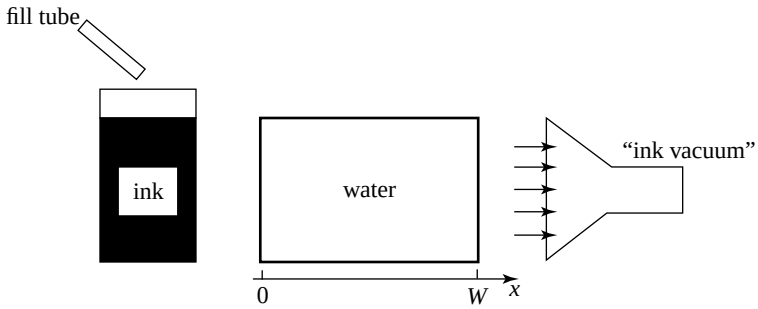
- The minority carrier concentration is maintained at thermal equilibrium at the ohmic contacts

Diffusion Transport in Steady-State

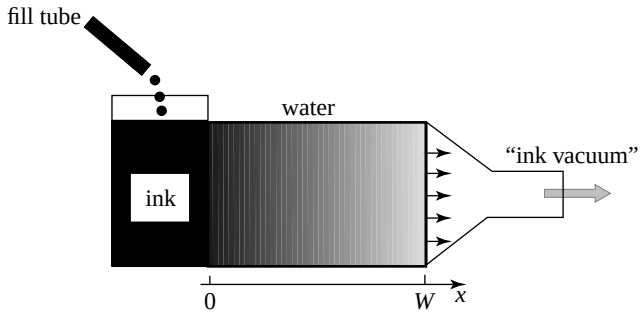
- How do we “fill in the blanks” between the contacts and the depletion region?

  Steady-state --> minority carriers must be continuously injected across the junction to keep $p_n(x_n) >> p_{no}$ and $n_p(-x_p) >> n_{po}$ and continously extracted at the contacts; huge gradient in minority carrier concentrations across the n and p regions --> transport occurs by *diffusion*.

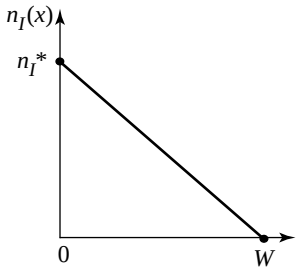
- Conceptual experiment:



(a)



(b)



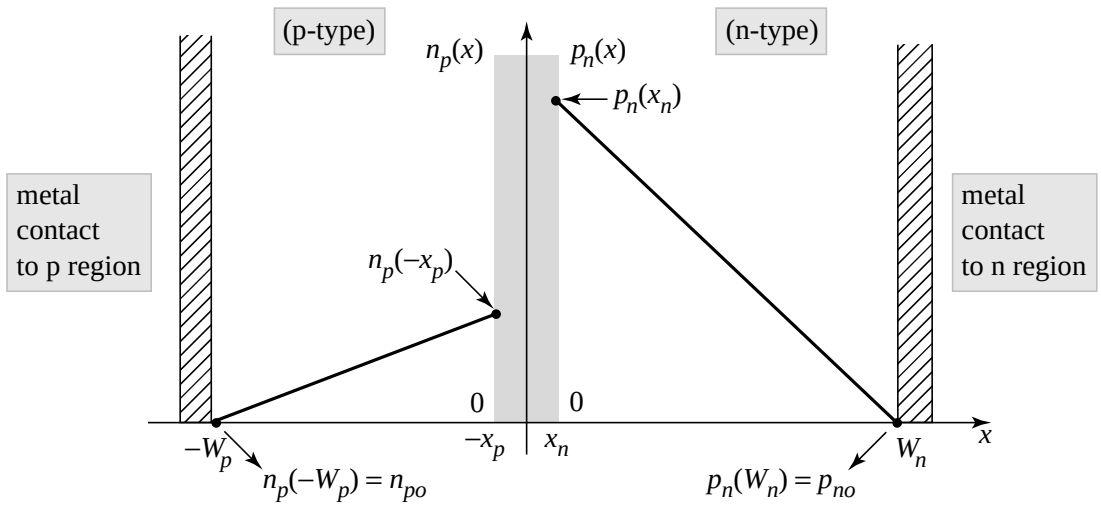
(c)

The Short-Base Solution

- Carrier concentrations --> linear solutions if we assume that the p-type and n-type regions are so short that all of the diffusing minority carriers "make it" across to the ohmic contacts

  In n-type region: $J_p^{diff} = -\, qD_p dp_n / dx$ = constant --> $p_n(x)$ is *linear*

  In p-type region: $J_n^{diff} = qD_n dn_p / dx$ = constant --> $n_p(x)$ is *linear*



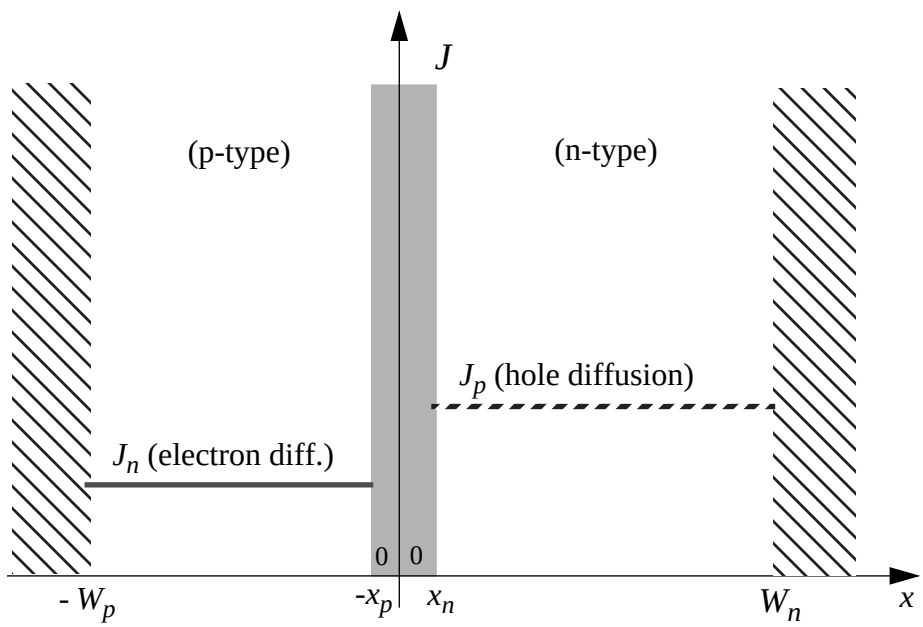
Current Densities

- Minority carrier diffusion currents

$$J_n^{diff} = qD_n \frac{dn_p}{dx} = qD_n \left(\frac{n_p(-x_p) - n_p(-W_p)}{W_p - x_p} \right) = qD_n n_{po} e^{V_D/V_{th}}$$

$$J_p^{diff} = -qD_p \frac{dp_n}{dx} = -qD_p \left(\frac{p_n(W_n) - p_n(x_n)}{W_n - x_n} \right) = qD_p p_{no} e^{V_D/V_{th}}$$

- Plot of minority carrier diffusion current densities

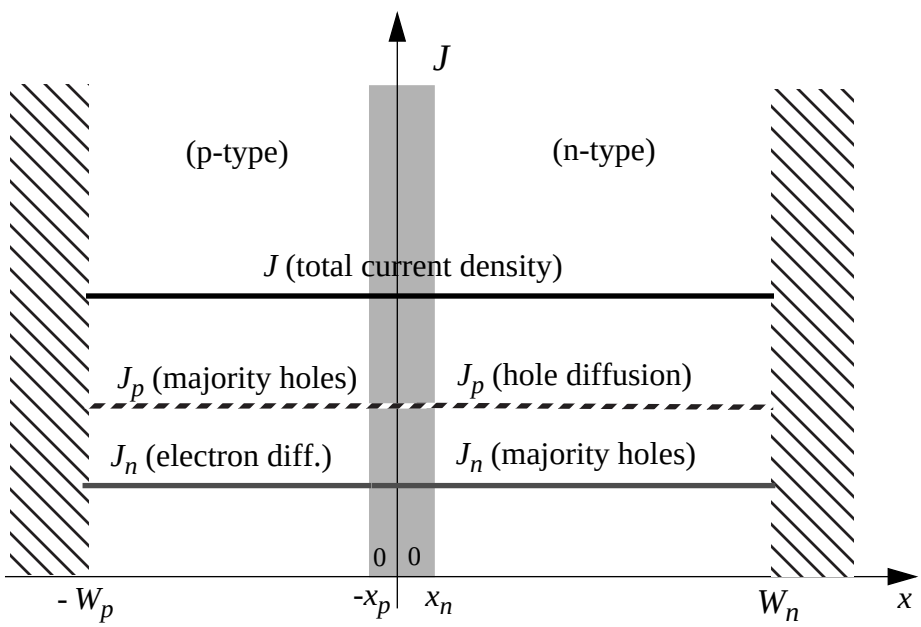


- Minority carriers are injected from the other side of the junction ... how do they get there? *by a majority carrier current density*

Total Current Density

- The total current density is the sum of the minority electron and hole diffusion current densities at the junction ... and is constant through the diode

$$J = J_n^{diff} + J_p^{diff}$$



$$J = q\left(\frac{D_n n_{po}}{W_p - x_p} + \frac{D_p p_{no}}{W_n - x_n}\right)(e^{V_D/V_{th}} - 1)$$

- Diode current: multiply by area A and note that x_n, $x_p << W_n$, W_p

$$I = qn_i^2\left(\frac{D_n}{N_a W_p} + \frac{D_p}{N_d W_n}\right)(e^{V_D/V_{th}} - 1) = I_o(e^{V_D/V_{th}} - 1)$$

Multistage Amplifiers

- Single-stage transistor amplifiers are inadequate for meeting most design requirements for **any** of the four amplifier types (voltage, current, transconductance, and transresistance.)
- Therefore, we use more than one amplifying stage. The challenge is to gain insight into when to use which of the **12** single stages that are available in a modern BiCMOS process:

  Bipolar Junction Transistor: CE, CB, CC -- in npn and pnp* versions

  MOSFET: CS, CG, CD -- in n-channel and p-channel versions

  * in many BiCMOS technologies, only the npn BJT is available
- How to design multi-stage amplifiers that satisfy the required performance goals?

*** Two fundamental requirements:**

1. Impedance matching:

output resistance of stage n, $R_{out,\,n}$ and input resistance of stage $n + 1$, $R_{in,\,(n+1)}$, must be in the proper ratio

$R_{in,\,(n+1)} / R_{out,\,n} \rightarrow \infty$ or $R_{in,\,(n+1)} / R_{out,\,n} \rightarrow 0$

to avoid degrading the overall gain parameter for the amplifier

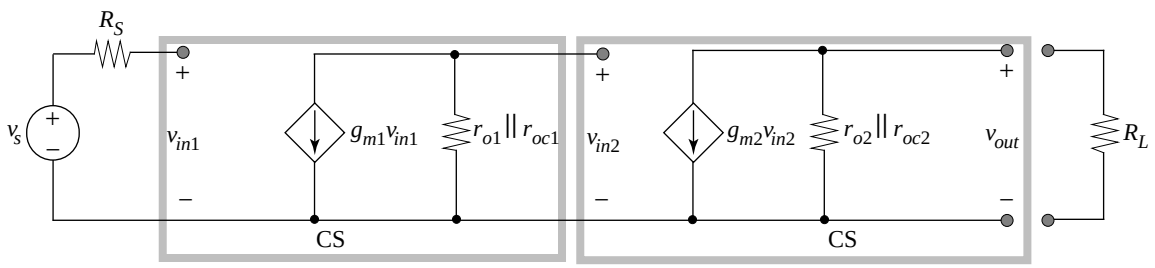
2. DC coupling:

direct connection between stages --> interaction between biasing sources must be considered (later)

Cascaded Voltage Amplifier

- Want R_{in} --> infinity, R_{out} --> 0, with high voltage gain.

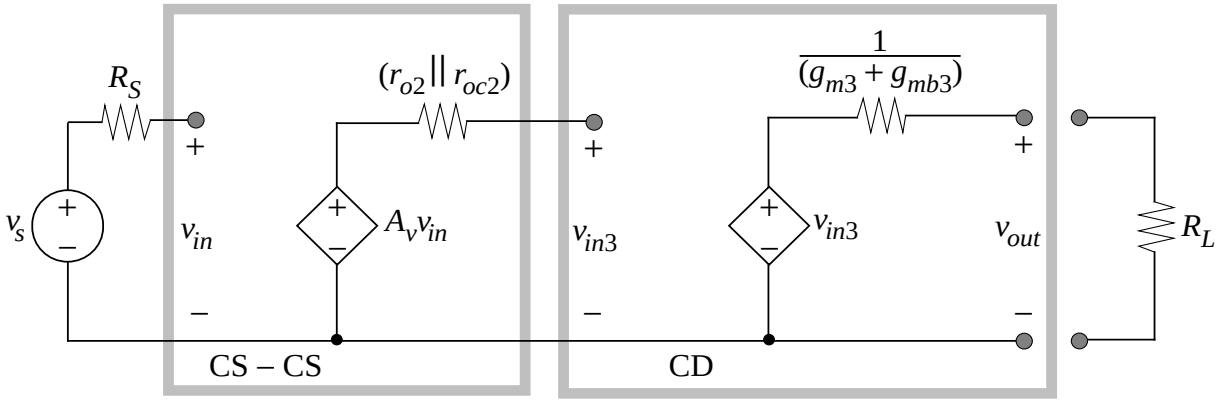
  Try CS as first stage, followed by CS to get more gain ... use 2-port models



- solve for overall voltage gain ... higher, but $R_{out} = R_{out2}$ which is too large

Three-Stage Voltage Amplifier

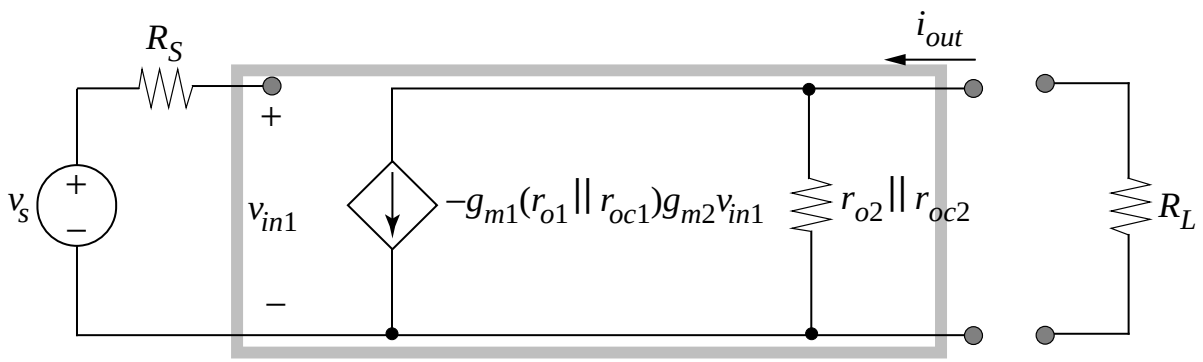
- Fix output resistance problem by adding a common drain stage (voltage buffer)



- Output resistance is not that low ... few kΩ for a typical MOSFET and bias --> could pay an area penalty by making (W/L) very large to fix.

Transconductance Amplifier

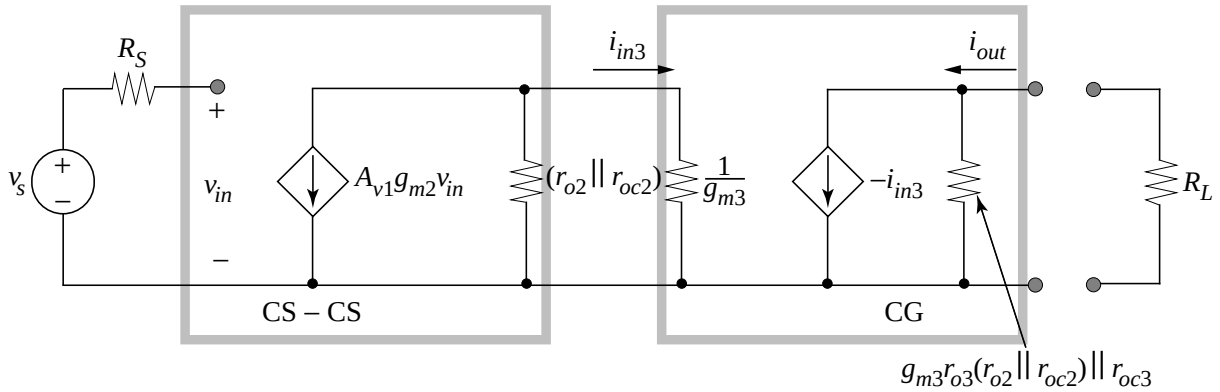
- input resistance should be high; output resistance should also be high
- initial idea: use CS stages (they are “natural” transconductance amps)



- Overall $G_m = - g_{m1} (r_{o1} \| r_{oc1}) g_{m2} = A_{v1} g_{m2}$ ... can be very large
- Output resistance is only moderately large

Improved Transconductance Amplifier

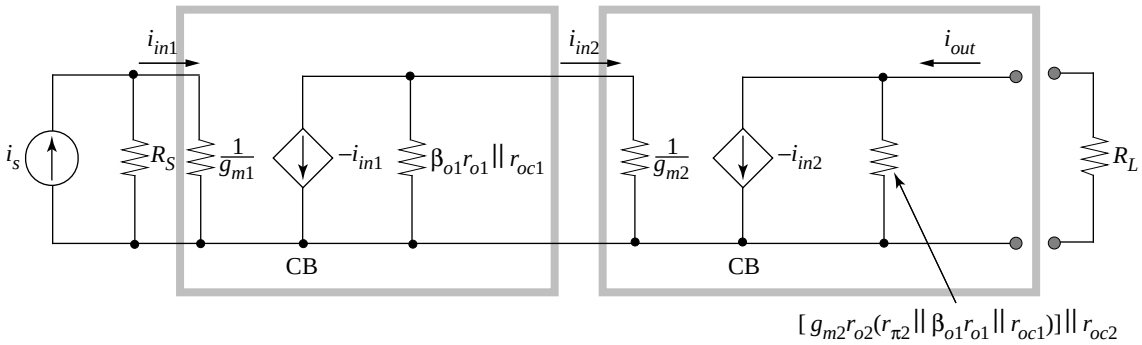
- Output resistance: boost using CB or CG stage



- high-resistance current sources are needed to avoid having r_{oc3} limit the resistance

Two-Stage Current Buffers

- since one CB stage boosted the output resistance substantially, why not add another one ...



- The base-emitter resistance of the 2nd stage BJT is $r_{\pi 2}$ which is much less than the 2nd stage source resistance = 1st stage output resistance

$$R_{S2} = R_{out1} = \beta_{o1}r_{o1} || r_{oc1}$$

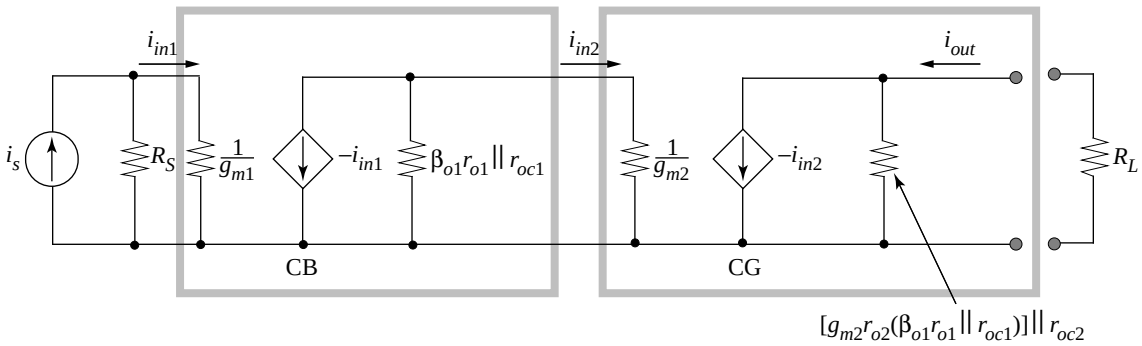
- Therefore, the output resistance expression reduces to

$$R_{out} \approx g_{m2}r_{o2}r_{\pi 2} || r_{oc2} = \beta_{o2}r_{o2} || r_{oc2}$$

... no improvement over a single CB stage

Improved Current Buffer: CB/CG

- The addition of a common-gate stage results in further increases in the output resistance, making the current buffer closer to an ideal current source at the output port



- The product of transconductance and output resistance $g_{m2}\, r_{o2}$ can be on the order of 500 - 900 for a MOSFET --> R_{out} is increased by over two orders of magnitude

  Of course, the current supply for the CG stage has to have at least the same order of output resistance in order for it not to limit the overall R_{out}.

Practical limit ... on the order of 100 MΩ

DC Coupling: General Trends

- **Goal**: want both input and output to be “centered” at halfway between the positive and negative supplies (or ground, for a single supply) -- in order to have maximum possible swing at the input and at the output.

  Summary of DC shifts through the single stages:

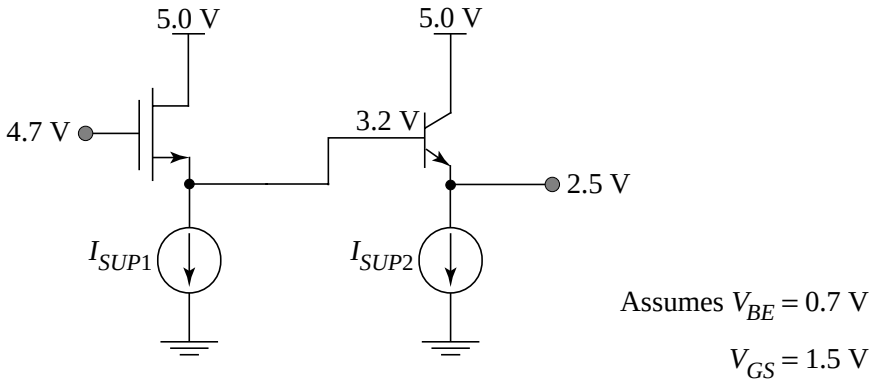
BJT Amp. Type	npn version	pnp version
CE	positive	negative
CB	positive	negative
CC	negative*	positive*

MOS Amp. Type	n-channel version	p-channel version
CS	positive	negative
CG	positive	negative
CD	negative*	positive*

The DC voltage shifts for CC/CD stages are set by the V_{BE} = 0.7 V drop or by the V_{GS} of the transistor and can be specified by the designer.

DC Coupling Example

- Common drain - common collector cascade (infinite input resistance, fairly low output resistance, unity voltage gain ... reasonable voltage buffer)



For CC stage, the optimum output voltage of 2.5 V
(centered between + 5 V and ground for maximum swing) -->

$$V_{IN2} = \text{DC input of CC amp} = 2.5 + 0.7 \text{ V} = 3.2 \text{ V}$$

The DC of the n-channel CD amplifier is then:

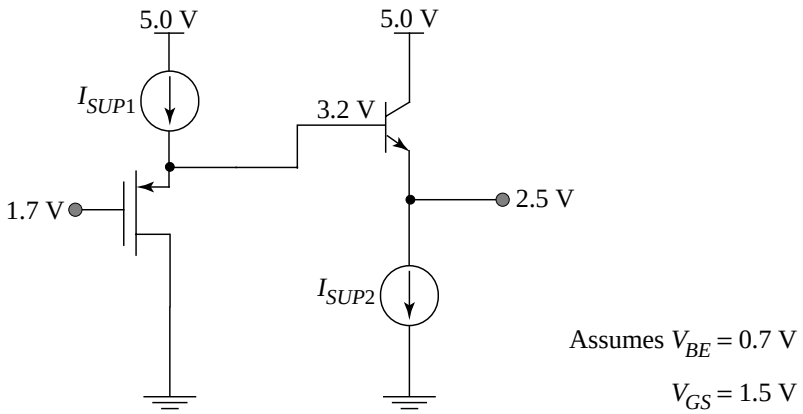
V_{IN} = DC input of CD amp = $V_{IN2} + V_{GS1}$ = 3.2 V + 1.5 V = 4.7 V

where we have assumed that V_{GS1} = 1.5 V as a typical gate-source voltage (actual number comes from $I_{SUP1}$and (W/L)).

- too close to the supply voltage -- input DC level should be centered at near 2.5 V.

DC Biasing Example (Cont.)

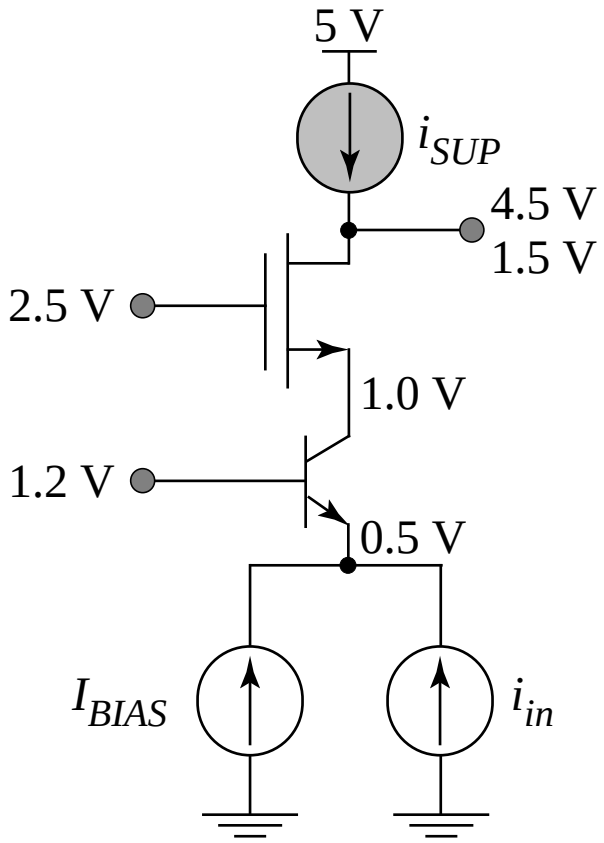
- Solution: use p-channel CD amplifier since it shifts the DC level in the **positive** direction from input to output



Selection of large (*W/L*) for the p-channel --> input DC level can be adjusted closer to 2.5 V.

Sharing a Current Supply: Current Buffer

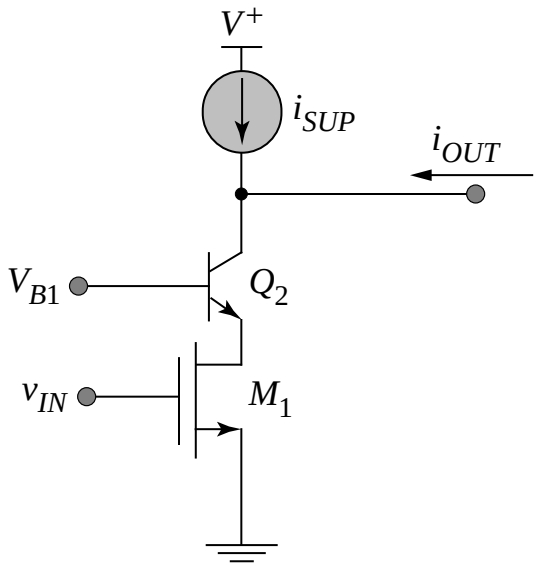
- Example: CB/CG cascade that shares common supply and bias sources



Sharing a Current Supply: the Cascode

- Common-source/common-base two-stage amplifier:

  common-source transistor is used to provide bias current to the common-base transistor



- Similar configurations are also referred to as a “cascode topology:

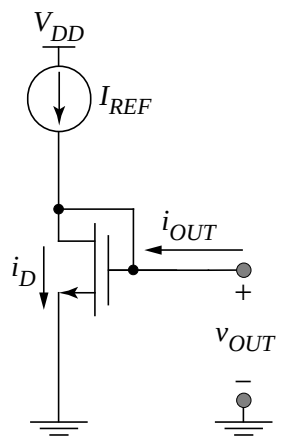
  CE/CB, CE/CG, CS/CB, and CS/CG are also cascodes

DC Voltage and Current Sources

- Output characteristic of a BJT or MOSFET look like a family of current sources ... how do we pick one?

  specify the gate-source *voltage* V_{GS} in order to select the desired current level for a MOSFET (specifiy V_{BE} for a BJT)

  how do we generate a precise voltage? ... we use a current source to set the current in a “diode-connected” MOSFET



(wait a minute ... where do we find I_{REF}? Assume that one is available)

$$i_D = I_{REF} + i_{OUT} = \left(\frac{W}{2L}\right)\mu_n C_{ox}(v_{OUT} - V_{Tn})^2$$

(neglect channel-length modulation term)

DC Voltage Sources (cont.)

- Solving for the output voltage

$$v_{OUT} = V_{Tn} + \sqrt{\frac{I_{REF} + i_{OUT}}{\left(\frac{W}{2L}\right)\mu_n C_{ox}}}$$

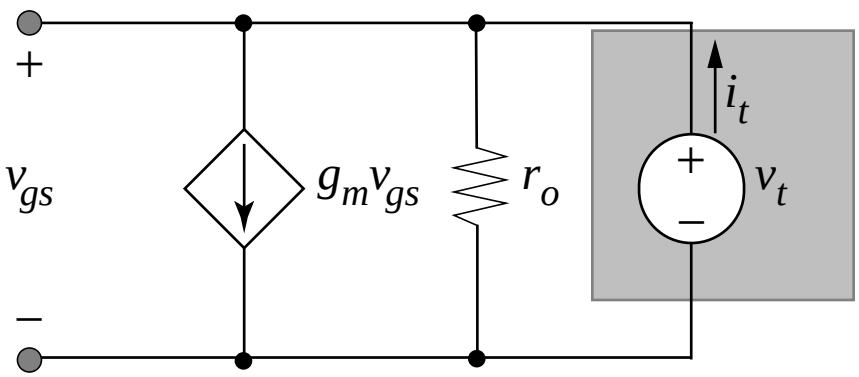
If I_D = 100 μA, μ_n = 50 μAV^{-2}, (W / L) = 20, V_{Tn} = 1 V, then

$$V_{OUT} = 1.45 \text{ V for } I_{OUT} = 0 \text{ A.}$$

- bias current and MOSFET dimensions set the I_{OUT} vs. V_{OUT} characteristic

Source Resistance of Voltage Source

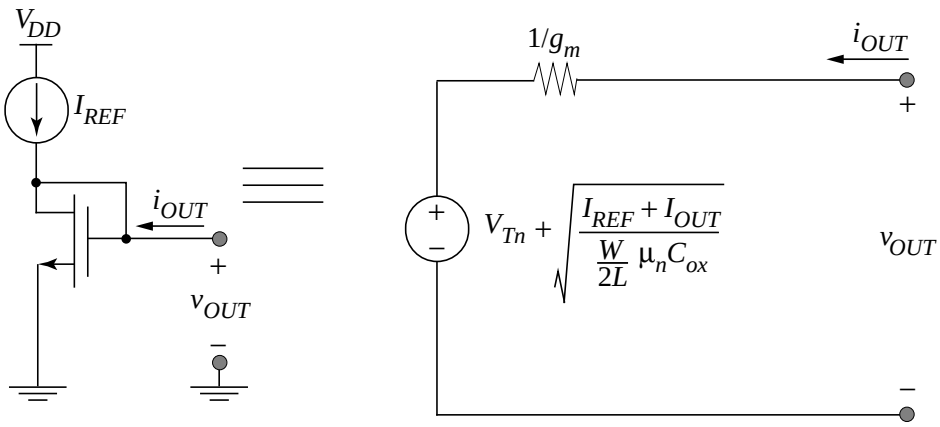
- Small-signal model of MOSFET with drain shorted to gate (“diode-connected”)



transconductance generator degenerates into a conductance
(since v_{gs} is now the voltage drop across it)

- Source resistance of voltage source (assume I_{REF} has r_{oc} --> infinity)

$$R_S = \frac{v_t}{i_t} = \frac{1}{g_m} \Big\| r_o \approx \frac{1}{g_m}$$

Voltage Source Equivalent Circuit (Around I_{OUT} = 0 A)

- Similar to idealized current source equivalent circuit
- Place incremental resistance $1/g_m$ in series with value of voltage source with I_{OUT} = 0 A