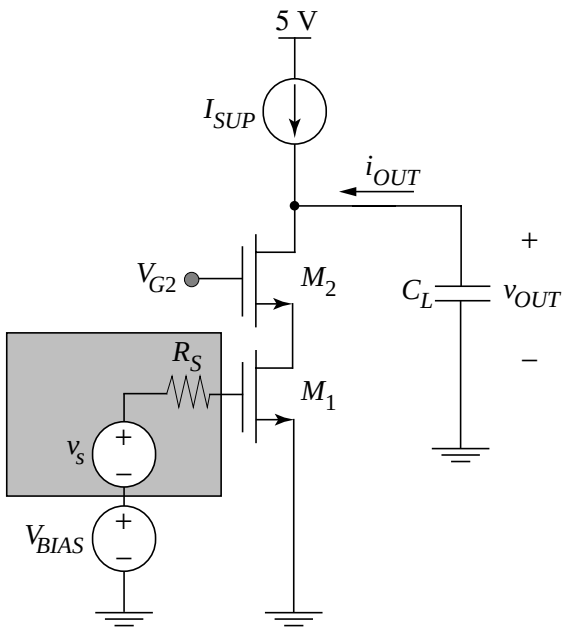
CMOS Cascode Transconductance Amplifier

- Basic topology.



(a)

Device Data

$V_{Tn} = 1$ V $V_{Tp} = -1$ V

$\mu_n C_{ox} = 50\ \mu A/V^2$

$\mu_p C_{ox} = 25\ \mu A/V^2$

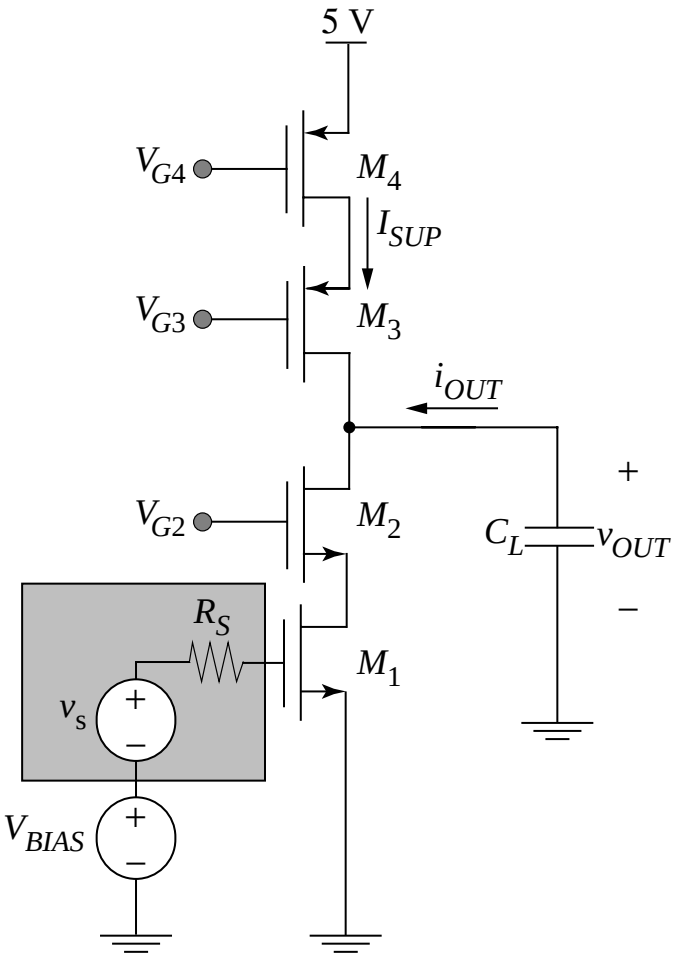
$\lambda_n = 0.05\ V^{-1}$ $\lambda_p = 0.02\ V^{-1}$ @ $L = 2\ \mu m$

(b)

- Current supply must have a very high source resistance r_{oc} since otherwise it will limit the output resistance of the amplifier

Current Supply Topology

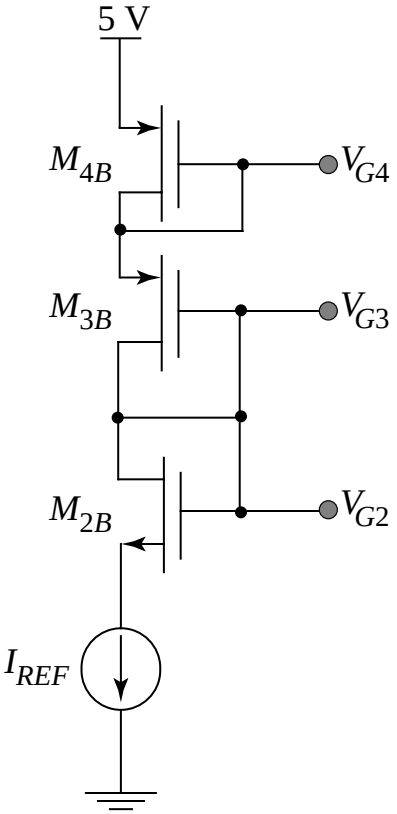
- p-channel cascode current supply is a obvious solution



- need to design a totem pole voltage supply to generate V_{G2}, V_{G3}, and V_{G4}

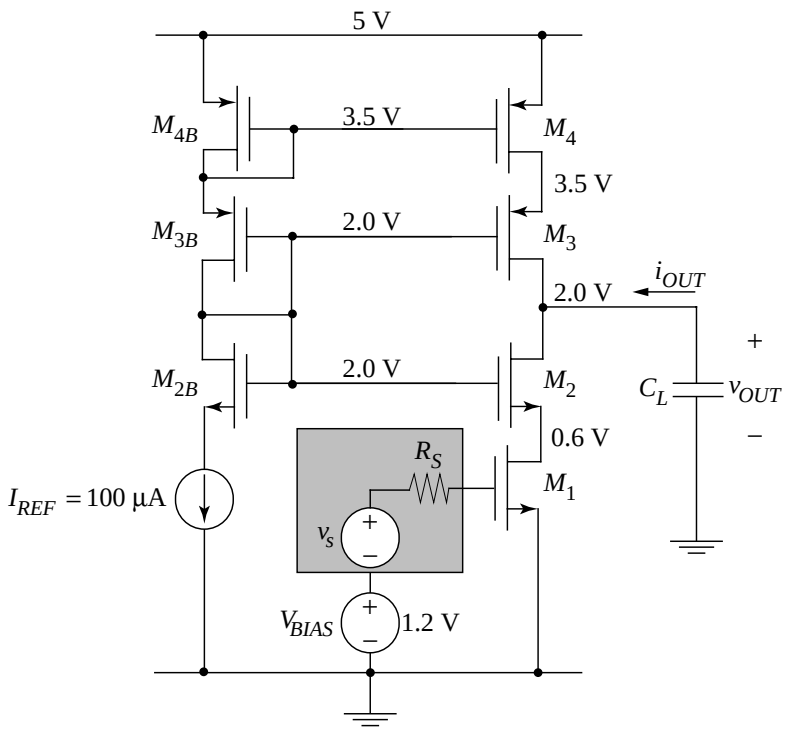
Totem Pole Voltage Reference

- Match device sizes of M_{2B}, M_{3B}, and M_{4B} to M_2, M_3, and M_4



Complete Transconductance Amplifier

- V_{BIAS}: user must supply a *very* precise DC voltage $V_{BIAS} \approx 1.2\ \text{V}$ so that the CS/CGcascode is biased so that it is in the high gain region



$M_1 = 200/2$

$M_2 = M_{2B} = 50/2$

$M_3 = M_{3B} = 64/2$

$M_4 = M_{4B} = 64/2$

- Overall two-port parameters: $G_m = g_{m1}$

  Output resistance: $R_{out} = r_{o2}(1 + g_{m2}\, r_{o1}) \parallel r_{o3}(1 + g_{m3}\, r_{o4})$

- Output swing:

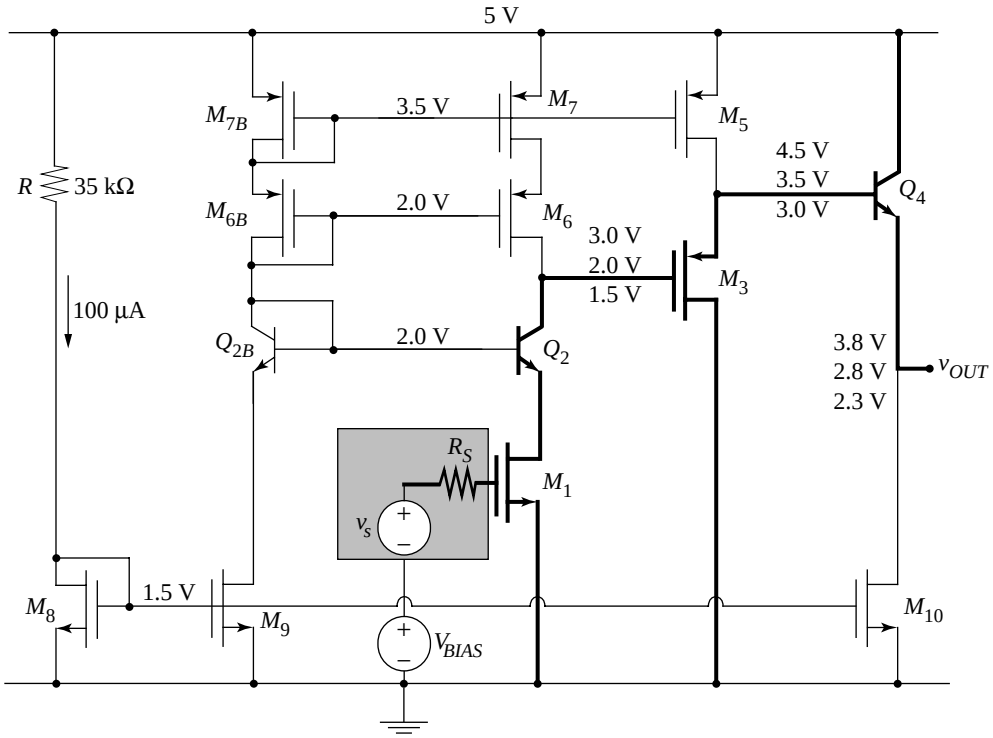
  $V_{OUT(max)} = V_{D4} - V_{SD3(sat)} = V_{DD} - V_{SG4B} - V_{SG3B} + V_{SG3} - V_{SD3(sat)}$

  $V_{OUT(max)} = 5\ \text{V} - 1.5\ \text{V} - 1.5\ \text{V} + 1.5\ \text{V} - 0.5\ \text{V} = 3.0\ \text{V}$

  $V_{OUT(min)} = V_{D1} + V_{DS2(sat)} = V_{G2} - V_{GS2} + V_{DS2(sat)} = 2\ \text{V} - 1.4\ \text{V} + 0.4\ \text{V} = 1\ \text{V}$

Multistage Voltage Amplifier

- Example to understand a complicated circuit



- 10 MOSFETs, 3 BJTs, 1 resistor ... must identify building blocks

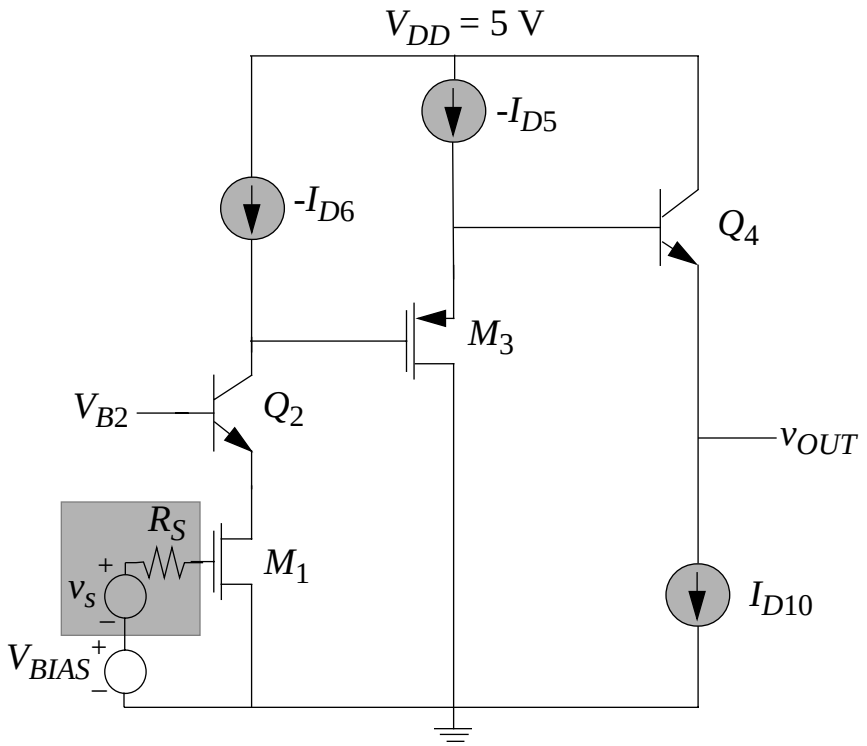
  Step-by-step approach to identifying the “important” transistors --

1. replace all transistor current sources and voltage sources by their symbols -- look for diodes and current mirrors! (M_5, M_6/M_{6B}, M_7/M_{7B}, and M_{10} and Q_{2B} are part of current sources or a totem pole voltage reference.)

2. for the (few) remaining transistors, identify the type and use two-port small-signal models to understand the circuit’s operation. (For the above amplifier, the remaining transistors are M_1, Q_2, M_3, and Q_4.)

Eliminating Current and Voltage Sources

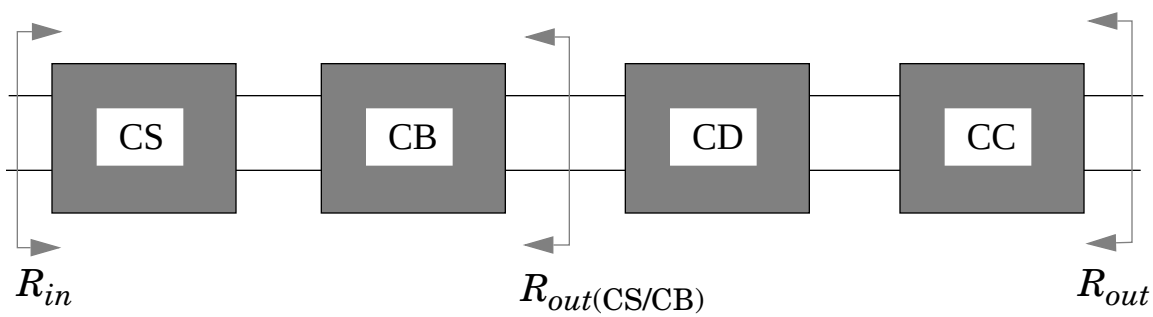
- Replace current and voltage sources with symbols



Identifying Amplifier Stages

- n-channel MOSFET M_1 has its source grounded --> common source
- npn BJT Q_2 has its gate tied to a voltage source (from “totem pole” string of diode-connected transistors) --> common base
- p-channel MOSFET M_3 has its drain connected to ground --> common drain
- npn BJT Q_4 has its collector tied to the positive supply --> common collector

Voltage amplifier is a cascade of two-port models:



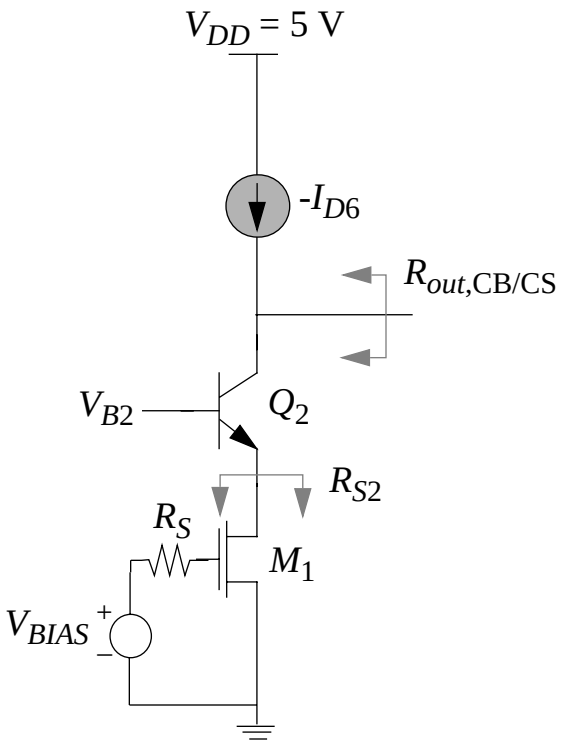
1. common source/common base with cascoded current-source supply: very high output resistance R_{out}(CS/CB) --> can get extremely high output resistance, with a transconductance equal to that of the CS stage

2. common drain: no loading on previous stage since infinite input resistance

3. common collector: low output resistance

Cascode Stage Output Resistance

- Cascode input stage output resistance determines gain



- Output resistance: note that $R_{S2} = r_{o1} >> r_{\pi 2}$

$$R_{out,\mathrm{CB}} = (\beta_{o2} r_{o2}) || r_{oc6} = (\beta_o r_{o2}) || (r_{o6}(1 + g_{m6} r_{o7}))$$

Overall Two-Port Parameters

- Since CC and CD stages have unity gain (approximately), we can quickly estimate the voltage gain by finding v_{in3}/v_{in} where v_{in3} is the input to the CD stage
- Voltage gain:

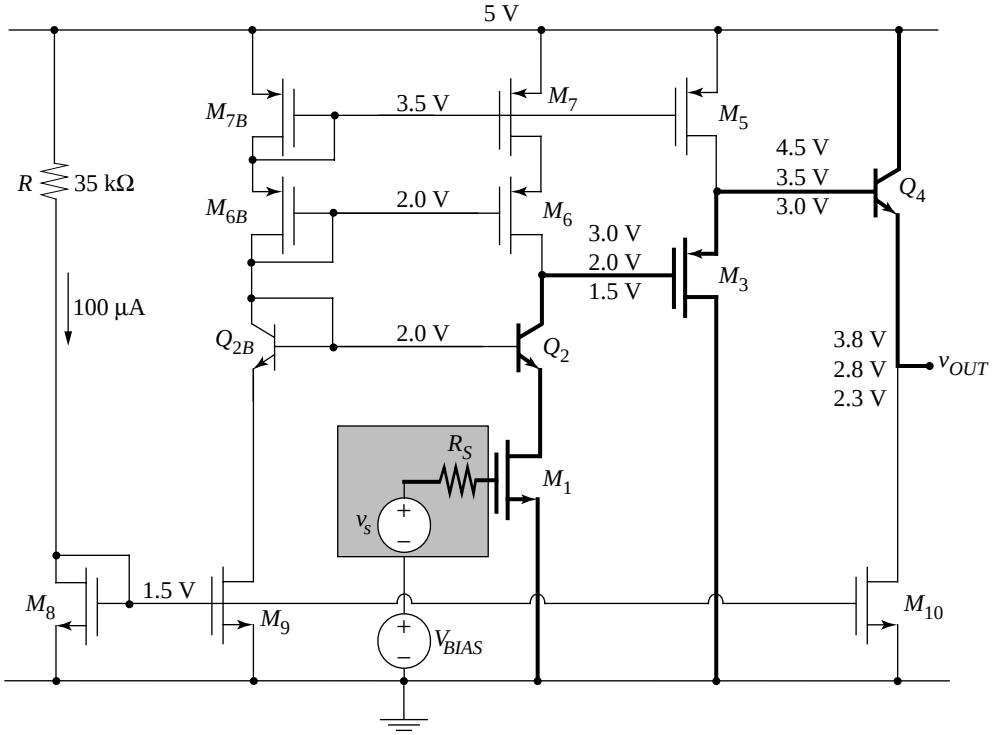
$$A_v \approx (-g_{m1})R_{out,\mathrm{CB}} = -g_{m1}((\beta_o r_{o2})||(r_{o6}(1+g_{m6}r_{o7})))$$

- Output resistance: source resistance of CC output stage is relatively small, since it preceded by a CD stage.

$$R_{out} = R_{out,\mathrm{CC}} \approx \frac{1}{g_{m4}} + \frac{R_{S,\mathrm{CC}}}{\beta_{o4}} = \frac{1}{g_{m4}} + \frac{1}{g_{m3}\beta_{o4}}$$

DC Bias and Output Swing

- Assuming all n-channel devices have V_{GS} = 1.5 V and p-channel devices have V_{SG} = 1.5 V, we can find all the node voltages ... we also assume that V_{BIAS} has been adjusted such that the circuit is in the high-gain region



- Output swing: must consider more than output stage to find limits to V_{OUT}

Frequency Response

- Before starting, review phasor analysis, Bode plots ...

  Key concept: small-signal models for amplifiers are *linear* and therefore, cosines and sines are solutions of the linear differential equations which arise from *R*, *C*, and controlled source (e.g., G_m) networks.

  It is much more efficient to work with *imaginary exponentials* rather than cosine and sine functions; the measured function *v(t)* is considered (by convention) to be the real part of this imaginary exponential

$$v(t) = v\cos(\omega t + \phi) \rightarrow \mathrm{Re}(ve^{(j\omega t + \phi)}) = \mathrm{Re}(ve^{j\phi}e^{j\omega t})$$

where v is the amplitude and ϕ is the phase of the sinusoidal signal *v(t)*.

The ***phasor V*** is defined as the complex number

$$\boxed{V = ve^{j\phi}}$$

Therefore, the measured function is related to the phasor by

$$\boxed{v(t) = \mathrm{Re}(Ve^{j\omega t})}$$

Circuit Analysis with Phasors

- The current through a capacitor is proportional to the derivative of the voltage:

$$i(t) = C\frac{d}{dt}v(t)$$

We assume that all signals in the circuit are represented by sinusoids. Substitution of the phasor expression for voltage leads to:

$$v(t) \rightarrow Ve^{j\omega t} \qquad \ldots \qquad Ie^{j\omega t} = C\frac{d}{dt}(Ve^{j\omega t}) = j\omega CVe^{j\omega t}$$

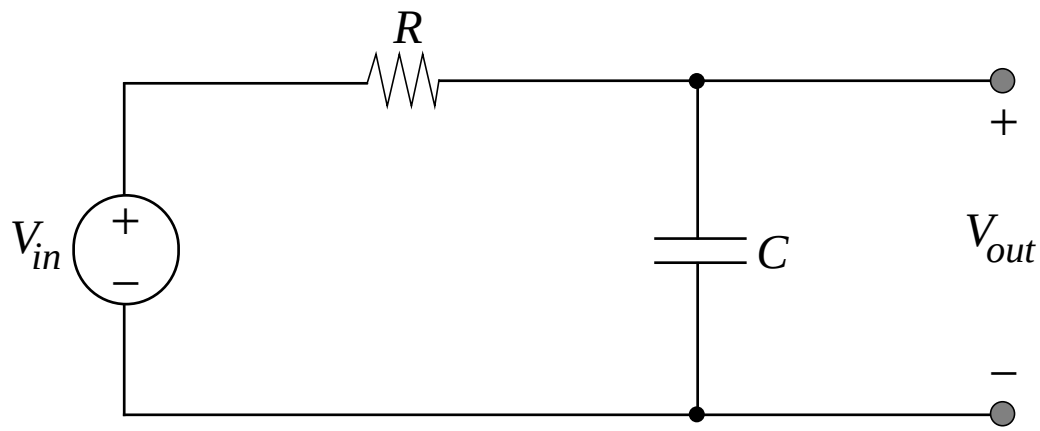
which implies that the ratio of the phasor voltage to the phasor current through a capacitor (the ***impedance***) is

$$\boxed{Z(j\omega) = \frac{V}{I} = \frac{1}{j\omega C}}$$

- Implication: the phasor current is *linearly proportional* to the phasor voltage, making it possible to solve circuits involving capacitors and inductors as rapidly as resistive networks ... as long as all signals are sinusoidal.

Phasor Analysis of the Low-Pass Filter

- Voltage divider with impedances --



Replacing the capacitor by its impedance, 1 / ($j\omega C$), we can solve for the ratio of the phasors V_{out} / V_{in}

$$\frac{V_{out}}{V_{in}} = \frac{1/j\omega C}{R + 1/j\omega C}$$

multiplying by $j\omega C/j\omega C$ leads to

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega RC}$$