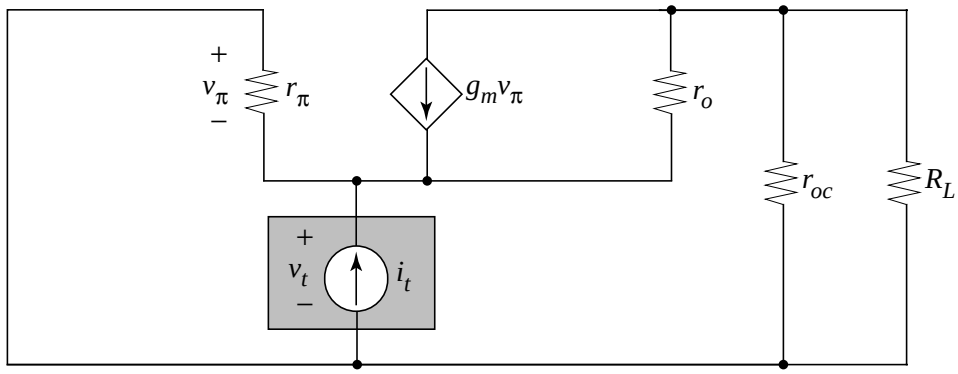
Common-Base Input Resistance R_{in}

- Apply test current, with load resistor R_L present at the output

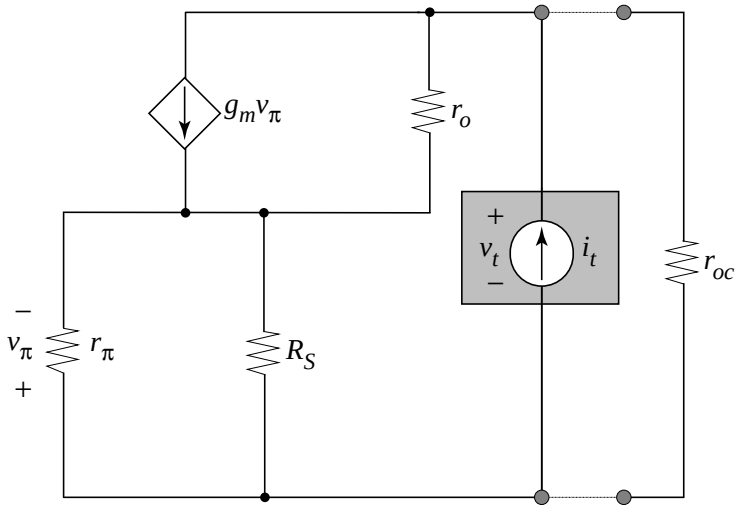


The transconductance generator dominates the sum of the currents at the input node since $g_m >> r_o^{-1}$ and $g_m >> r_\pi^{-1}$ and

$$R_{in} \approx \frac{1}{g_m}$$

Common-Base Output Resistance R_{out}

- Test circuit: leave source resistance of input current in place; remove r_{oc} for analysis and place it in parallel ...



- Complicated analysis (see Section 8.8), with the final result boiling down to:

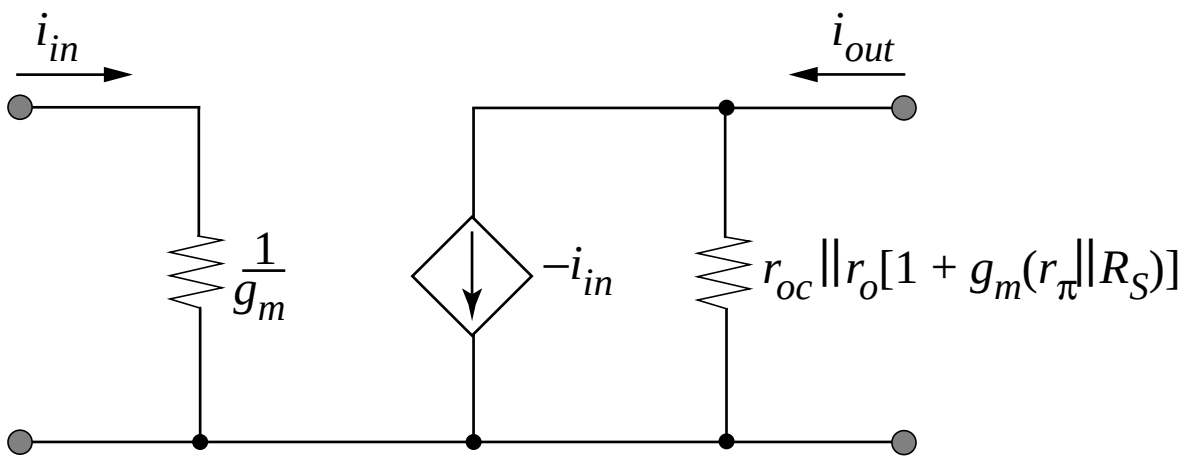
$$\boxed{R_{out} \approx r_{oc} || [r_o(1 + g_m(r_\pi || R_S))]}$$

If the R_S is much greater than r_π, then the output resistance is approximately:

$$\boxed{R_{out} \approx r_{oc} || [\beta r_o]}$$

Common-Base Two-Port Model

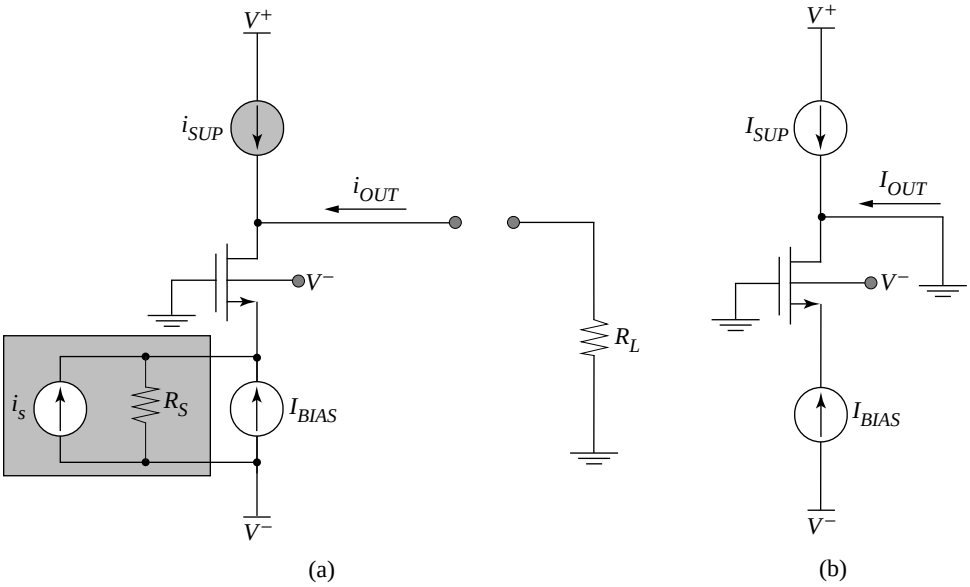
- Note that the output resistance depends on the source resistance -- which means that the CB current buffer is *not* unilateral and the two-port formal model is not strictly valid. However, the error in using the model is small (see Appendix A8.1).



- Controlled source can be flipped to make current gain + 1.

Common-Gate Amplifier

- Circuit configuration: analogous to common-base

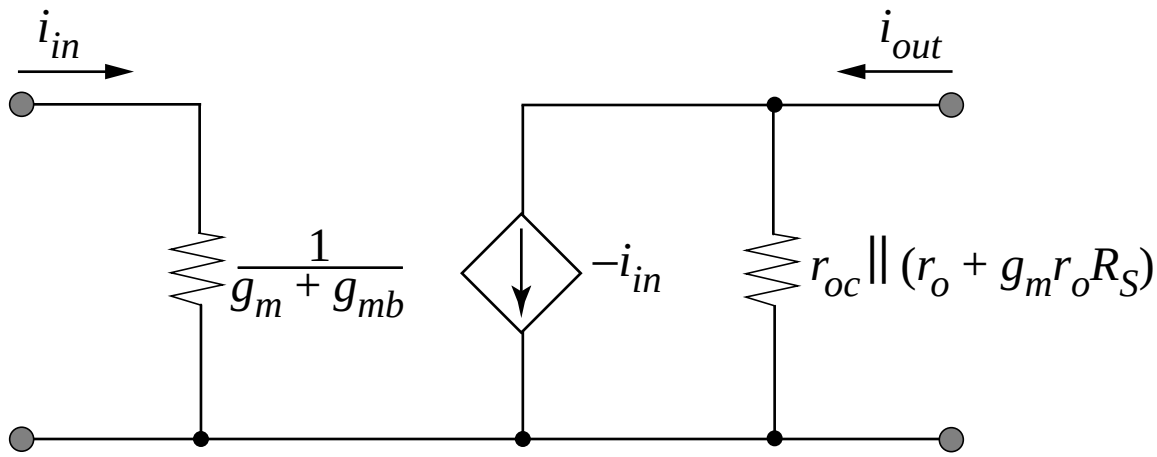


The backgate can be tied to the source if the device is in a well.

It is obvious that the current gain for this amplifier must be unity, since the gate current for a MOSFET is zero

Common-Gate Two-Port Model

- The resulting two port model is:



The input resistance is the same as for the CB for the case where source and backgate are shorted. When this isn't the case, the backgate generator is added in:

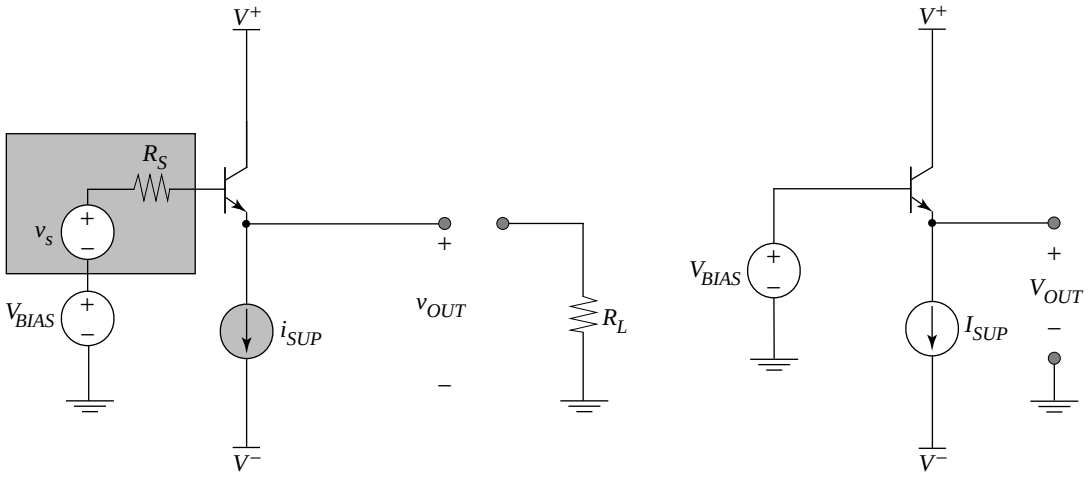
$$R_{in} = \frac{1}{g_m} \qquad \text{or} \qquad R_{in} = \frac{1}{g_m + g_{mb}}$$

- The output resistance is similar to the CB result with r_π --> infinity

$$R_{out} = r_{oc} || r_o[1 + g_m R_S]$$

Common-Collector Amplifier

- Circuit configuration

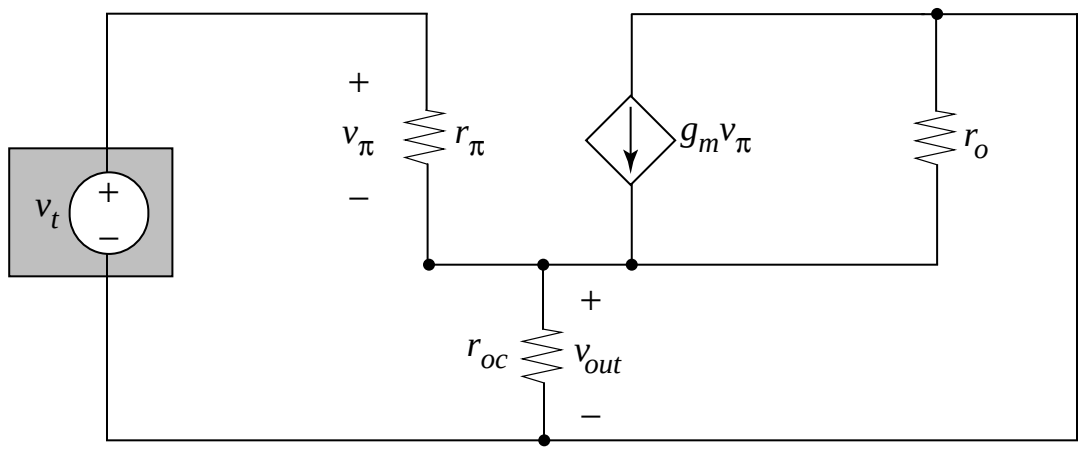


- Biasing: if transistor is “on” (i.e., not cutoff), then

$$V_{BIAS} - V_{OUT} = 0.7 \text{ V}$$

Common-Collector as a Small-Signal Amplifier

- Linear relationship between output voltage and total input voltage indicates that the CC amplifier is a *voltage buffer* -- the voltage gain is about equal to 1.
- Small-signal model and procedure for finding A_v for two-port model:



- Circuit analysis: current through $r_{oc} \parallel r_o$ is $v_\pi / r_\pi + g_m r_\pi$ -->

$$\frac{v_t - v_{out}}{r_\pi} + g_m(v_t - v_{out}) = \frac{v_{out}}{r_{oc}||r_o}$$

multiplying by r_π and recognizing that $g_m r_\pi = \beta_o$,

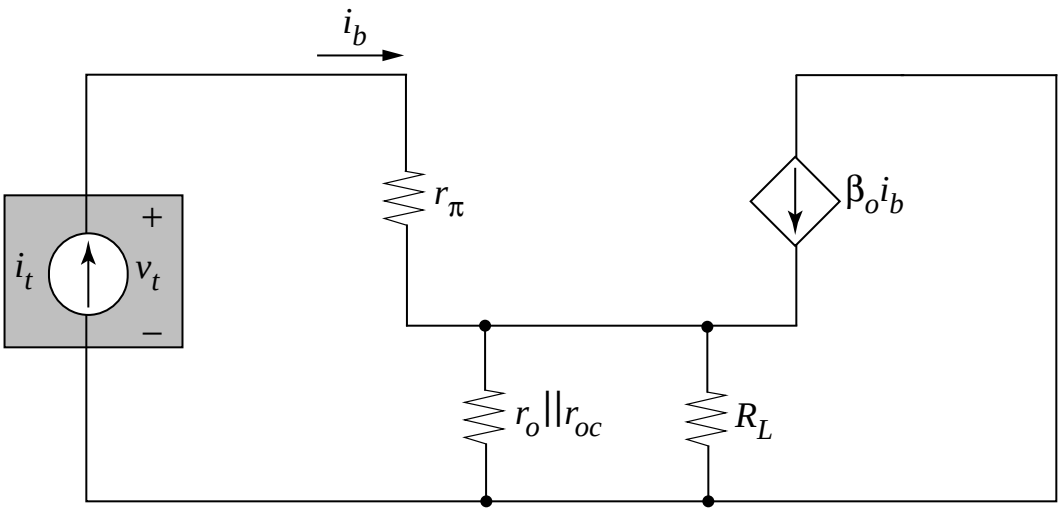
$$v_t - v_{out} + \beta_o(v_t - v_{out}) = (1 + \beta_o)(v_t - v_{out}) = \frac{v_{out} r_\pi}{r_{oc}||r_o}$$

solving for the open-circuit voltage gain:

$$\boxed{A_v = \frac{1}{1 + \dfrac{r_\pi}{r_{oc}||r_o(\beta_o + 1)}} \approx 1}$$

Common-Collector Input Resistance R_{in}

- Procedure: apply pure test source, leave load resistor R_L in
  -- *very important for CC amplifier*



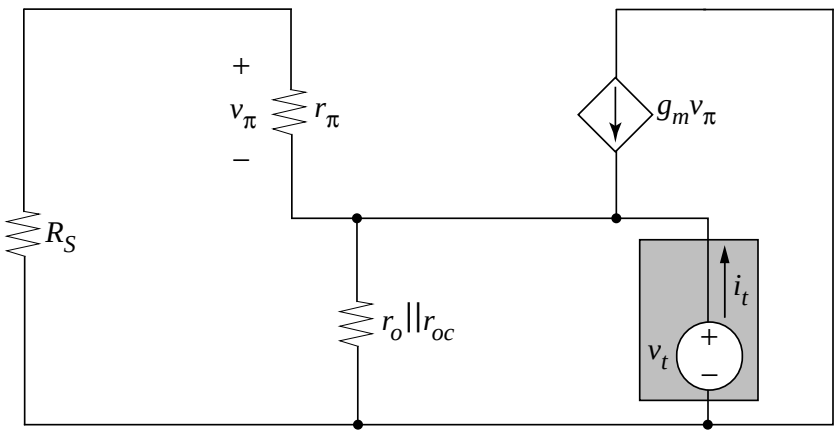
note that current through $r_{oc} \parallel r_o \parallel R_L$ is $i_t + \beta_o\, i_t$ -->

$$R_{in} = r_\pi + (\beta_o + 1)(r_{oc} || r_o || R_L)$$

- When the load resistor is much smaller than the output resistance of the transistor and the current source resistance, then the input resistance of the CC amplifier is approximately $R_{in} = r_\pi + (\beta_o + 1)R_L$

Common Collector Output Resistance

- Apply test current source at the output, leaving any source resistance R_S attached at the input.

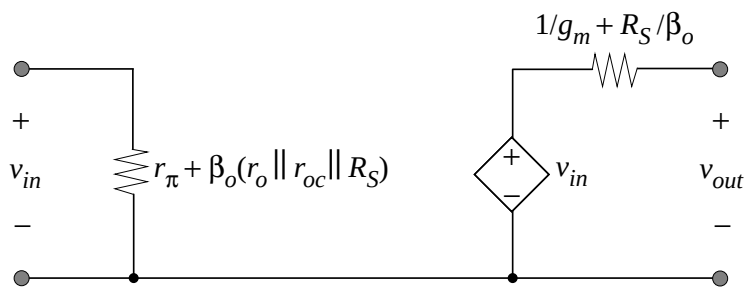


KCL at the common node + algebra -->

$$R_{out} = \frac{1}{g_m} + \frac{R_S}{\beta_o}$$

Common Collector Two-Port Model

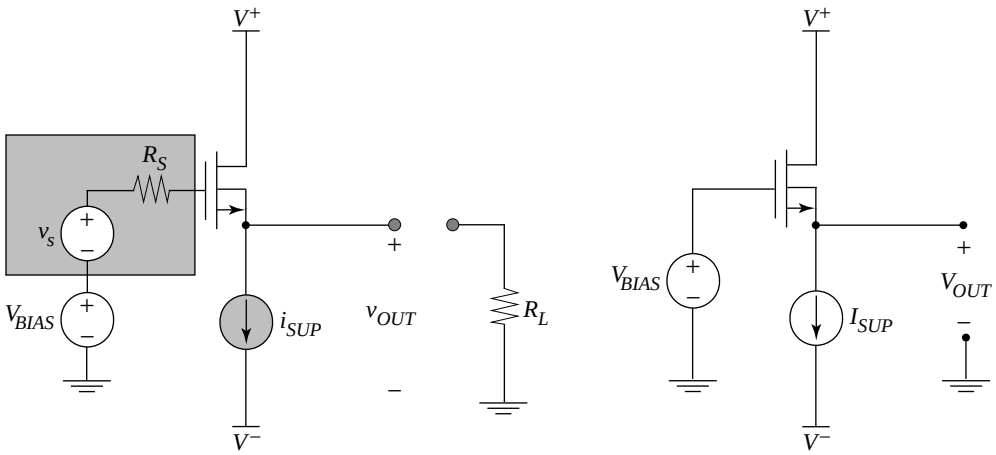
- Final result: pretty good voltage buffer:



Note: this model is approximate and can give erroneous results for extremely low values of R_L. However, it is very convenient for hand analysis.

Common-Drain Amplifier

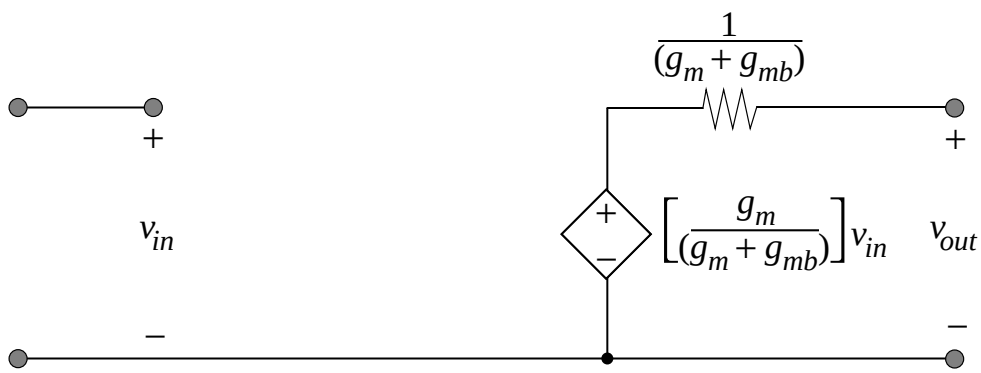
- Similar configuration to common collector.



Analysis: much the same as for CC amplifier -- if V_{SB} isn't zero, then the voltage gain is degraded from about 1 to 0.8-0.9

Common-Drain Two-Port Model

- Two-Port model:

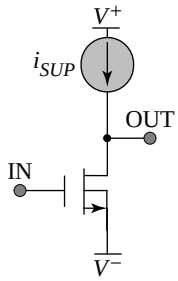
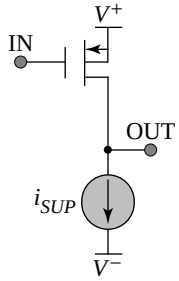
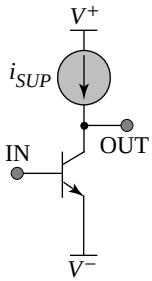
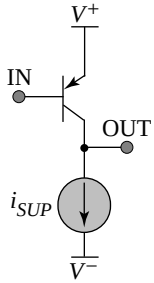
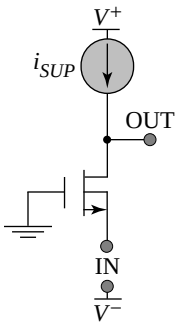
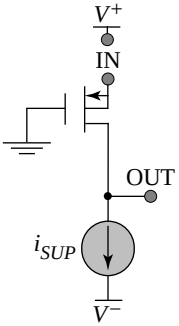
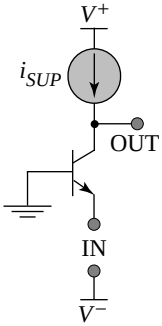
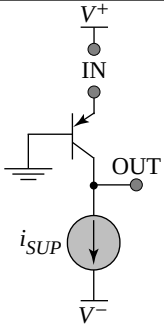
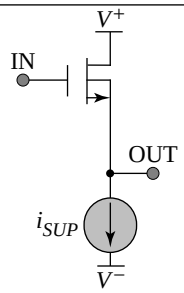
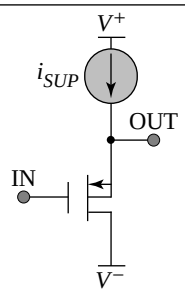
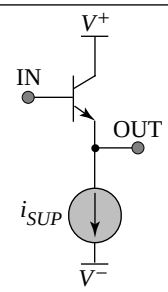
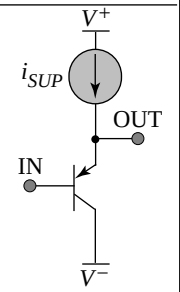


If $V_{SB} = 0$, then the input resistance is $A_v = 1$ and $R_{out} = 1 / g_m$ (for hand analysis)

The CD amplifier is a reasonable voltage buffer, especially for large (W / L) --> large g_m.

Single-Stage Amplifier Configurations

- Two complemetary versions exist for each amplifier type.
- CS/CE, CG/CB, and CD/CC have similar topologies (and properties)

Amplifier Type	**Transistor Type**			
	NMOS	PMOS	npn	pnp
Common Source/ Common Emitter (*CS*/*CE*)				
Common Gate/ Common Base (*CG*/*CB*)				
Common Drain/ Common Collector (*CD*/*CC*)				

Two-Port Parameters for Single-Stage Amplifiers

Amplifier Type	Controlled Source	Input Resistance R_{in}	Output Resistance R_{out}
Common Emitter	$G_m = g_m$	r_π	$r_o \parallel r_{oc}$
Common Emitter $+R_E$	$G_m = g_m / (1+g_m R_E)$	$r_\pi (1 + g_m R_E)$	$r_{oc} \parallel [(1 + g_m R_E) r_o]$ for $r_\pi >> R_E, R_S$
Common Source	$G_m = g_m$	infinity	$r_o \parallel r_{oc}$
Common Base	$A_i = -1$	$1 / g_m$	$r_{oc} \parallel [(1 + g_m(r_\pi \parallel R_S))\, r_o]$, for $g_m R_S >> 1$
Common Gate	$A_i = -1$	$1 / g_m$, $(v_{sb} = 0)$ -otherwise- $1 / (g_m + g_{mb})$	$r_{oc} \parallel [(1 + g_m R_S) r_o]$, $(v_{sb}=0)$ -otherwise- $r_{oc} \parallel [(1+ (g_m + g_{mb}) R_S)\, r_o]$ both for $g_m R_S >> 1$
Common Collector	$A_v = 1$	$r_\pi + \beta_o (r_o \parallel r_{oc} \parallel R_L)$	$(1 / g_m) + R_S / \beta_o$
Common Drain	$A_v = 1$ if $v_{sb} = 0$, -otherwise- $g_m / (g_m + g_{mb})$	infinity	$1 / g_m$ if $v_{sb} = 0$, -otherwise- $1 / (g_m + g_{mb})$

Note: appropriate two-port model is used, depending on controlled source

Ultra-Simplified Two-Port Parameters

- $g_{mb} = 0$, common base has reasonable source resistance --> $R_S >> r_\pi$

Amplifier Type	Controlled Source	Input Resistance R_i	Output Resistance R_o
Common Emitter	$G_m = g_m$	r_π	$r_o \parallel r_{oc}$
Common Source	$G_m = g_m$	infinity	$r_o \parallel r_{oc}$
Common Base	$A_i = -1$	$1 / g_m$	$r_{oc} \parallel (\beta\, r_o)$
Common Gate	$A_i = -1$	$1 / g_m$	$r_{oc} \parallel [(1+g_m R_S)\, r_o]$
Common Collector	$A_v = 1$	$r_\pi + \beta\, (r_o \parallel r_{oc} \parallel R_L)$	$(1 / g_m) + R_S / \beta$
Common Drain	$A_v = 1$	infinity	$1 / g_m$

- this table is adequate for first-cut hand design