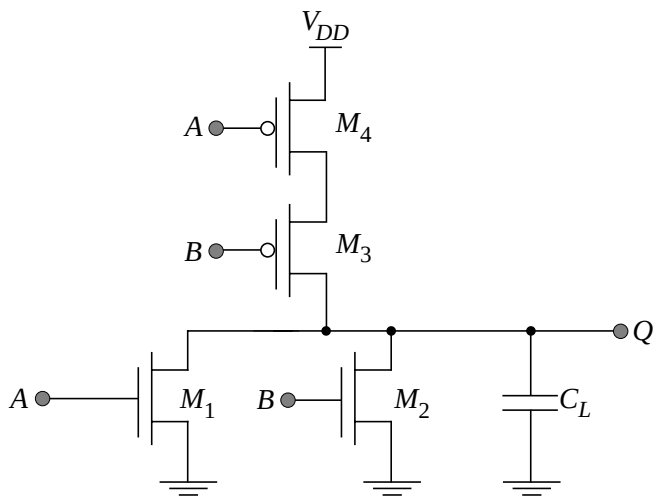
CMOS Dynamic Logic

- Static NOR gate



Idea: n-channel and p-channel devices separately perform the same logic function.

replace p-channels with a resistor -->

$$Q = \overline{A + B}$$

replace n-channels with a resistor -->

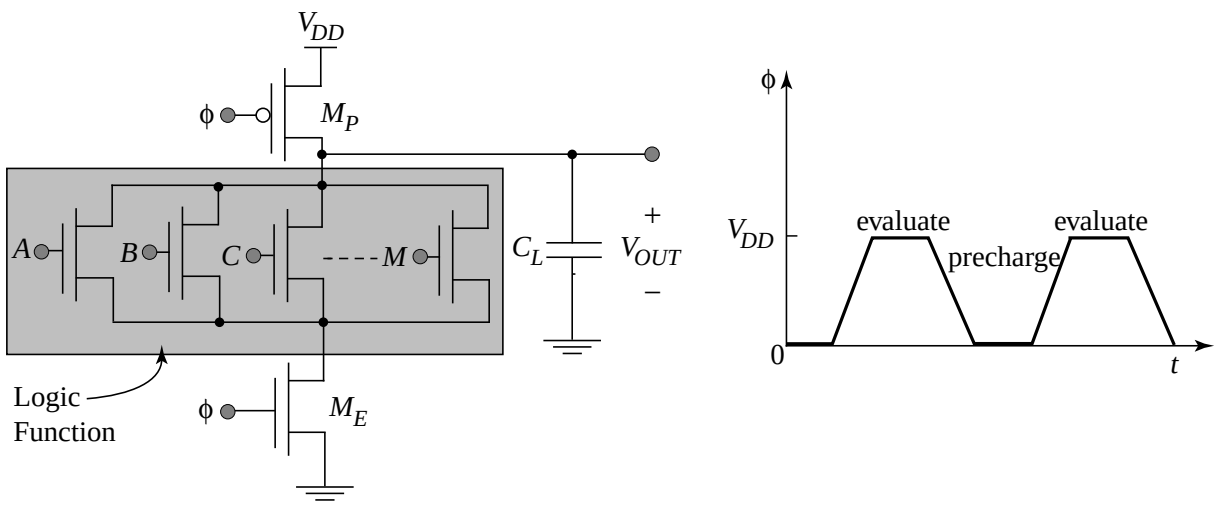
$$Q = \overline{A}\,\overline{B}$$

... two functions are identical by DeMorgan's Theorem

- Let n-channels perform the logic and get rid of the pull-up devices (or vice versa)

n-Channel CMOS Dynamic Logic

- clock signal $\phi(t)$ charges up load capacitance through M_P (P = *precharge)* when it transitions from high to low; M_E (E = evaluate) is cutoff and prevents any discharge path of C_L through logic function transistors.
- clock signal goes high --> M_P is cutoff, M_E conducts --> C_L discharges if one of the logic transistors has a high input.



(a) (b)

- Payoffs:

  1. large fan-in NOR gates without huge p-channel load devices (also, avoids backgate effect on loads)

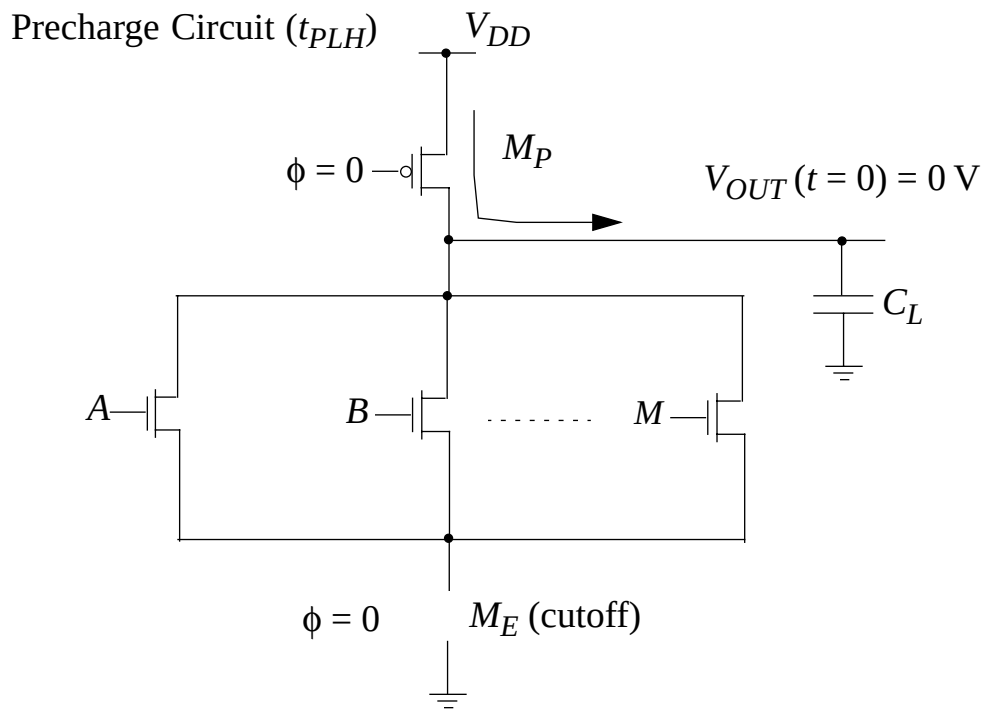
  2. tends to be fast due to smaller load capacitances

- Drawback:

  1. clock is essential to refresh logic level stored on C_L, which complicates the design

n-Channel Dynamic Logic Propagation Delays

- Consider "t_{PLH}" to be the time required to pre-charge the output node

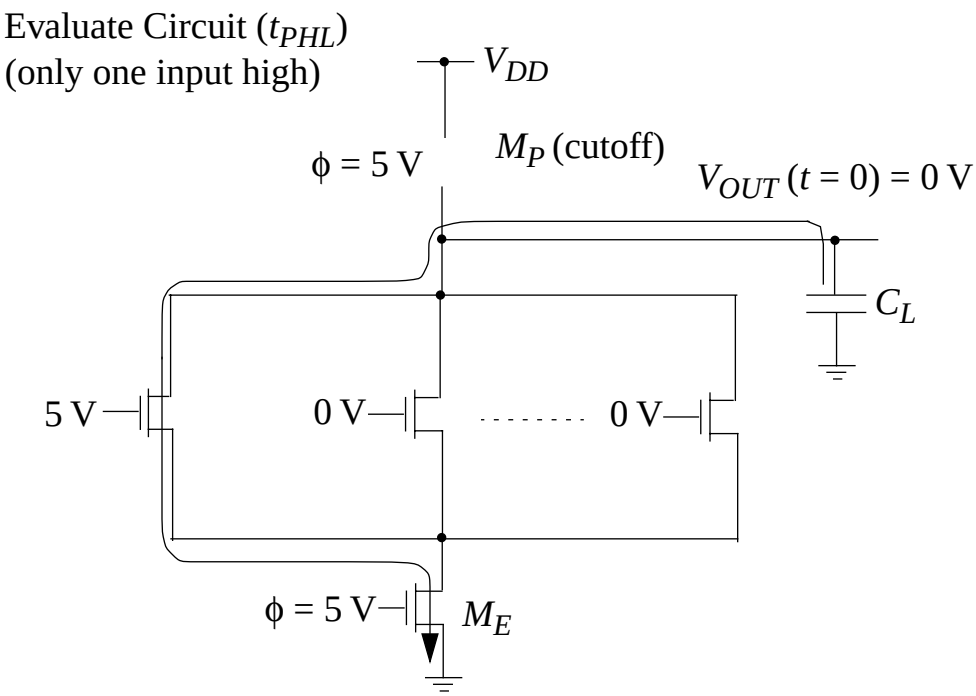


- Charging current

$$-I_{Dp} = \frac{k_p}{2}(V_{DD} + V_{Tp})^2$$

n-Channel Dynamic Logic Propagation Delays

- Consider "t_{PHL}" to be the *worst-case* time to evaluate the logical function after clock goes high.

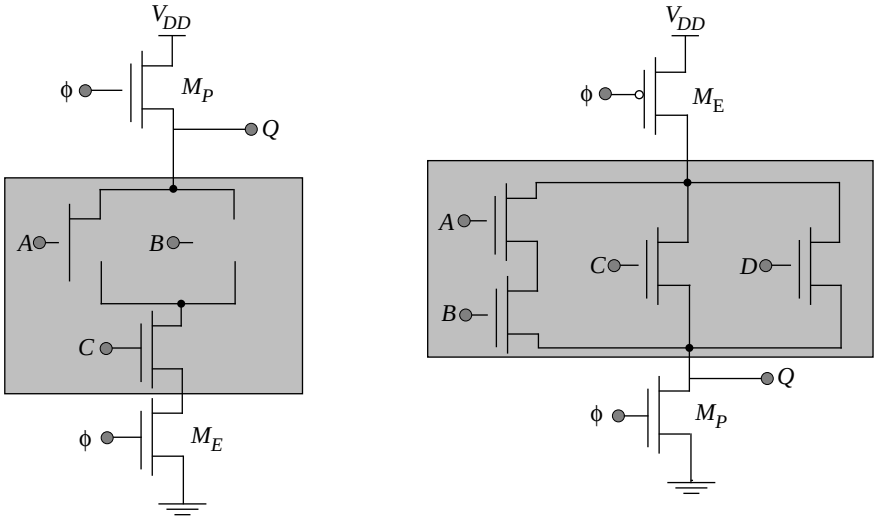


- Discharging current: assume $(W/L)_E = (W/L)_A = \ldots (W/L)_M$ and note that the transistors are in series -->effective value is k_n / 2

$$I_{D_n} = \mu_n C_{ox}\left(\frac{k_n}{4}\right)(V_{DD} - V_{Tn})^2$$

Boolean Functions in Dynamic Logic

- Examples:



(a) (b)

- (a) n-channel dynamic logic

$$Q = \overline{(A + B)C}$$

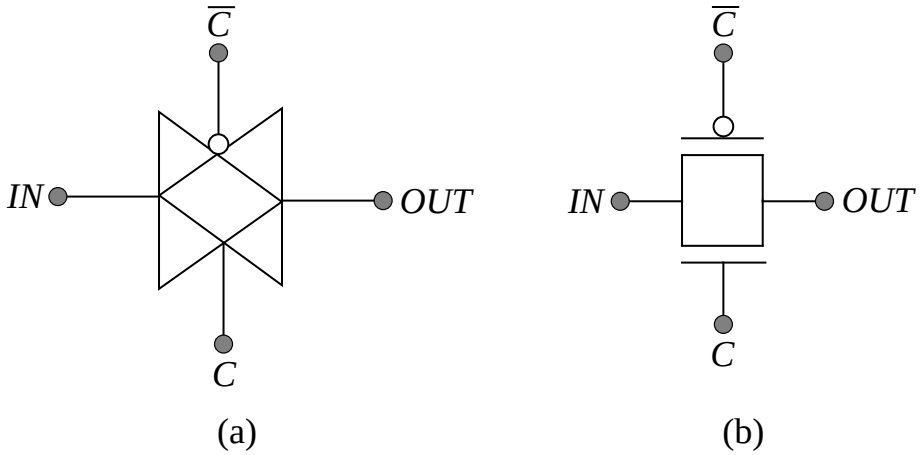
- (b) p-channel dynamic logic

  The output is "pre-discharged" to zero by M_P and is only charged if there is a path through the logic transistors when the clock goes low and M_E conducts.

$$Q = \overline{A}\,\overline{B} + \overline{C} + \overline{D}$$

CMOS Transmission Gates

- Need: “gate” signals by having a series switch that can be shorted or open-circuited.



- Why n-channel and p-channel in parallel? Only one device (say, n-channel): can’t pass an input voltage > V_{DD} - V_{Tn}, since device will enter the cutoff region

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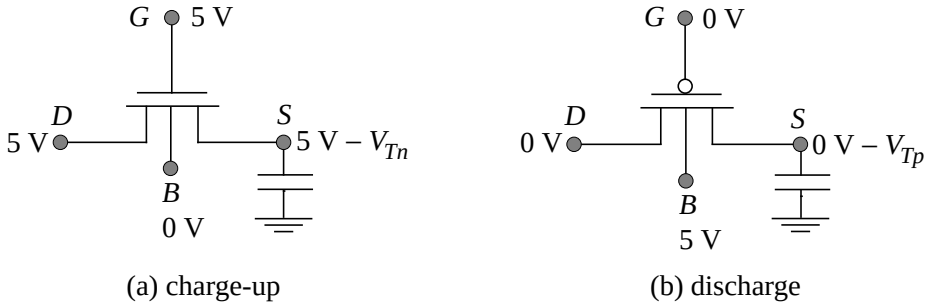
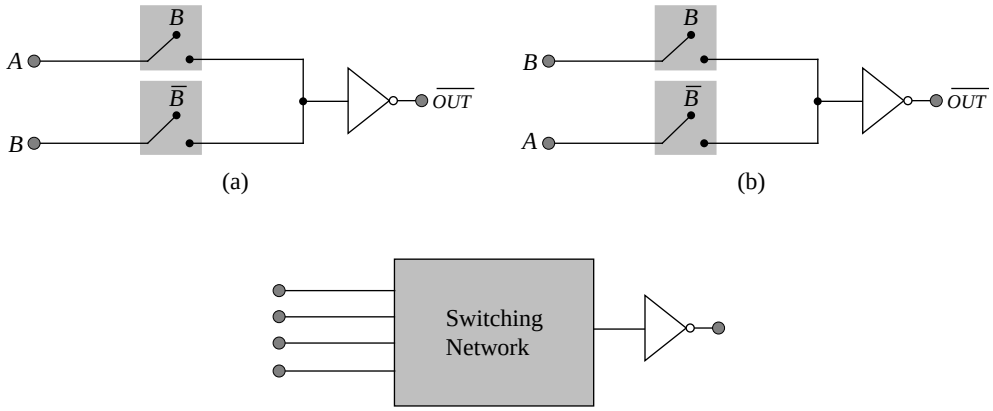


Pass Transistor Logic

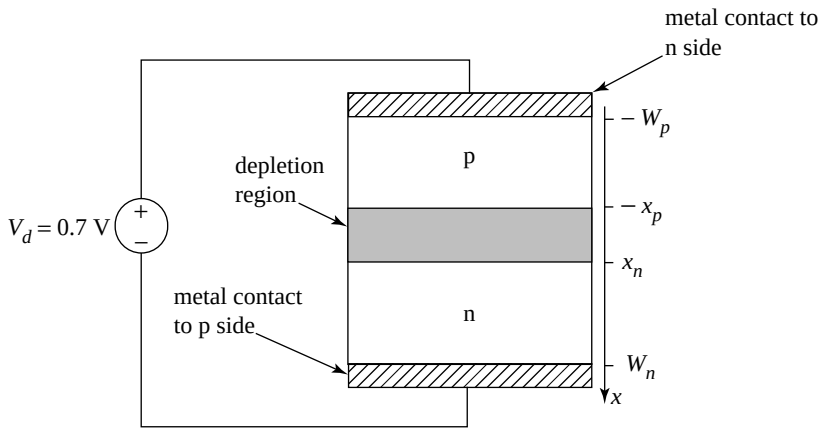
- Advantages: reduced transistor count and higher speed compared with static CMOS
- Disadvantage: reduced noise margins



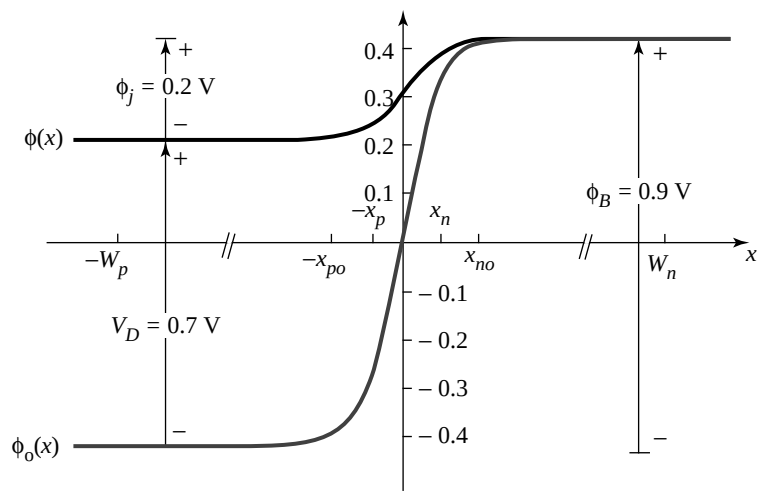
The pn Junction under Forward Bias

- $V_D > 0$ --> what happens?

  Many assumptions: from Chapter 6 (current not too big) --> resistive potential drops in bulk p & n regions can be neglected in KVL and $\phi_j = \phi_B - V_D$



(a)



(b)

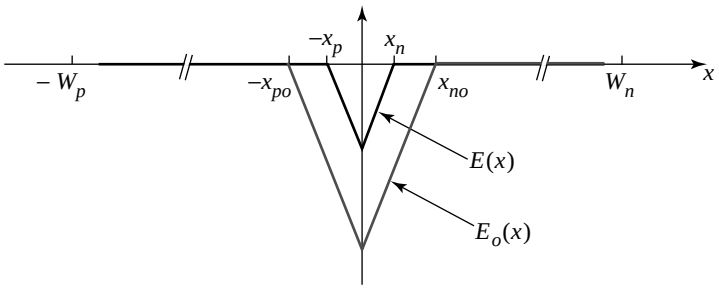
ϕ_B = thermal equilibrium barrier height = $\phi_n - \phi_p$

Physical Reasoning

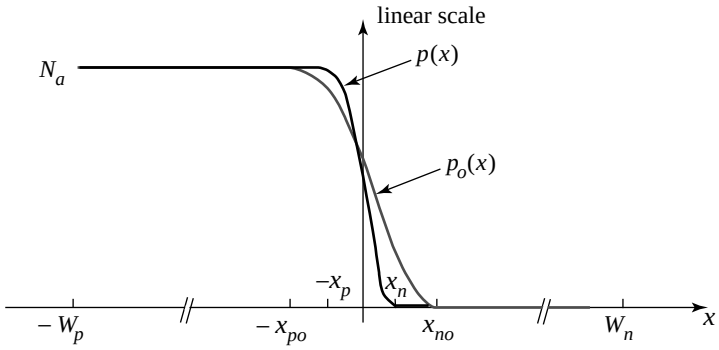
- thermal equilibrium --> balance between drift and diffusion:

  $J = J^{drift} + J^{diff} = 0$ for holes and electrons

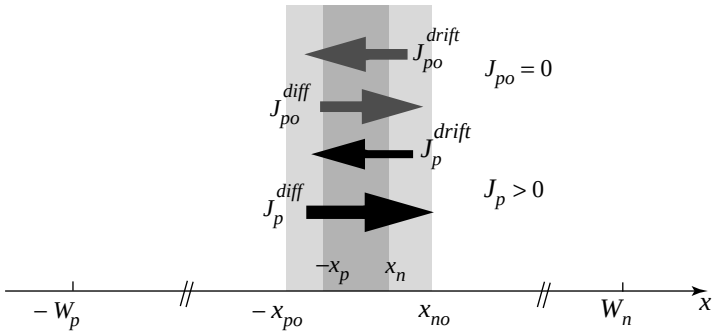
- forward bias upsets balance



(a)



(b)



(c)

Modelling Forward-Bias Diode Currents

- **Step 1**: find how minority carrier concentrations at the edges of depletion region change with forward bias V_D

- **Step 2**: what happens to the minority carrier concentration at the ohmic contacts under forward bias? *Answer*: no change from equilibrium.

- **Step 3**: find the minority carrier concentrations $n_p(x)$ in the p region and $p_n(x)$ in the n region.

- **Step 4**: find the minority carrier diffusion currents.

- **Step 5**: find the total current J.

Carrier Concentrations in Thermal Equilibrium at the pn Junction

- For the junction in thermal equilibrium,

$$\phi_B = \frac{kT}{q} ln(\frac{N_a N_d}{n_i^2}), \text{ where}$$

If we identify $p_{no} = n_i^2 / N_d$ and $n_{po} = n_i^2 / N_a$, we can reexpress this basic result in two ways --

$$\phi_B = V_{th} ln(\frac{N_d}{n_{po}}) \qquad \text{and} \qquad \phi_B = V_{th} ln(\frac{N_a}{p_{no}}).$$

- Solving for the equilibrium minority carrier concentrations in terms of the built-in potential,

$$p_{no} = N_a e^{-\phi_B/(V_{th})} \qquad \text{and} \qquad n_{po} = N_d e^{-\phi_B/(V_{th})} \quad .$$

This result is very important, since it relates the minority carrier concentration on one side of the junction to the majority carrier concentration on the *other side* of the junction ... !

Law of the Junction

- What happens under an applied bias?

  assume that the new potential barrier $\phi_j = \phi_B - V_D$ can substituted for the thermal equilibrium barrier to find the new minority carrier concentrations *at the depletion region edges* $-x_p$ (p-side) and x_n (n-side)

$$n_p(-x_p) = N_d e^{-\phi_j/V_{th}} = N_d e^{-(\phi_B - V_D)/V_{th}} \text{ and}$$

$$p_n(x_n) = N_a e^{-\phi_j/V_{th}} = N_a e^{-(\phi_B - V_D)/V_{th}}.$$

These results can be re-expressed in a simpler form, by expanding the exponentials:

$$\boxed{\begin{aligned} n_p(-x_p) &= N_d e^{-\phi_B/V_{th}} e^{V_D/V_{th}} = n_{po} e^{V_D/V_{th}} \\ p_n(x_n) &= N_a e^{-\phi_B/V_{th}} e^{V_D/V_{th}} = p_{no} e^{V_D/V_{th}} \end{aligned}}$$

- These two equations are known as the **Law of the Junction**.

  Note that the minority carrier concentration is an exponential function of the applied bias on the junction.