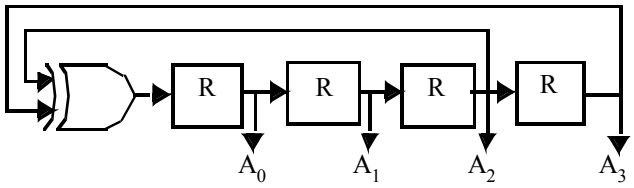
Chapter 7

Design Project:
A superfast random number generator

The goal of this project is to design a 4-bit random number generator, to be used for test pattern generation. The random number generator uses the Linear Feedback Shift Register approach.

The block diagram of the generator is shown in FIG. 1.



Pseudo-Random number generator.

The goal of the project is **SPEED, SPEED (!!!!)** and nothing else. This means that you should minimize the clock period to the maximal extent. Area and power are not in issue in this design project.

1. Implementation and Constraints

The project is to be **done in pairs**.
You are free to choose any CMOS implementation style for the design, including but not limited to: complementary CMOS, ratioed logic, DCVSL, pass-transistor logic, CPL, and dynamic logic. Feel free to mix the logic families in your design. All complimentary signals must be internally generated, and any number of levels of logic may be used. Registers can be dynamic or static.

You are free to use the clocking strategy of your choice (single phase, two phase, four phase, ...). **Make sure, however, that races do not occur.**

TECHNOLOGY: The design is to be implemented in a 0.25 μm CMOS process with 4 metal layers. The SPICE technology is in the g25.mod file.
POWER SUPPLY: A power supply of 2.5 **V** should be used.

PERFORMANCE METRIC: V_{OH}, V_{OL}: The output signals should settle to within 10% of their final value before the next clock event can be introduced!!!

NOISE MARGINS: The noise margins should be at least 10% of the voltage swing.

LOAD CAPACITANCE: Each output bit of the generator should have a **20 fF** load.

CLOCKS: You are given a primary clock signal with a rise and fall time of 50 psec and a duty cycle of 50%. All other clock signals should be derived from this primary signal using actual logic (e.g. complimentary clocks, non-overlapping clocks, clocks with a faster rise and fall time, etc.). The logic schematics and the simulated waveforms for these derived clocks should be included in the report.

2. Simulation

Use HSPICE to simulate the design. The simulation should be executed over the complete sequence of output signals (15 output values). Identify clearly the critical path in your design. Make sure that your simulation model contains good estimations of all the necessary parasitics.

3. Layout

No layout is needed for this project.

4. Reporting

Considerable emphasis is placed on the reporting of your results. Instead of writing a report however, you and your partner will present a poster on your results. You will get 8 minutes to explain why your design is good, and what is special about it. The poster should contain at most 9 power-point slides. One of these slides should contain your names and summarize in a number of bullets your important design decisions and results. The rest should be used to show the important schematics, simulation results, and everything to demonstrate the functionality and performance of your design. MAKE SURE THAT YOUR POSTER CONTAINS THE MAXIMUM INFORMATION IN THE MINIMUM NUMBER OF WORDS. Graphics convey data a lot more effectively.
In addition, you are required to submit a single sheet that summarizes your results (by e-mail).

Grading

The quality of the poster is a important (major) part of the grade!

Again, the grade will be divided as follows:

30%	Result + Correctness
30%	Creativity of Approach
40%	Poster Quality

Enjoy!

