Chapter 3
PROBLEMS

For all problems, use the device parameters provided in Chapter 3 (Tables 3.2 and 3.5) and the inside back book cover, unless otherwise mentioned. Also assume T = 300 K by default.

1. [E,SPICE,3.2.2]

a. Consider the circuit of Figure 0.1. Using the simple model, with $V_{Don} = 0.7$ V, solve for I_D.

b. Find I_D and V_D using the ideal diode equation. Use $I_s = 10^{-14}$ A and $T = 300$ K.

c. Solve for V_{D1}, V_{D2}, and I_D using SPICE.

d. Repeat parts *b* and *c* using $I_S = 10^{-16}$ A, $T = 300$K, and $I_S = 10^{-14}$A, $T = 350$ K.

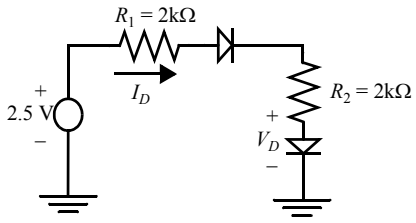

Figure 0.1 Resistor diode circuit.

2. [M, None, 3.2.3] For the circuit in Figure 0.2, $V_s = 3.3$ V. Assume $A_D = 12$ μm^2, $\phi_0 = 0.65$ V, and $m = 0.5$. $N_A = 2.5$ E16 and $N_D = 5$ E15.

a. Find I_D and V_D.

b. Is the diode forward- or reverse-biased?

c. Find the depletion region width, W_j, of the diode.

d. Use the parallel-plate model to find the junction capacitance, C_j.

e. Set V_s = 1.5 V. Again using the parallel-plate model, explain qualitatively why C_j increases.

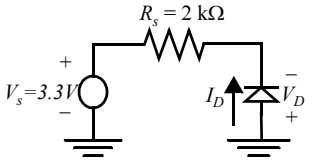

Figure 0.2 Series diode circuit

3. [E, None, 3.3.2] Figure 0.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the mode of operation (saturation, linear, or cutoff) and drain current I_D for each of the biasing configurations given below. Verify with SPICE. Use the following transistor data: NMOS: $k_n' = 115\mu A/V^2$, $V_{T0} = 0.43$ V, $\lambda = 0.06$ V^{-1}, PMOS: $k_p' = 30$ μA/V^2, $V_{T0} = -0.4$ V, $\lambda = -0.1$ V^{-1}. Assume $(W/L) = 1$.

a. NMOS: $V_{GS} = 2.5$ V, $V_{DS} = 2.5$ V. PMOS: $V_{GS} = -0.5$ V, $V_{DS} = -1.25$ V.

b. NMOS: $V_{GS} = 3.3$ V, $V_{DS} = 2.2$ V. PMOS: $V_{GS} = -2.5$ V, $V_{DS} = -1.8$ V.

c. NMOS: $V_{GS} = 0.6$ V, $V_{DS} = 0.1$ V. PMOS: $V_{GS} = -2.5$ V, $V_{DS} = -0.7$ V.

4. [E, SPICE, 3.3.2] Using SPICE plot the *I-V* characteristics for the following devices.

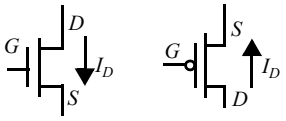

Figure 0.3 NMOS and PMOS devices.

a. NMOS $W = 1.2\mu m$, $L = 0.25\mu m$

b. NMOS $W = 4.8\mu m$, $L = 0.5\mu m$

c. PMOS $W = 1.2\ \mu m$, $L = 0.25\ \mu m$

d. PMOS $W = 4.8\ \mu m$, $L = 0.5\ \mu m$

5. [E, SPICE, 3.3.2] Indicate on the plots from problem 4.

a. the regions of operation.

b. the effects of channel length modulation.

c. Which of the devices are in velocity saturation? Explain how this can be observed on the *I-V* plots.

6. [M, None, 3.3.2] Given the data in Table 0.1 for a short channel NMOS transistor with $V_{DSAT} = 0.6\ V$ and $k' = 100\ \mu A/V^2$, calculate V_{T0}, γ, λ, $2|\phi_f|$, and W / L:

Table 0.1 Measured NMOS transistor data

	V_{GS}	V_{DS}	V_{BS}	I_D (μA)
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	–1	1146
5	2	1.8	-2	1039

7. [E, None, 3.3.2] Given Table 0.2 ,the goal is to derive the important device parameters from these data points. As the measured transistor is processed in a deep-submciron technology, the '**unified model**' holds. From the material constants, we also could determine that the saturation voltage V_{DSAT} equals -1V. You may also assume that $-2\Phi_F = -0.6V$.

NOTE: The parameter values on Table 3.3 do NOT hold for this problem.

a. Is the measured transistor a PMOS or an NMOS device? Explain your answer.

b. Determine the value of V_{T0}.

c. Determine γ.

d. Determine λ.

e. Given the obtained answers, determine for each of the measurements the operation region of the transistor (choose from *cutoff, resistive, saturated, and velocity saturated*). Annotate your finding in the right-most column of the above.

Table 0.2 Measurements taken from the MOS device, at different terminal voltages.

Measurement number	VGS (V)	VDS (V)	VSB (V)	ID (μA)	Operation Region?
1	-2.5	-2.5	0	-84.375	
2	1	1	0	0.0	
3	-0.7	-0.8	0	-1.04	
4	-2.0	-2.5	0	-56.25	
5	-2.5	-2.5	-1	-72.0	
6	-2.5	-1.5	0	-80.625	
7	-2.5	-0.8	0	-66.56	

8. [M, None, 3.3.2] An NMOS device is plugged into the test configuration shown below in Figure 0.4. The input V_{in} =2V. The current source draws a constant current of 50 μA. *R* is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $k' = 110*10^{-6}$ V/A^2, $V_T = 0.4$, and V_{DSAT} = 0.6V. The transistor has a W/L = 2.5μ/0.25μ. For simplicity body effect and channel length modulation can be neglected. i.e λ=0, γ=0. .

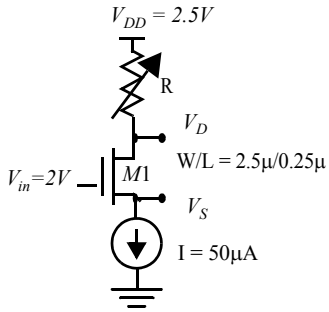

Figure 0.4 Test configuration for the NMOS device.

a. When *R* =10kΩ find the operation region, V_D and V_S.

b. When R= 30kΩ again determine the operation region V_D, V_S

c. For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively

9. [M, None, 3.3.2] Consider the circuit configuration of Figure 0.5.

a. Write down the equations (and only those) which are needed to determine the voltage at node *X*. Do NOT plug in any values yet. Neglect short channel effects and assume that $\lambda_p = 0$.

b. Draw the (approximative) load lines for both MOS transistor and resistor. Mark some of the significant points.

c. Determine the required width of the transistor (for $L = 0.25\mu m$) such that *X* equals 1.5 V.

d. We have, so far, assumed that M_1 is a long-channel device. Redraw the load lines assuming that M_1 is velocity-saturated. Will the voltage at *X* rise or fall?

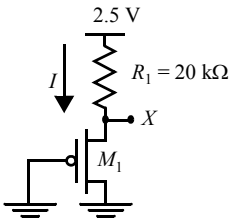

Figure 0.5 MOS circuit.

10. [M, None, 3.3.2] The circuit of Figure 0.6 is known as a *source-follower* configuration. It achieves a DC level shift between the input and output. The value of this shift is determined by the current I_0. Assume $\gamma = 0.4$, $2|\phi_f| = 0.6$ V, $V_{T0} = 0.43$ V, $k' = 115\ \mu A/V^2$, and $\lambda = 0$. The NMOS device has $W/L = 5.4\mu/1.2\mu$ such that the short channel effects are not observed.

a. Derive an expression giving V_i as a function of V_o and $V_T(V_o)$. If we neglect body effect, what is the nominal value of the level shift performed by this circuit.

b. The NMOS transistor experiences a shift in V_T due to the body effect. Find V_T as a function of V_o for V_o ranging from 0 to 1.5V with 0.25 V intervals. Plot V_T vs. V_o.

c. Plot V_o vs. V_i as V_o varies from 0 to 1.5 V with 0.25 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter? At V_o (body effect) = 1.5 V, find V_o (ideal) and, thus, determine the maximum error introduced by body effect.

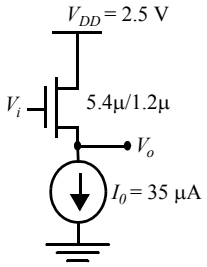

Figure 0.6 Source-follower level converter.

11. [M, SPICE, 3.3.2] Problem 11 uses the MOS circuit of Figure 0.7.

a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). $V_{DD} = 2.5$ V.

b. Repeat *a* using SPICE.

c. Repeat *a* and *b* using a MOS transistor with $(W / L) = 4 / 1$. Is the discrepancy between manual and computer analysis larger or smaller. Explain why.

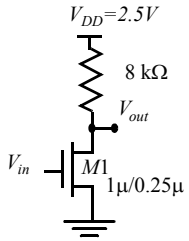

Figure 0.7 MOS circuit.

12. [E, None, 3.3.2]Below in Figure 0.8 is an I-V transfer curve for an NMOS transistor. In this problem, the objective is to use this I-V curve to obtain information about the transistor. The transistor has (W/L)=(1μ/1μ). It may also be assumed that velocity saturation does not play a role in this example. Also assume $-2\Phi_F$ = 0.6V. Using Figure 0.8 determine the following parameters: device V_{TO}, γ, λ.

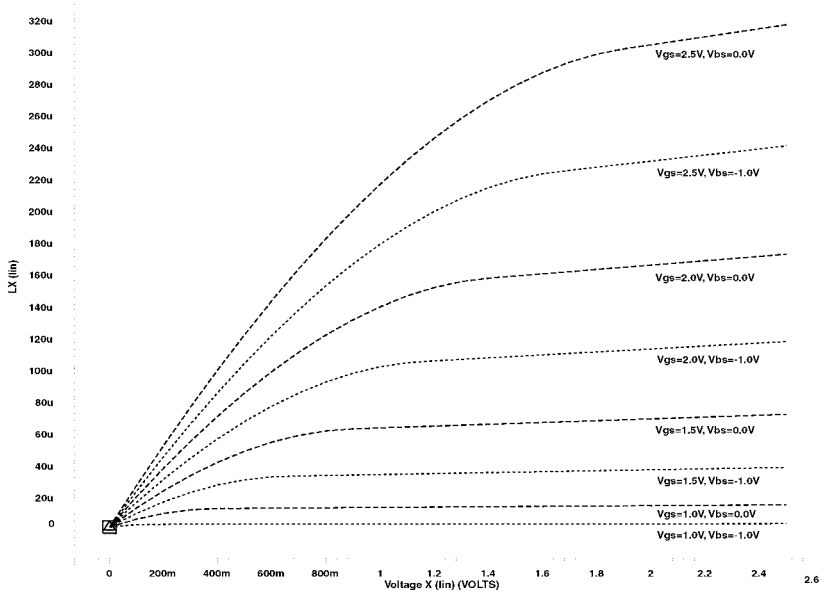

Figure 0.8 I-V curves

13. [E, None , 3.3.2]The curves below in Figure 0.9 represent the gate voltage(V_{GS}) vs. drain current (I_{DS}) of two NMOS devices which are on the same die and operate in subthreshold region. Due to process variations on the same die the curves do not overlap.

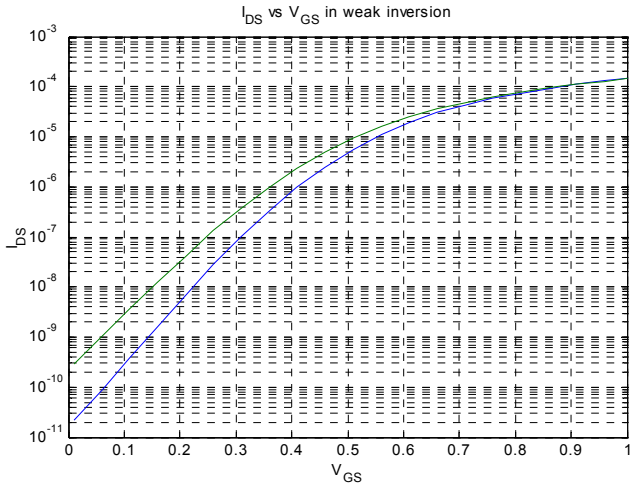

Figure 0.9 Subthreshold current curves. Difference is due to process variations

Also assume that the transistors are within the same circuit configurations as Figure 0.10 in If the in put voltages are both V_{in} = 0.2V. What would be the respective durations to discharge the load of C_L = 1pF attached to the drains of these devices.

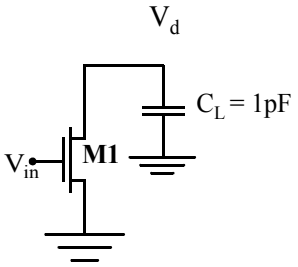

Figure 0.10 The circuit for testing the time to discharge the load capacitance through a device operating in subthreshold region.

14. [M, None, 3.3.2] Short-channel effects:

a. Use the fact that current can be expressed as the product of the carrier charge per unit length and the velocity of carriers (I_{DS} = Q*v)* to derive I_{DS} as a function of *W*, C_{ox}, $V_{GS} - V_T$, and carrier velocity *v.*

b. For a long-channel device, the carrier velocity is the mobility times the applied electric field. The electrical field, which has dimensions of V/m, is simply $(V_{GS} - V_T) / 2L$. Derive I_{DS} for a long-channel device.

c. From the equation derived in *a*, find I_{DS} for a short-channel device in terms of the maximum carrier velocity, v_{max}.

Based on the results of *b* and *c* describe the most important differences between short-channel and long-channel devices.

15. [C, None, 3.3.2] Another equation, which models the velocity-saturated drain current of an MOS transistor is given by

$$I_{dsat} = \frac{1}{1 + (V_{GS} - V_t)/(E_{sat}L)} \left(\frac{\mu_0 C_{ox}}{2} \right) \frac{W}{L} (V_{GS} - V_T)^2$$

Using this equation it is possible to see that velocity saturation can be modeled by a MOS device with a source-degeneration resistor (see Figure 0.11).

a. Find the value of R_S such that $I_{DSAT}(V_{GS}, V_{DS})$ for the composite transistor in the figure matches the above velocity-saturated drain current equation. *Hint: the voltage drop across R_S is typically small.*

b. Given $E_{sat} = 1.5$ V/μm and $k' = \mu_0 C_{ox} = 20$ μA/V^2, what value of R_S is required to model velocity saturation. How does this value depend on W and L?

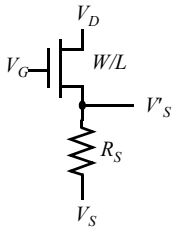

Figure 0.11 Source-degeneration model of velocity saturation.

16. [E, None, 3.3.2] The equivalent resistances of two different devices need to be computed.

a. First, consider the fictive device whose I-V characteristic is given in Figure 0.12. Constant k has the dimension of S (or1/Ω). V_0 is a voltage characteristic to the device. Calculate the equivalent resistance for an output voltage transition from 0 to $2V_0$ by integrating the resistance as a function of the voltage.

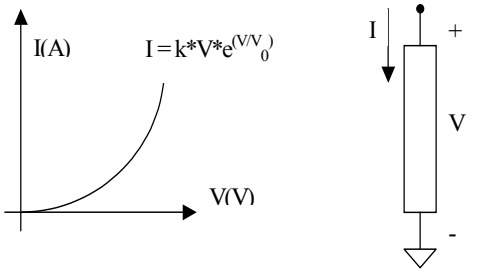

Figure 0.12 Fictive device whose equivalent resistance is to be calculated.

b. Next, obtain the resistance equation 3.43 using the Figure 0.13. Assuming the V_{GS} is kept at V_{DD}, Calculate the Req as output (V_{DS}) transitions from V_{DD} to $V_{DD}/2$.(Figure 0.13).

Hint: Make sure you use the Short channel Unified MOS Model equations. **Hint:** You will need to use the expansion. $ln(1+x) \approx x - x^2/2 + x^3/3$

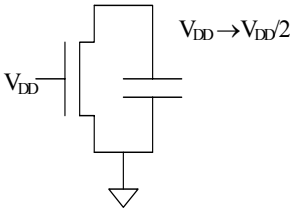

Figure 0.13 The equivalent resistance is to be computed for the H→L transition.

17. [M, None, 3.3.3] Compute the gate and diffusion capacitances for transistor *M*1 of Figure 0.7. Assume that drain and source areas are rectangular, and are 1 μm wide and 0.5 μm long. Use the parameters of Example 3.5 to determine the capacitance values. Assume $m_j = 0.5$ and $m_{jsw} = 0.44$. Also compute the total charge stored at node *In*, for the following initial conditions:

a. $V_{in} = 2.5$ V, $V_{out} = 2.5$ V, 0.5 V, and 0 V.

b. $V_{in} = 0$ V, $V_{out} = 2.5$ V, 0.5 V, and 0 V.

18. [E, None, 3.3.3]Consider a CMOS process with the following capacitive parameters for the NMOS transistor: C_{GSO}, C_{GDO}, C_{OX}, C_J, m_j, C_{jsw}, m_{jsw}, and PB, with the lateral diffusion equal to L_D. The MOS transistor M1 is characterized by the following parameters: W, L, AD, PD, AS, PS.

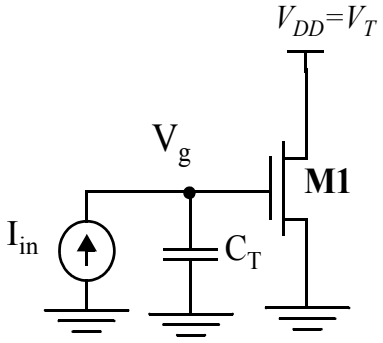

Figure 0.14 Circuit to measure total input capacitance

a. Consider the configuration of Figure 0.14. V_{DD} is equal to V_T (the threshold voltage of the transistor) Assume that the initial value of V_g equals 0. A current source with value I_{in} is applied at time 0. Assuming that all the capacitance at the gate node can be lumped into a single, grounded, linear capacitance C_T, derive an expression for the time it will take for V_g to reach 2 V_T

b. The obvious question is now how to compute C_T. Among, C_{db}, C_{sb}, C_{gs}, C_{gd}, C_{gb} which of these parasatic capacitances of the MOS transistor contribute to C_T. For those that contribute to C_T write down the expression that determines the value of the contribution. Use only the parameters given above. If the transistor goes through different operation regions and this impacts the value of the capacitor, **determine the expression of the contribution for each region (and indicate the region)**.

c. Consider now the case depicted in Figure 0.15. Asssume that V_d is initially at 0 and we want to charge it up to 2 V_T. Again among, C_{db}, C_{sb}, C_{gs}, C_{gd}, C_{gb} which device capacitances contribute to the total drain capacitance? Once again, make sure you differentiate between different operation regions..

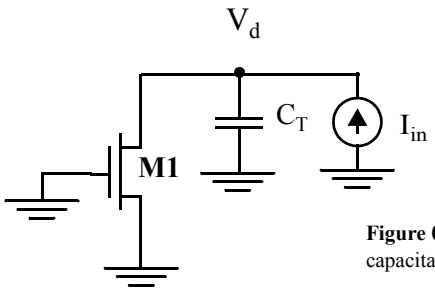

Figure 0.15 Circuit to measure the total drain capacitance

19. [M, None, 3.3.3]For the NMOS transistor in Figure 0.16, **sketch the voltages** at the source and at the drain as a function of time. Initially, both source and drain are at +2.5 volts. Note that the drain is open circuited. The 10 μA current source is turned on at t=0. Device parameters:W/L_{eff} = 125μ/0.25μ ; μC_{ox} = 100 μA/V^2 ; C_{ox} = 6fF/μ^2 ;C_{OL}(per width) = 0.3 fF/μ ; C_{sb} = 100 fF; Cdb = 100fF;V_{DSAT} =1V.

HINT: Do not try to solve this analytically. Just use a qualitative analysis to derive the different operation modes of the circuit and the devices**.**

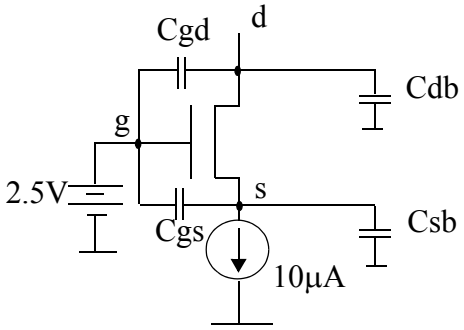

Figure 0.16 Device going through different operation regions over time

20. [C, SPICE, 3.4] Though impossible to quantify exactly by hand, it is a good idea to understand process variations and be able to at least get a rough estimate for the limits of their effects.

a. For the circuit of Figure 0.7, calculate nominal, minimum, and maximum currents in the NMOS device with V_{in} = 0 V, 2.5 V and 5 V. Assume 3σ variations in V_{T0} of 25 mV, in k' of 15%, and in lithographic etching of 0.15 μm.

b. Analyze the impact of these current variations on the output voltage. Assume that the load resistor also can vary by 10%. Verify the result with SPICE.

21. [E, None, 3.5] A state-of-the-art, synthesizable, embedded microprocessor consumes 0.4mW/MHz when fabricated using a 0.18 μm process. With typical standard cells (gates), the area of the processor is 0.7 mm2. Assuming a 100 Mhz clock frequency, and 1.8 V power

supply. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.

a. Using fixed voltage scaling and constant frequency, what will the area, power consumption, and power density of the same processor be, if scaled to 0.12 μm technology, assuming the same clock frequency?

b. If the supply voltage in the scaled 0.12 μm part is reduced to 1.5 V what will the power consumption and power density be?

c. How fast could the scaled processor in Part (b) be clocked? What would the power and power density be at this new clock frequency?

d. Power density is important for cooling the chip and packaging. What would the supply voltage have to be to maintain the same power density as the original processor?

22. The superscalar, superpipelined, out-of-order executing, highly parallel, fully x86 compatible JMRII microprocessor was fabricated in a 0.25 m technology and was able to operate at 100 MHZ, consuming 10 watts using a 2.5 V power supply.

a. Using fixed voltage scaling, what will the speed and power consumption of the same processor be if scaled to 0.1 μm technology?

b. If the supply voltage on the 0.1 μm part were scaled to 1.0 V, what will the power consumption and speed be?

c. What supply should be used to fix the power consumption at 10 watts? At what speed would the processor operate?