Circuit Simulation

- *Objectives*:
  - fabricating an IC costs $1000 ... $100,000 per run

    ---> nice to get it “right” the first time
  - check results from hand-analysis

    (e.g. validity of assumptions)
  - evaluate functionality, speed, accuracy, ... of large circuit blocks or entire chips
- *Simulators*:
  - **SPICE**: invented at UC Berkeley circa 1970-1975

    commercial versions: HSPICE, PSPICE, I-SPICE, ... (same core as Berkeley SPICE, but add functionality, improved user interface, ...)

    EE 105: student version of PSPICE on PC, limited to 10 transistors
  - other simulators for higher speed, special needs (e.g. SPLICE, RSIM)
- *Limitations*:
  - simulation results provide no insight (e.g. how to increase speed of circuit)
  - results sometimes wrong (errors in input, effect not modeled in SPICE)

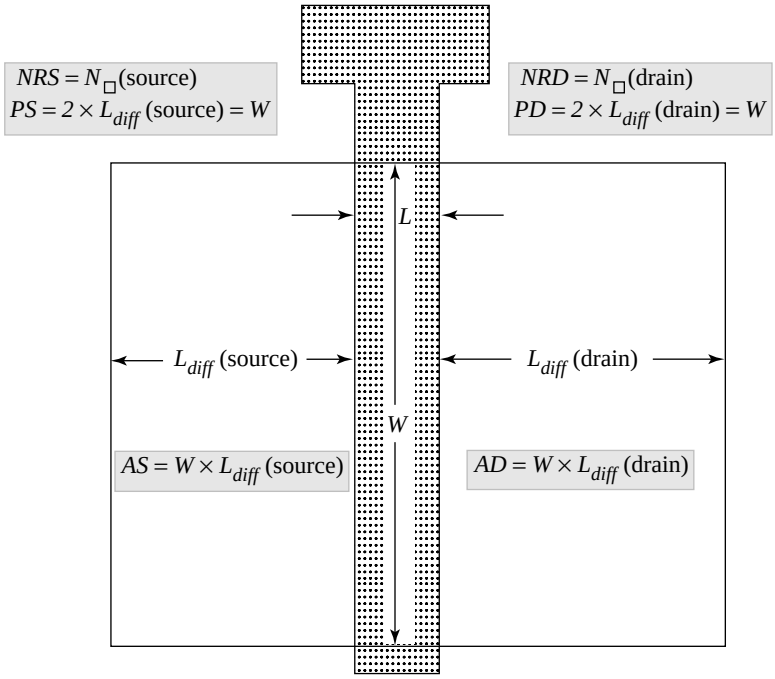
  ===> always do hand-analysis first and COMPARE RESULTS

MOSFET Geometry in SPICE

- Statement for MOSFET ... *D,G,S,B* are node numbers for drain, gate, source, and bulk terminals

M*name D G S B MODname* **L= _ W=_ AD= _ AS=_ PD=_ PS=_**

MODname specifies the model name for the MOSFET



MOSFET Model Statement

.MODEL *MODname* **NMOS/PMOS VTO=_ KP=_ GAMMA=_ PHI=_ LAMBDA=_ RD=_ RS=_ RSH=_ CBD=_ CBS=_CJ=_ MJ=_ CJSW=_ MJSW=_ PB=_ IS= _ CGDO=_ CGSO=_ CGBO=_ TOX=_ LD=_**

Parameter name (SPICE / this text)	SPICE symbol Eqs. (4.93), (4.94)	Analytical symbol Eqs. (4.59), (4.60)	Units
channel length	L_{eff}	L	m
polysilicon gate length	L	L_{gate}	m
lateral diffusion/ gate-source overlap	LD	L_D	m
transconductance parameter	KP	$\mu_n C_{ox}$	A/V^2
threshold voltage / zero-bias threshold	VTO	V_{TnO}	V
channel-length modulation parameter	$LAMBDA$	λ_n	V^{-1}
bulk threshold / backgate effect parameter	$GAMMA$	γ_n	$V^{1/2}$
surface potential / depletion drop in inversion	PHI	$-\phi_p$	V

DC Drain Current Equations:

$$I_{DS} = 0 \qquad (V_{GS} \le -V_{TH})$$

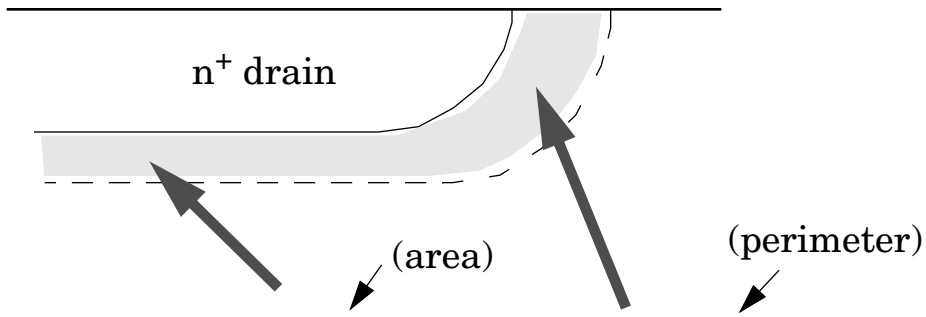
$$I_{DS} = \frac{KP}{2}(W/L_{eff})V_{DS}[2(V_{GS} - V_{TH}) - V_{DS}](1 + LAMBDA \cdot V_{DS}) \qquad (0 \le V_{DS} \le V_{GS} - V_{TH})$$

$$I_{DS} = \frac{KP}{2}(W/L_{eff})(V_{GS} - V_{TH})^2(1 + LAMBDA \cdot V_{DS}) \qquad (0 \le V_{GS} - V_{TH} \le V_{DS})$$

$$V_{TH} = V_{TO} + GAMMA(\sqrt{2 \cdot PHI - V_{BS}} - \sqrt{2 \cdot PHI})$$

Capacitances

SPICE includes the “sidewall” capacitance due to the perimeter of the source and drain junctions --



$$C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}$$

Gate-source and gate-bulk overlap capacitance are specified by *CGDO* and *CGSO* (units: F/m).

Level 1 MOSFET model:

```
.MODEL MODN NMOS LEVEL=1 VTO=1 KP=50U LAMBDA=.033 GAMMA=.6
+ PHI=0.8 TOX=1.5E-10 CGDO=5E-10 CGSO= 5e-10 CJ=1E-4 CJSW=5E-10
+ MJ=0.5 PB=0.95
```

The Level 1 model is adequate for channel lengths longer than about 1.5 μm

For sub-μm MOSFETs, BSIM = “Berkeley Short-Channel IGFET Model” is the industry-standard SPICE model.