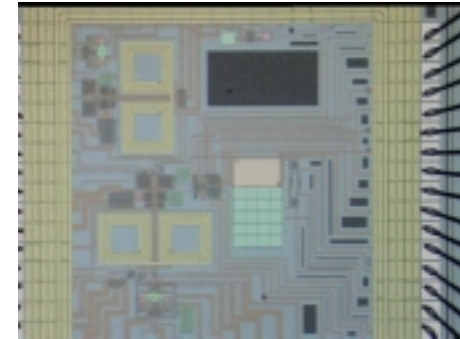




Design and power optimization of CMOS RF blocks operating in the moderate inversion region

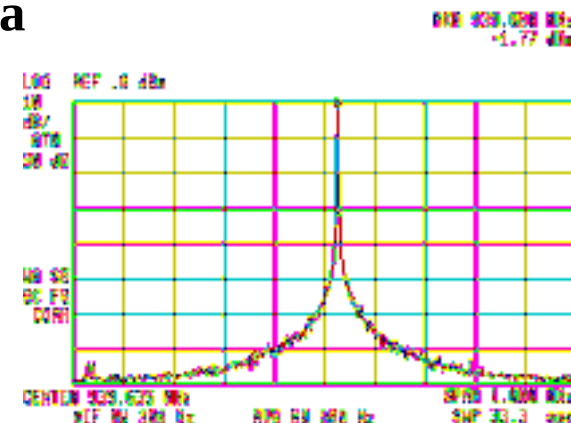
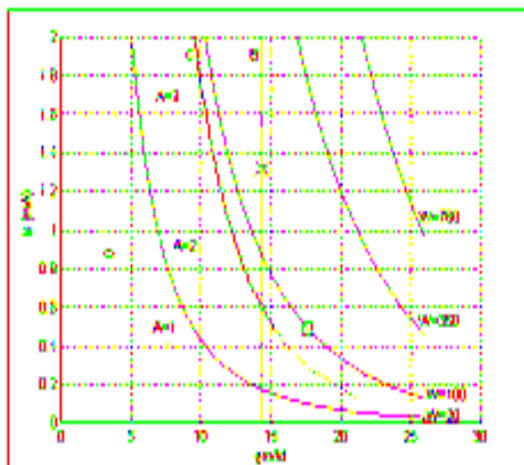
Leonardo Barboni, Raffaella Fiorelli, Fernando Silveira

Instituto de Ingeniería Eléctrica

Facultad de Ingeniería

Universidad de la República

Montevideo, Uruguay

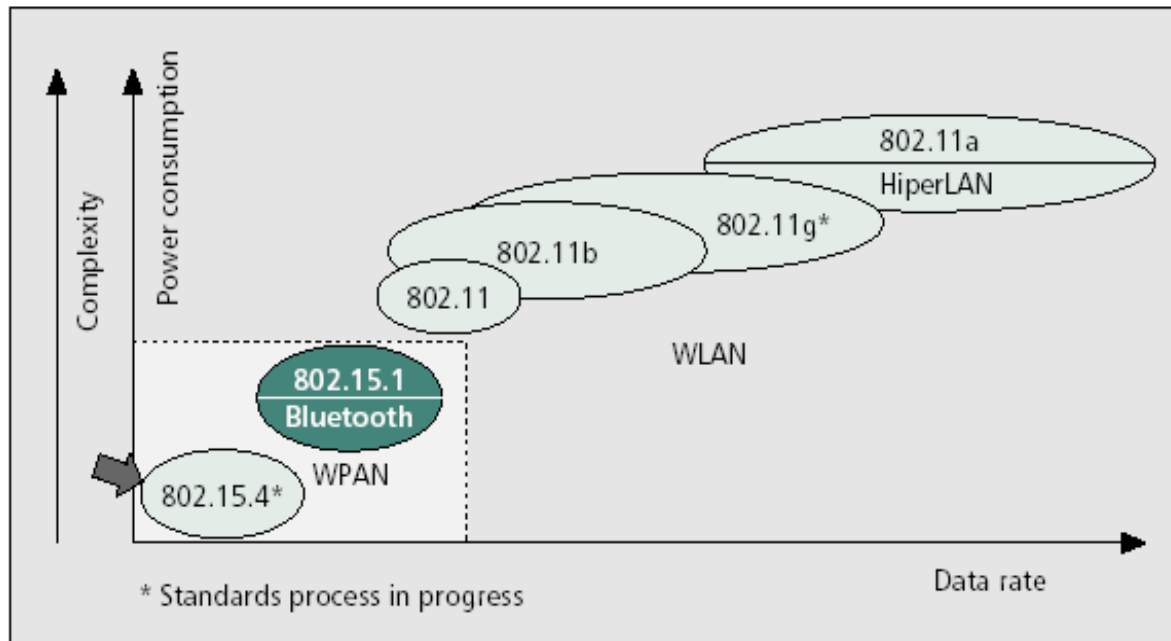


Outline

- ◆ I. Motivations, Objectives, Introduction
- ◆ II. Tool for CMOS RF Amplifier Power Optimization
- ◆ III. 900 MHz Amplifiers prototypes and experimental results
- ◆ IV. 900 MHz Voltage Controlled Oscillator Design
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 - Design Methodology and Trade Offs
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I. Motivations and Framework.

- ◆ Applications: Short Range (< 10m) Links for Wireless Sensors or Telemetry (WPAN: Wireless Personal Area Networks)



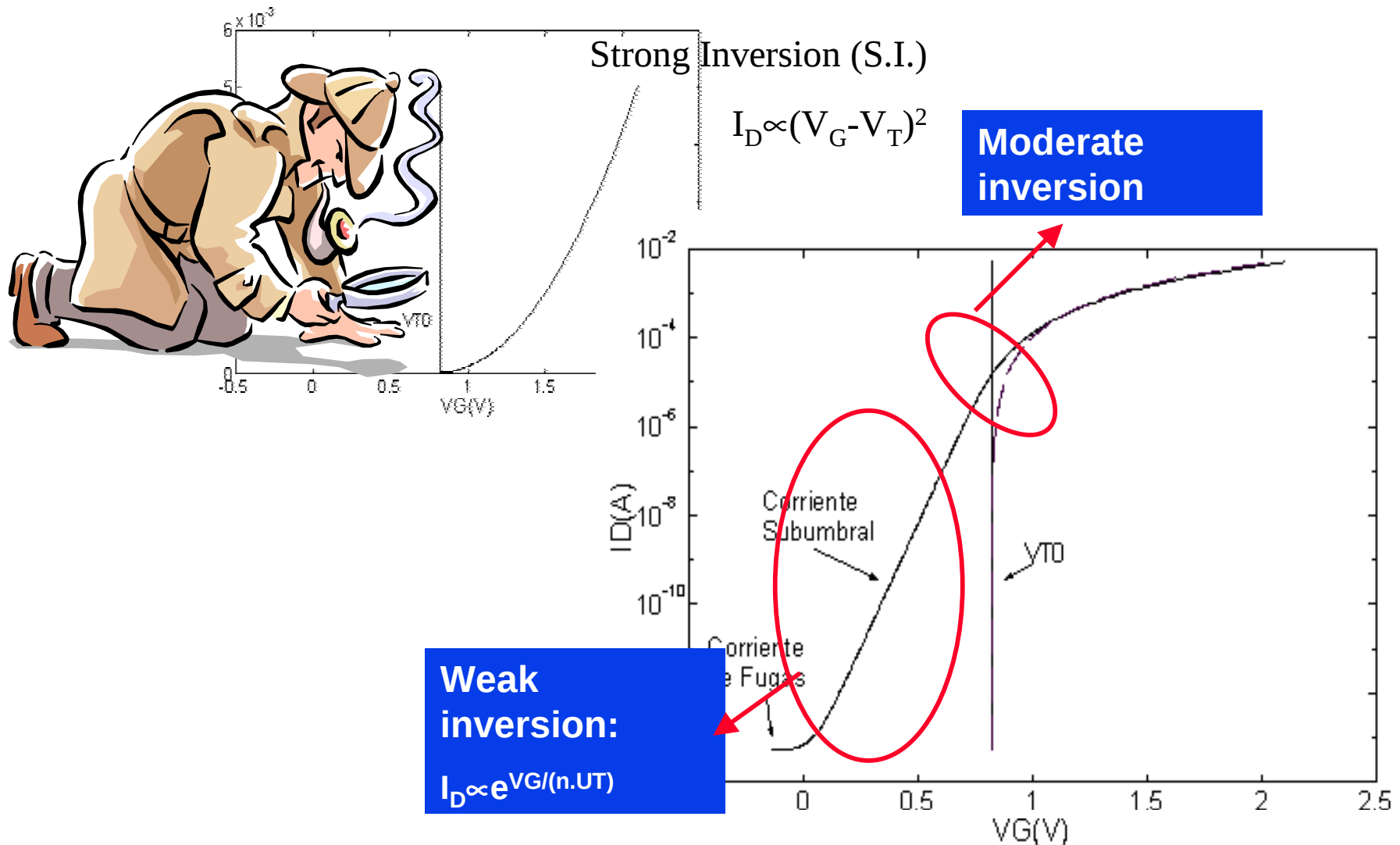
- IEEE 802.15.4 (2003) / Zigbee
- f (MHz): 868 / 915 / 2400
- 1 / 10 / 16 Channels
- 20 / 40 / 250 kbps

(*)"IEEE 802.15.4: A Developing Standard for Low Power Low Cost Wireless Personal Area Networks", IEEE Network, Oct2001

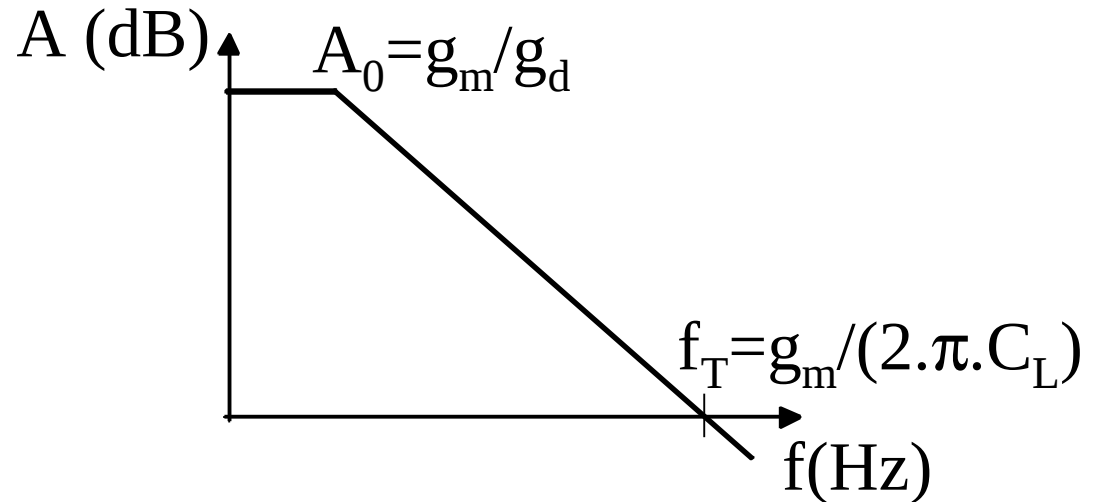
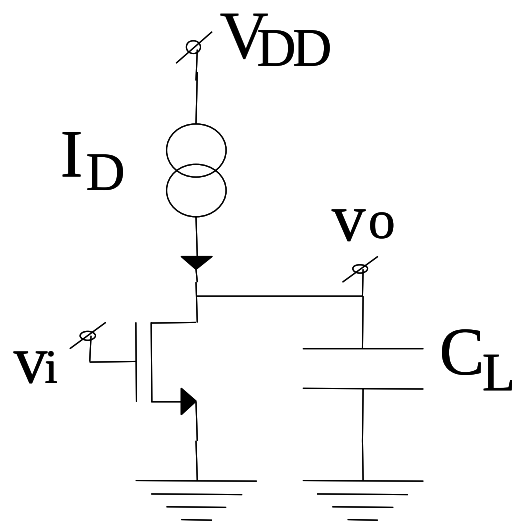
I. Objectives

- ◆ Design of IEEE 802.15.4 (or ad hoc) transmitter + integrated sensor.
- ◆ Test possibility of translating low-frequency ultra low power analog experience to the RF domain.
- ◆ Tool to design and evaluate the operation of RF circuits in Weak and Moderate Inversion.
(previous work Porret et al, CSEM, 0.5 μ m, 433MHz, JSSC 3/2001)
- ◆ First experiences in design of RF integrated circuits.

I. Introduction: MOST Inversion Regimes



I. Introduction: “Intrinsic” MOS Amplifier



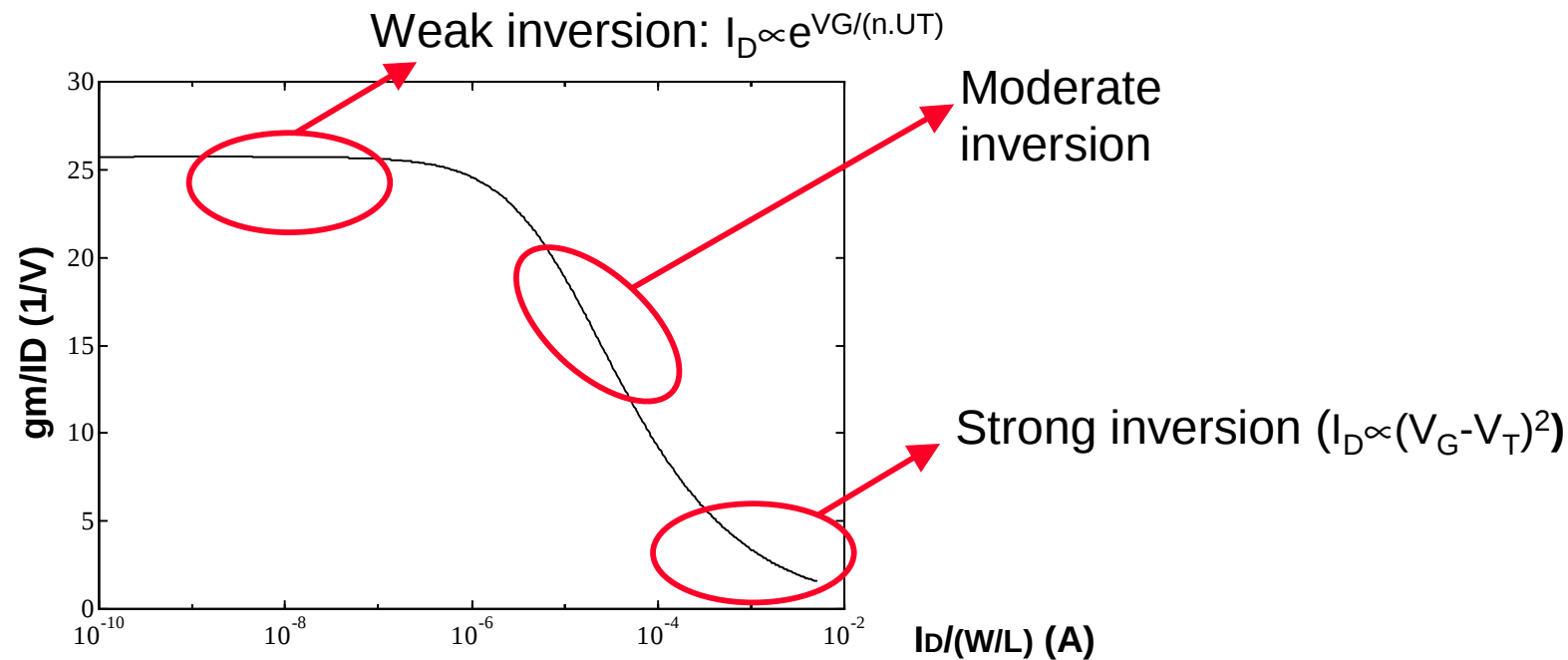
OTA: Operational Transconductance Amplifier

$$A_0 = g_m \cdot r_o = \frac{g_m}{g_d} = \frac{g_m}{I_D} \cdot V_A$$

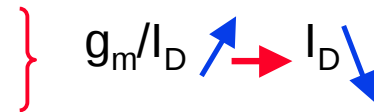
$$f_T = \frac{g_m}{2\pi C_L}, \quad A = \frac{A_0}{1 + \frac{s \cdot A_0}{2\pi f_T}}$$

- ◆ Consumption: I_D
- ◆ Speed g_m/C_L
- ◆ Speed - Consumption trade-off : g_m/I_D

I. Introduction: Optimum of Power Consumption



- Working towards WI



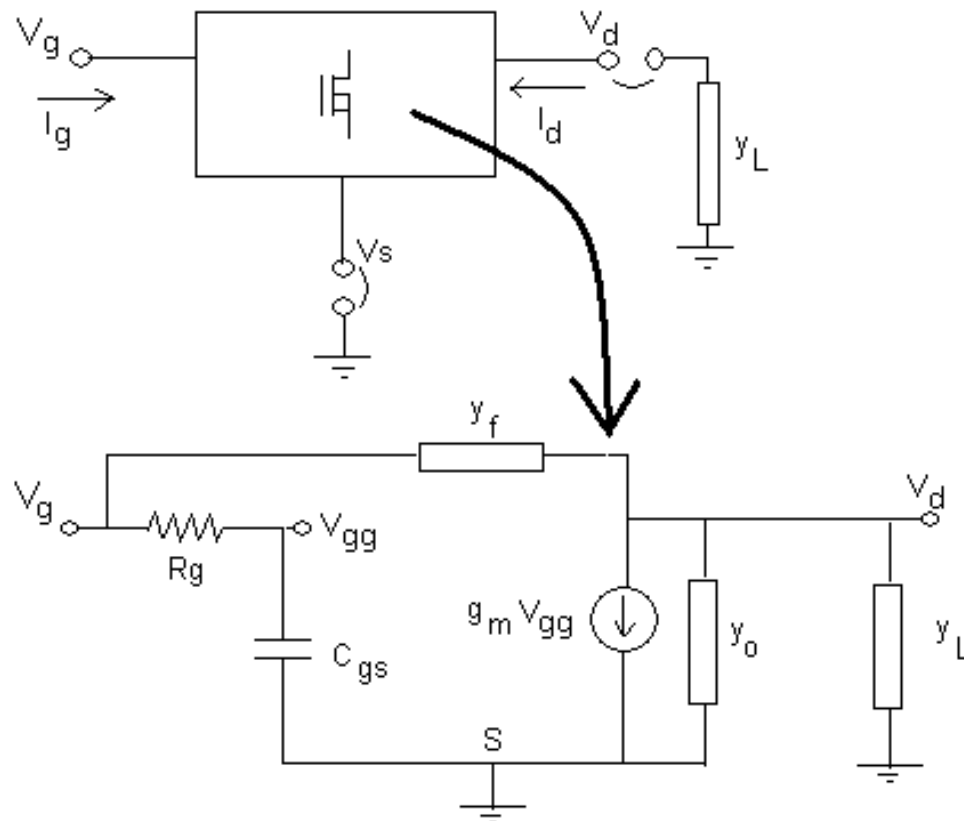
Usually an optimum exists in moderate inversion

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II. MOS transistor modeling (I)

- ◆ Continuous model for W.I to S.I => ACM model
- ◆ Basic structures modeled as 2-port network



II. MOS transistor modeling (2)

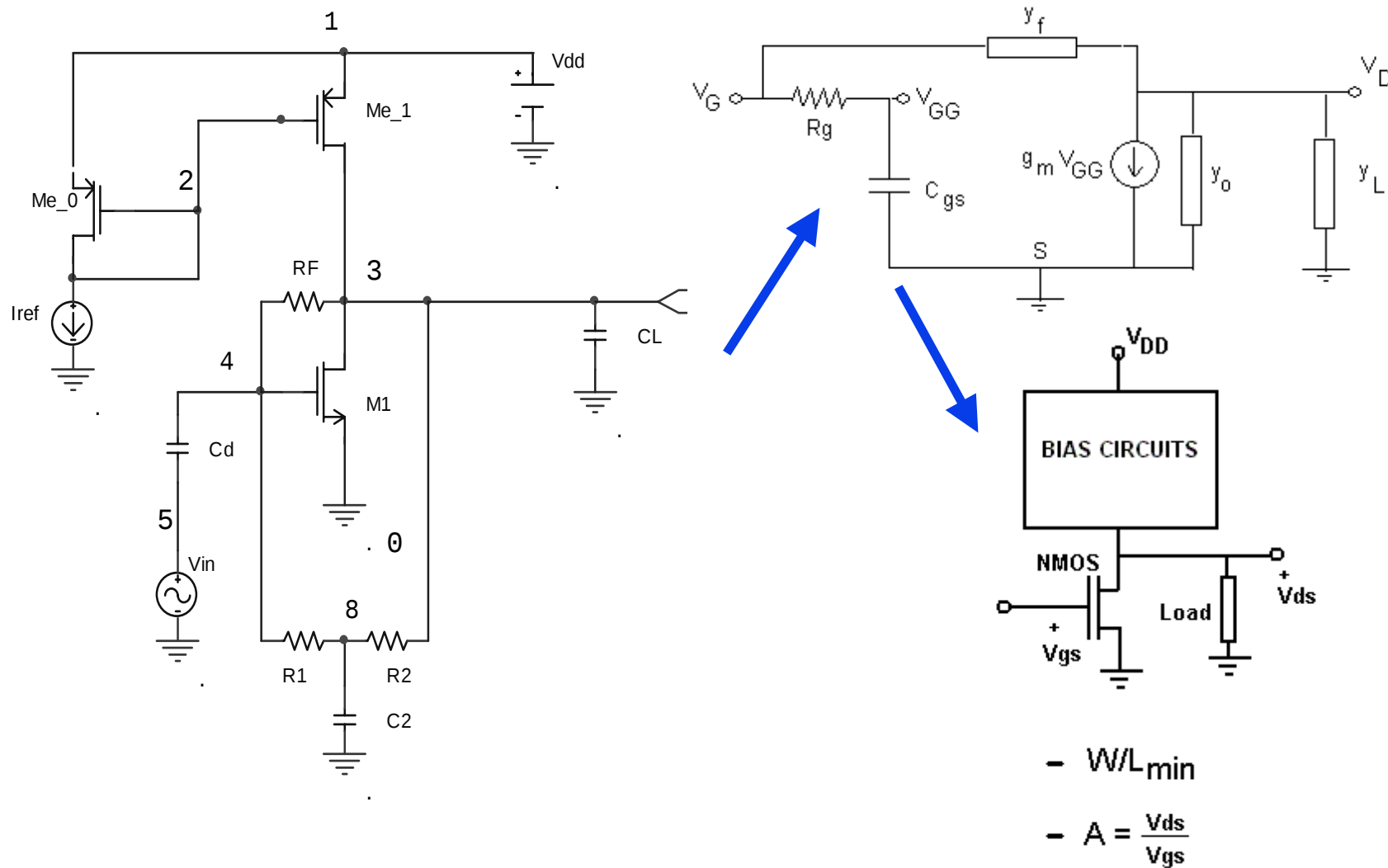
- ◆ Medium frequency model: 5 capacitors, Quasi-static, No velocity saturation effect
- ◆ Quasi-static:

$$g_m(\omega) = \frac{g_m}{1 + j\omega\tau_1 + \dots} \approx g_m$$

$$\rightarrow f_{QS\max} \approx \frac{f_T}{10} = \frac{1}{10} \frac{g_m}{2\pi(C_{gs} + C_{gb} + C_{gd})} = f\left(\frac{g_m}{I_D}\right)$$

→ **Quasi-static
model limit**

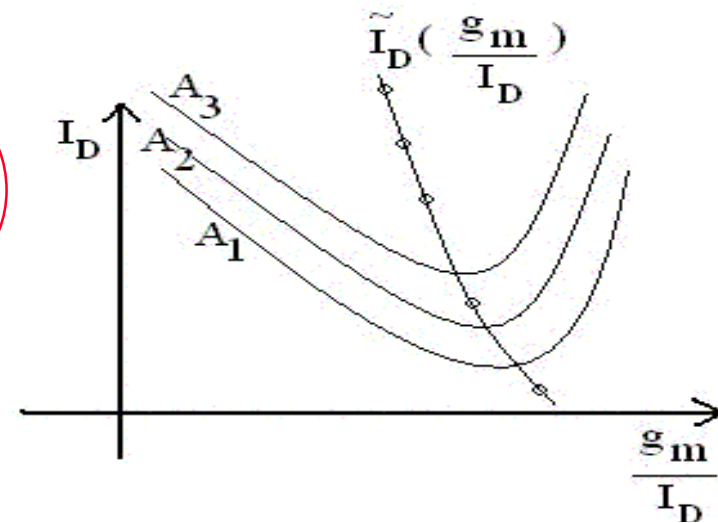
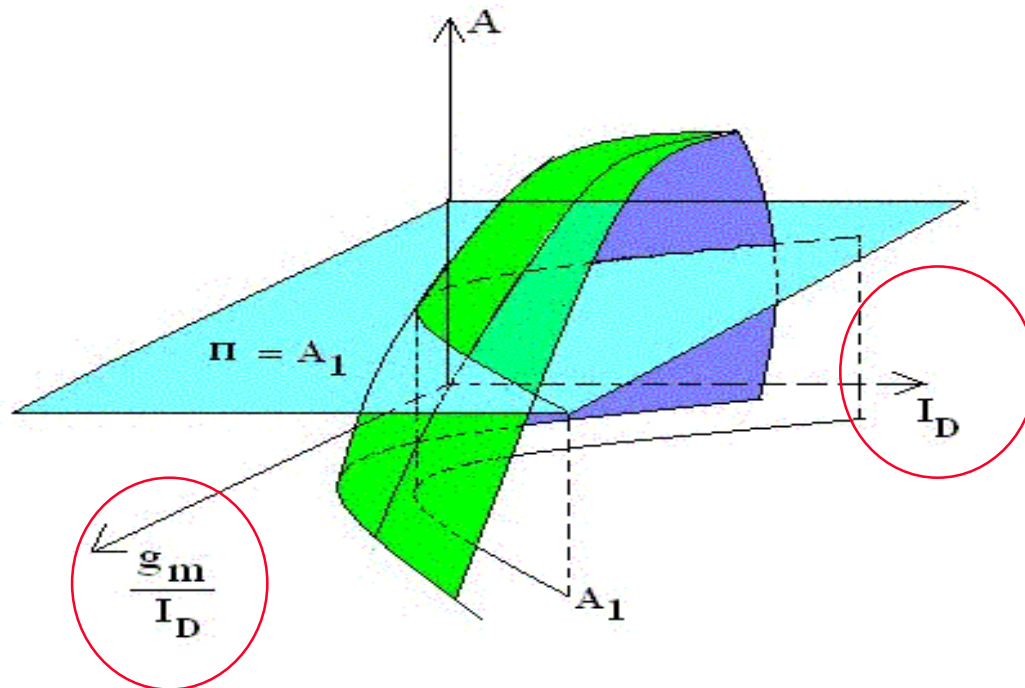
II. Object of study: Basic RF amplifier stages



II. Design Space Exploration

ISCAS 2006

- ◆ In the design space $(I_D - g_m/I_D)$ are calculated the curves of constant gain A .

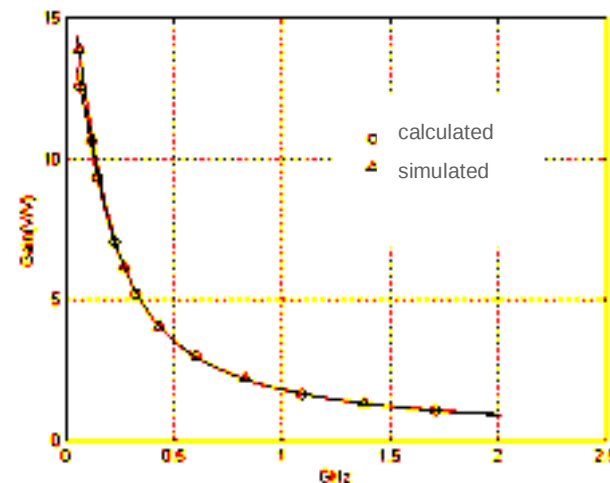
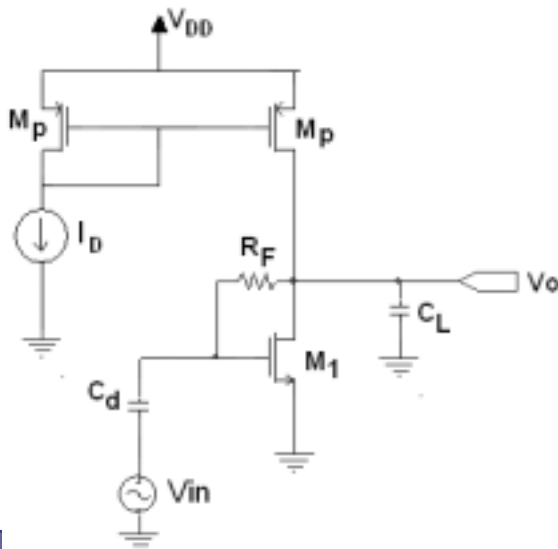
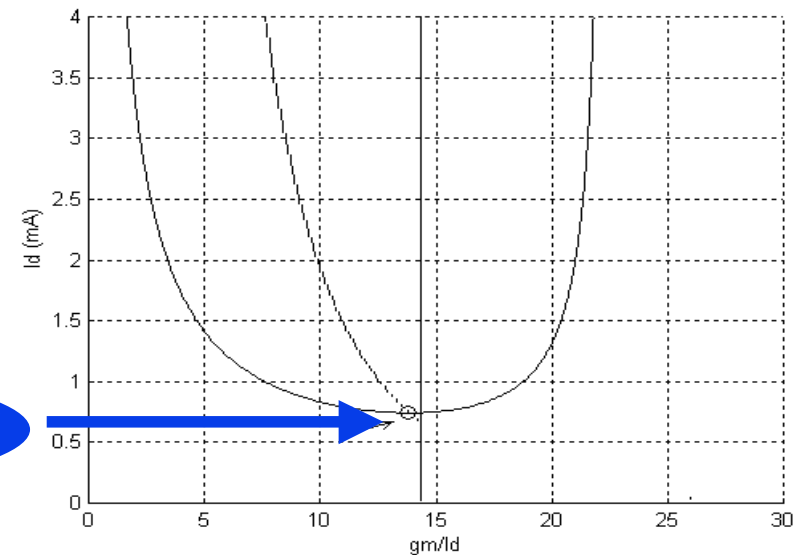


II. Ex. (1): One Stage Amplifier

One stage amplifier at 910MHz and $L=0.35\mu\text{m}$ with:

- ◆ Load capacitance $C_L=0.5\text{pF}$
- ◆ Feedback resistance $R_F=5\text{k}\Omega$
- ◆ R_g neglected

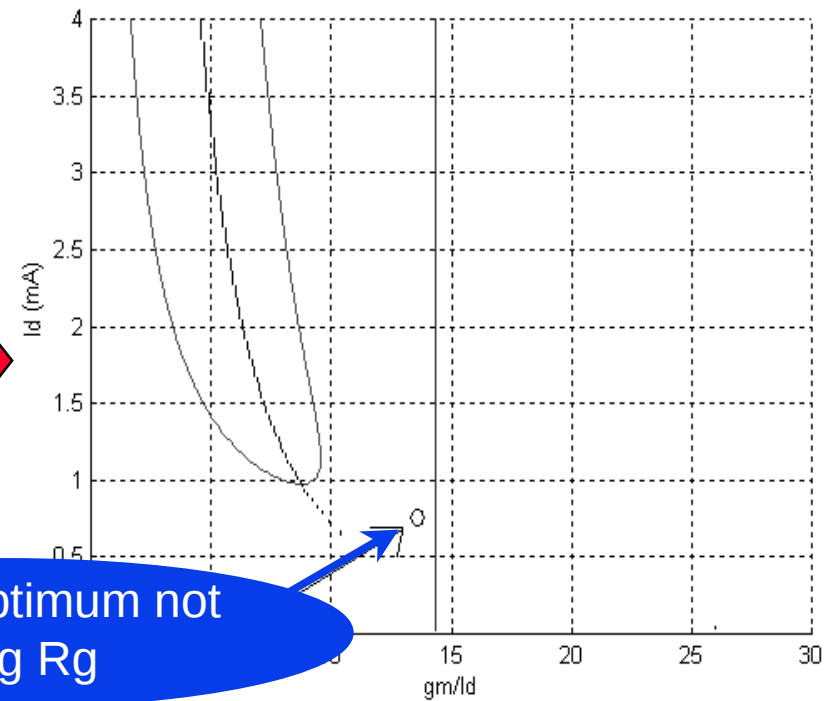
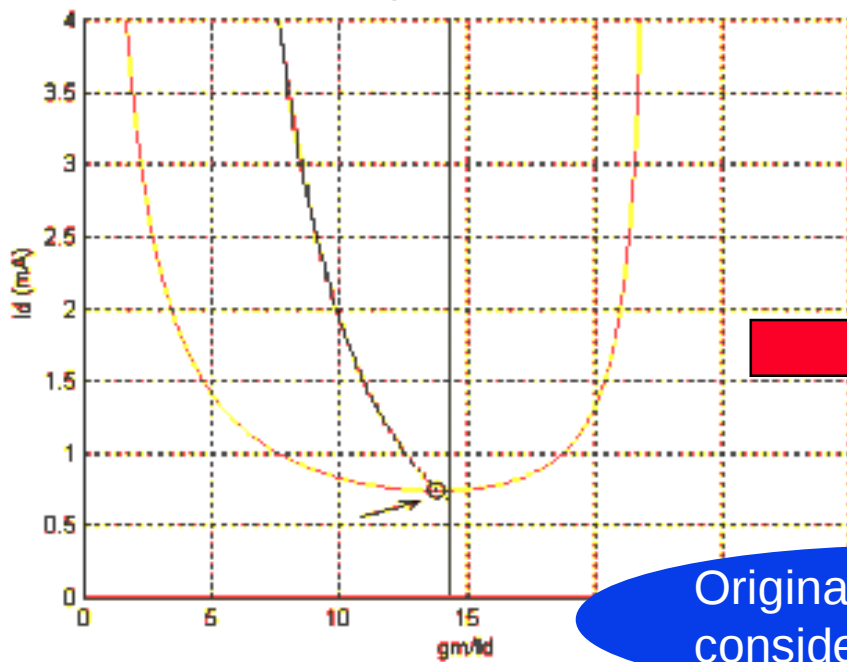
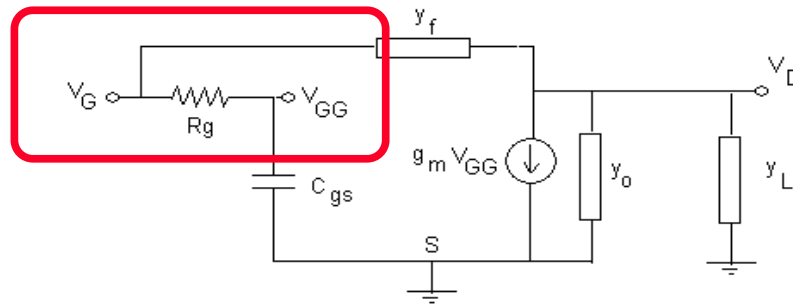
Minimum consumption @ $A=2\text{V/V}$



II. Ex. (2): Effect of gate resistance

- ◆ Gate resistance, non interdigitized layout

$$R_g \approx \frac{1}{3} \frac{W}{L} R^{\square}$$



Original optimum not considering R_g

II. Tool user interface

DCop =

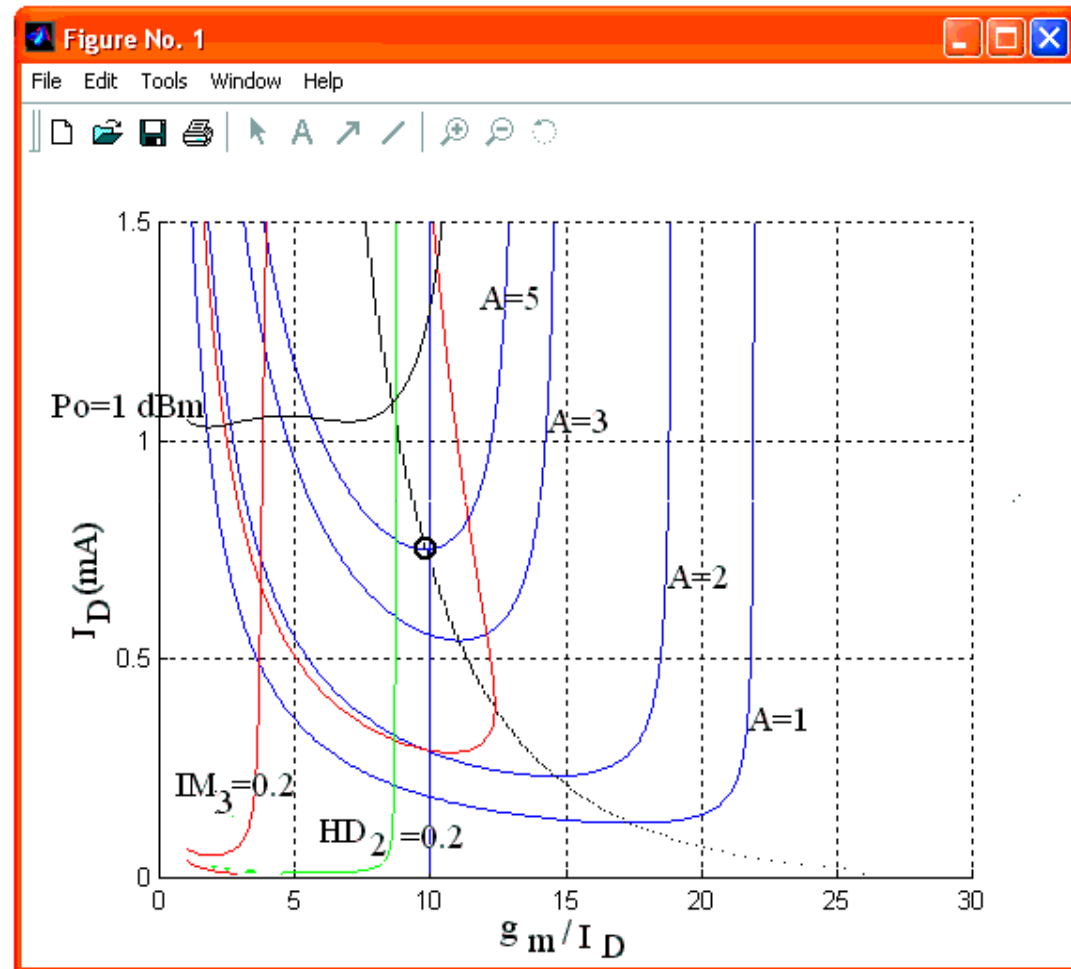
$I_D = 0.80 \text{ mA}$
 $g_m/I_D = 9.33$
 $W = 122.42 \mu\text{m}$
 $A(@f) = 6.1977$
 $RE(Z_{in}) = 445.13 \text{ ohm}$
 $IM(Z_{in}) = -728.11 \text{ ohm}$
 $V_{DSsat} = 0.23 \text{ V}$
 $V_{GS} = 0.67 \text{ V}$
 $f_{lim} = 0.99 \text{ GHz}$
 $G_p = 25.14$

HD2op =

$RE(Z_{in@2f}) = 211.02 \text{ ohm}$
 $IM(Z_{in@2f}) = -476.51 \text{ ohm}$
 $HD_2/V_{GS} = 0.96$
 $IM_3/V_{GS}^2 = 0.64$

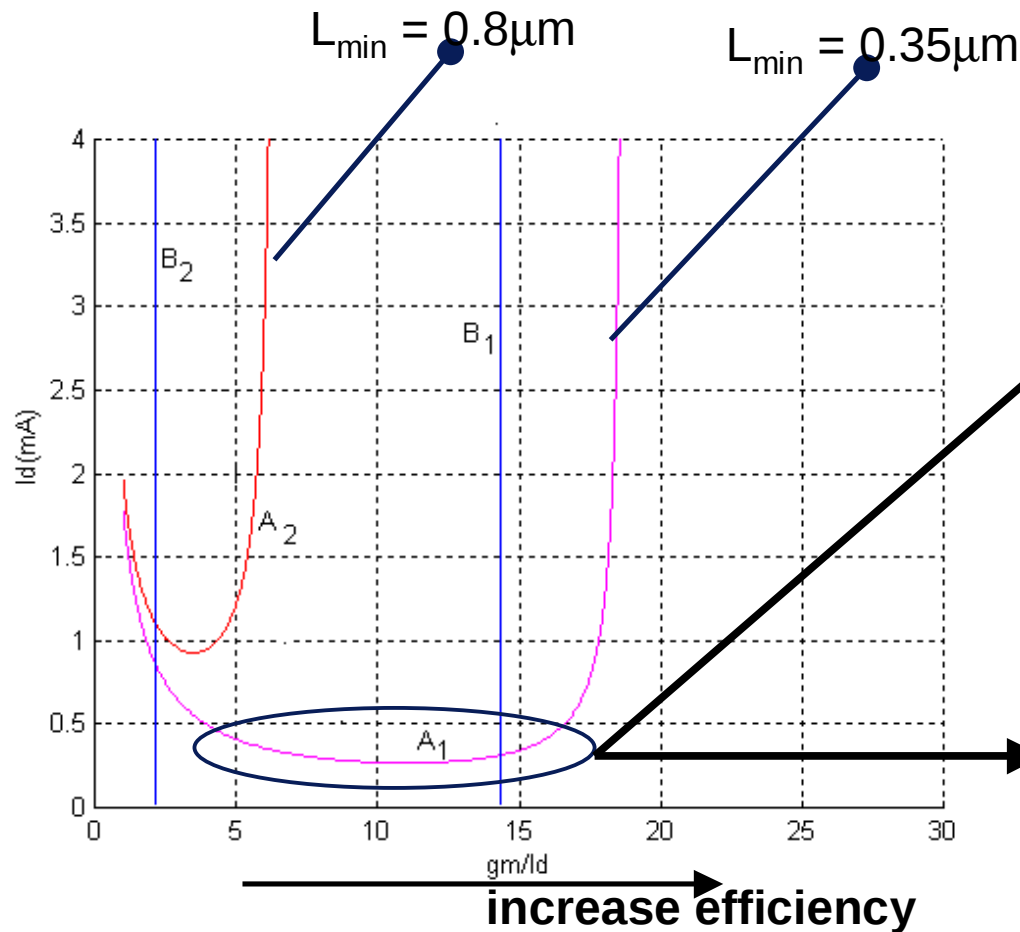
Usenal =

$V_{GS_disponible} = 0.21 \text{ V}$
 $V_{DS_disponible} = 1.30 \text{ V}$
 $Po(\text{dBm}) = -1.73$



II. Ex. (3): Technology comparison

One stage amplifier with $G=2V/V$, $C_L=0.1pF$ and no R_F .

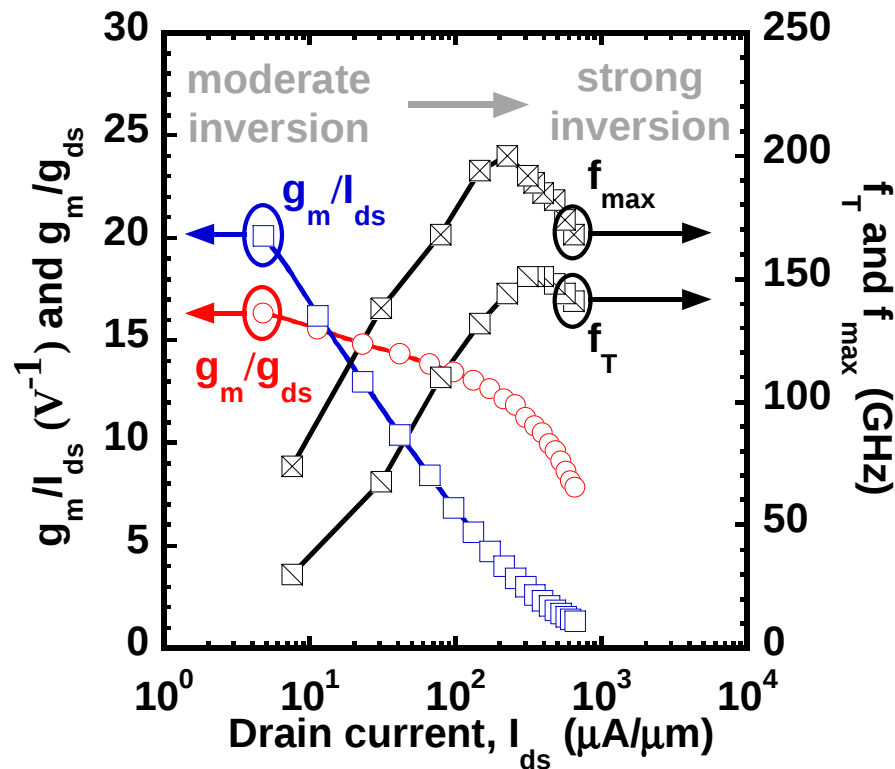


•900MHz is not high frequency for 0.35 μm technology

•Ultra low power consumption techniques (MOS transistor in MI and WI) can be used

It is possible to work optimally in MI and in QS region

II. Other Recent Results:IMEC, 2004, 90nm



Design specification:
 f_{max} and $f_T > 5-10$ times $f_{application}$

Moderate inversion

- Up to 5GHz applications.
- Low power consumption.

Strong inversion

- Up to 20GHz applications.
- Higher power consumption.

* W. Jeamsaksiri et al. **Symposium on VLSI Technology**, June, 2004

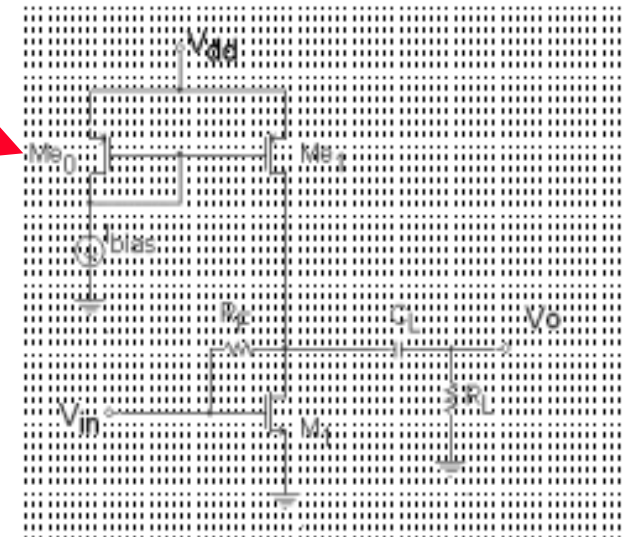
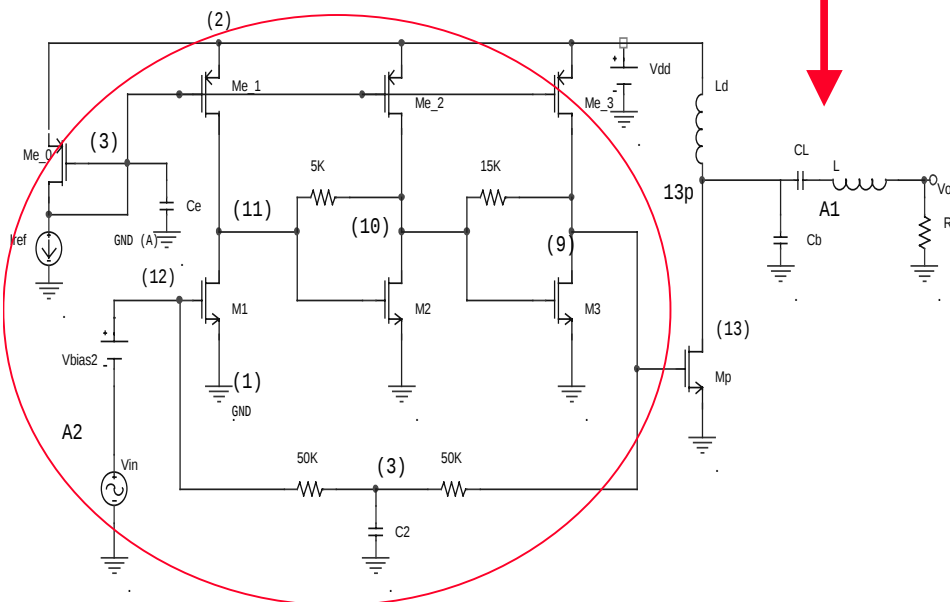
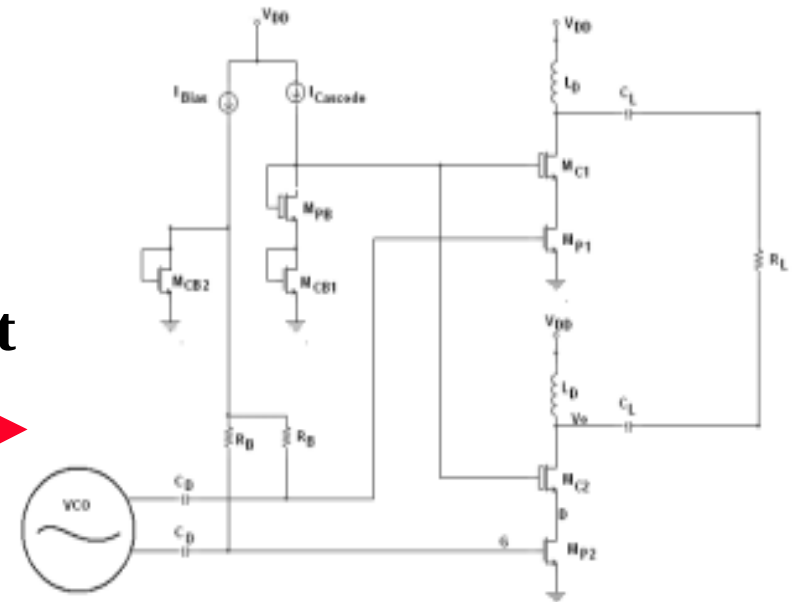
** J. Ramos et al. **ESSDERC**, September 2004

Outline

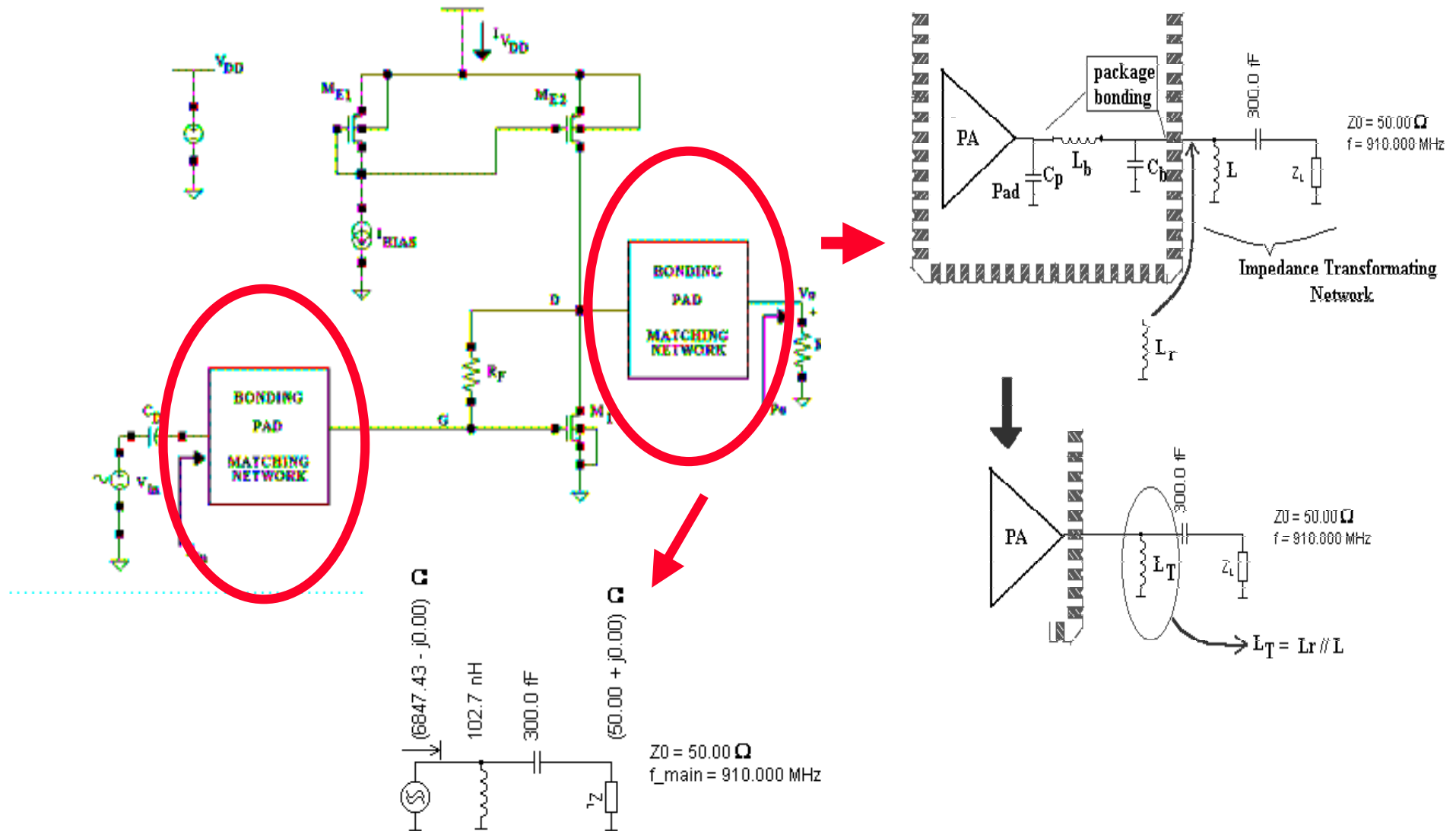
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III. Experimental Prototypes

- ◆ 1- PA of a Low Power Short Range Tx
- ◆ 2- Optimum Amplifier Stage
- ◆ 3- Three Stages Preamplifier

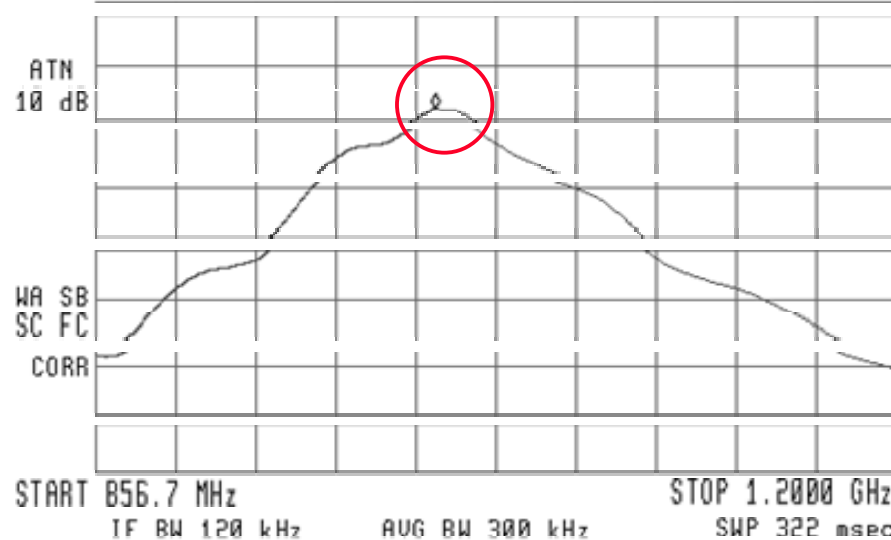


III. Measurement: Optimal Stage



III. Measurement: Optimal Stage

LIN REF -15.0 dBm



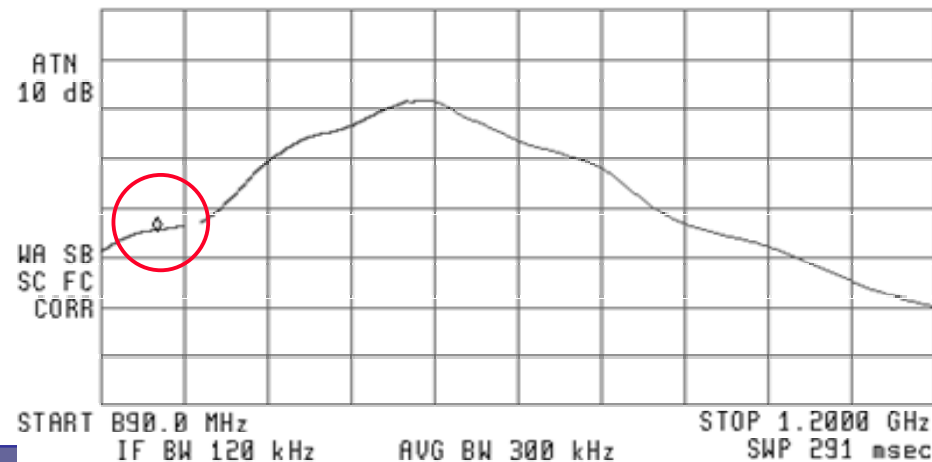
ACTV DET: PEAK

MEAS DET: PEAK QP AVG

MKR 1.0026 GHz

-17.22 dBm

LIN REF -15.0 dBm



ACTV DET: PEAK

MEAS DET: PEAK QP AVG

MKR 910.9 MHz

-22.00 dBm

III. Measurement: Optimal Stage

- ◆ $I_D = 0.50\text{mA}$ estimated, 0.53mA simulated, 0.54mA measured.
- ◆ With Input Power estimated from simulations

	Pout	Gp (Power Gain)
Simulated	-21.78dBm	10.93 dB
Measured	-22.08dBm	10.6 dB
Estimated	-16.10dBm	11 dB

Outline

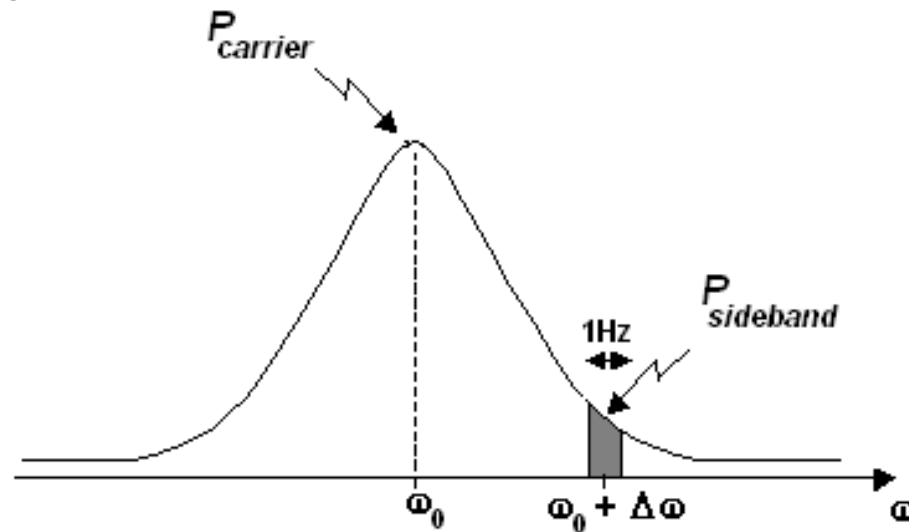
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IV. Phase Noise in LC VCOs

$$V_0(t) = A \cos(\omega_0 t + \varphi) \rightarrow V_0(t) = A(t) \cos(\omega_0 t + \varphi(t))$$

◆ Origin

- Upconversion of the $1/f$ noise and white noise due to a non-linear system

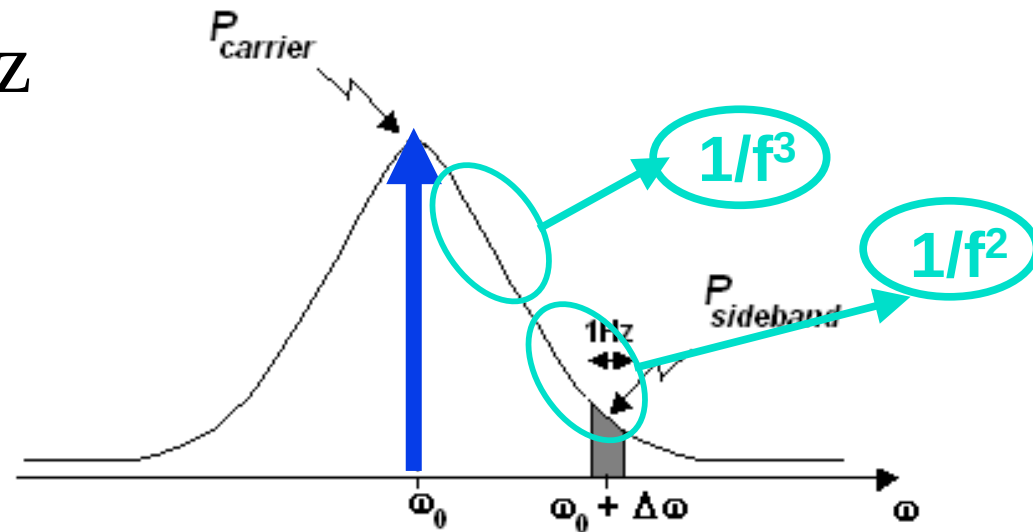


IV. Phase Noise in LC VCOs

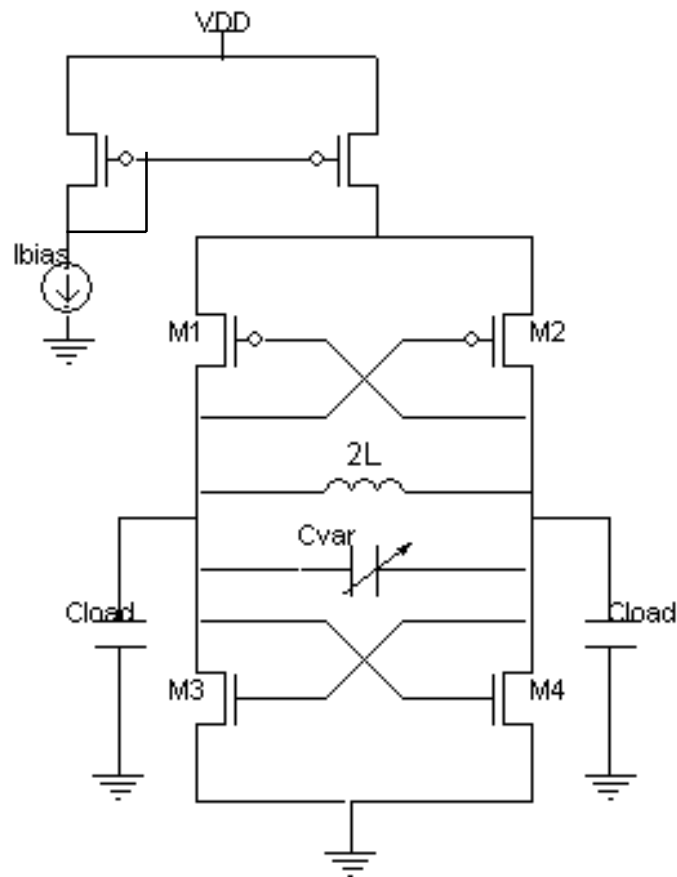
◆ Phase noise definition

$$L(\Delta\omega) = 10\log\left(\frac{P_{\text{sideband}}(\omega_0 + \Delta\omega, 1\text{Hz})}{P_{\text{carrier}}}\right)$$

$$[L(\Delta\omega)] = \text{dBc/Hz}$$



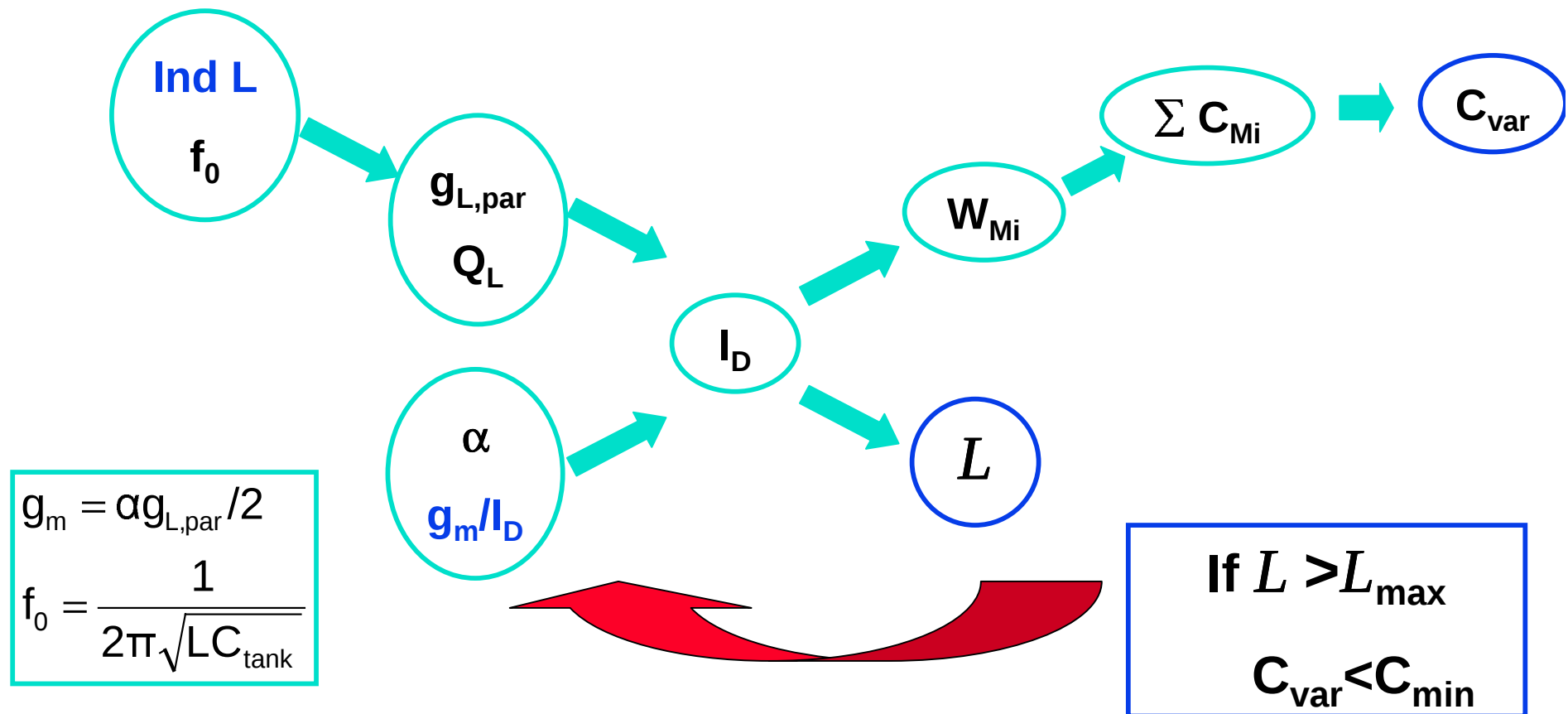
IV.–Gm LC Complementary VCO Circuit



Margin

$$g_m = \alpha g_{\text{tank}}/2$$
$$f_0 = \frac{1}{2\pi\sqrt{LC_{\text{tank}}}}$$

IV. VCO Design Methodology



IV. VCO Design Trade-offs

$Q \uparrow \rightarrow L \downarrow$

$g_m/I_D \downarrow \rightarrow (I_D \uparrow) \rightarrow L \downarrow$

but ... $L \downarrow \div 2$ then $P_d \uparrow \times 2$
(-6dB)

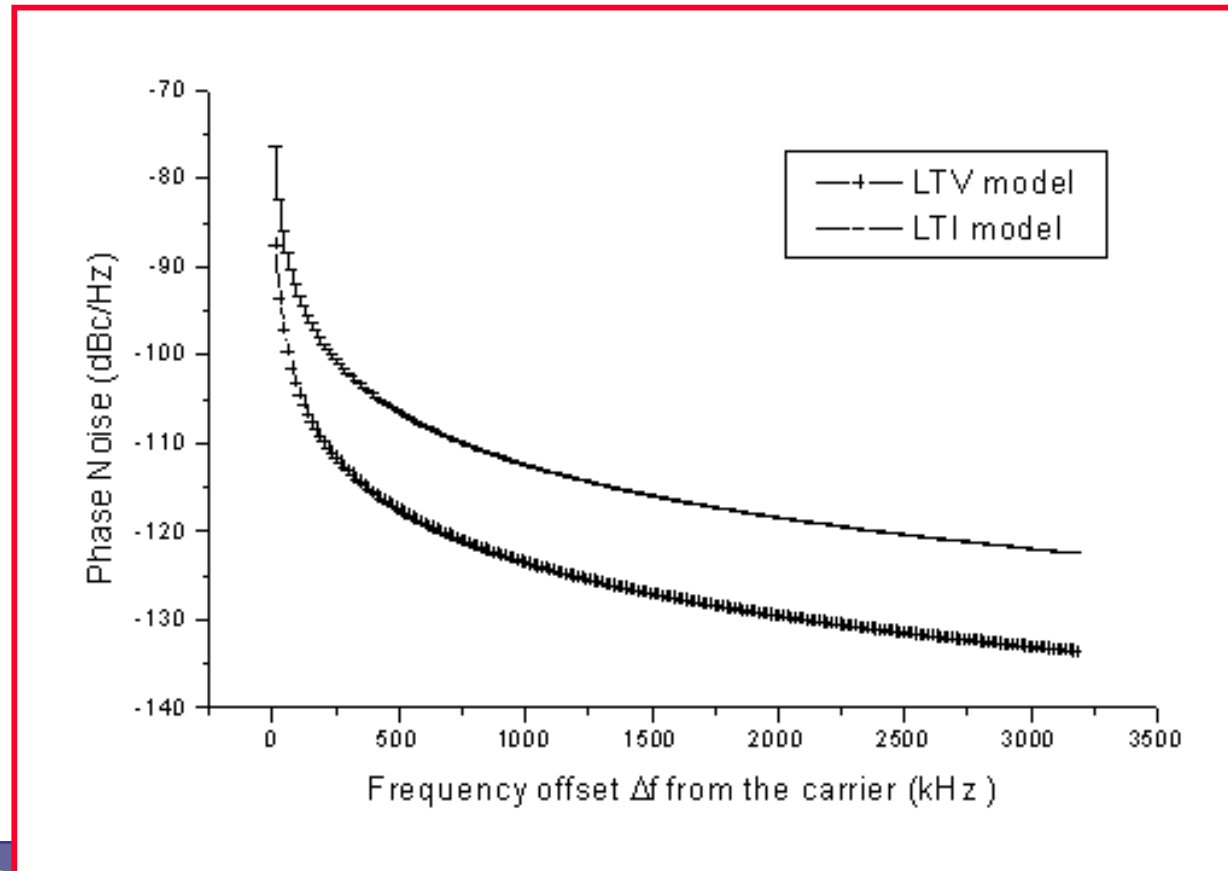
IV. VCO Final Design

Design parameter	Value
L	5nH
g_m/I_D	11
C_{var}	0.7pF
W_n	336 μm
W_p	782 μm

IV. Phase Noise

- ◆ Phase noise models:

- Linear time **invariant** model (LTI) (by Leeson, Proc. IEEE, 1966), Adjustment parameter F.
- Linear time **variant** model (LTV) (by Hajimiri and Lee, JSSC 2000)



IV. Phase Noise

◆ Phase noise obtained from simulation

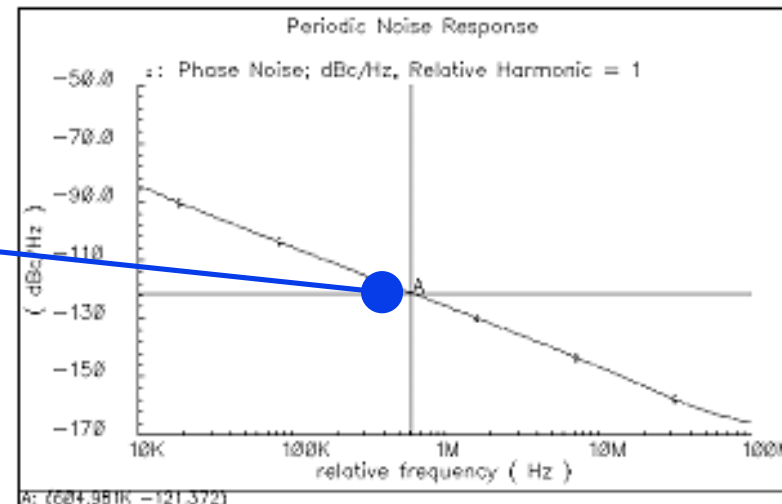
With a Matlab routine:

LTI model	-108dBc/Hz @600kHz
LTV model	-120dBc/Hz @600kHz

Differences
probably due to
factor F

With Cadence:

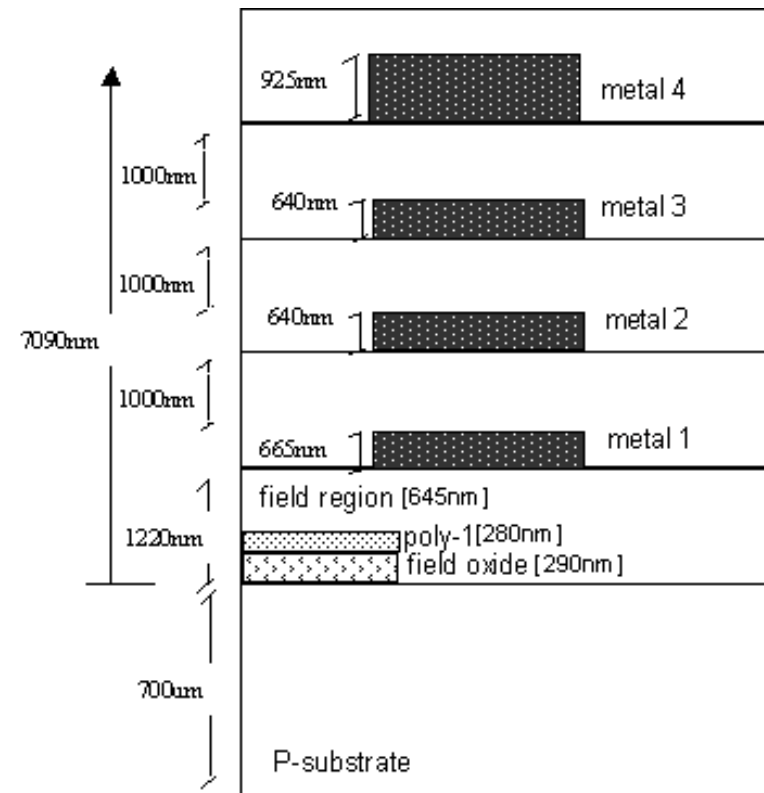
-119dBc/Hz @600kHz



IV. Inductors Design

◆ Characteristics

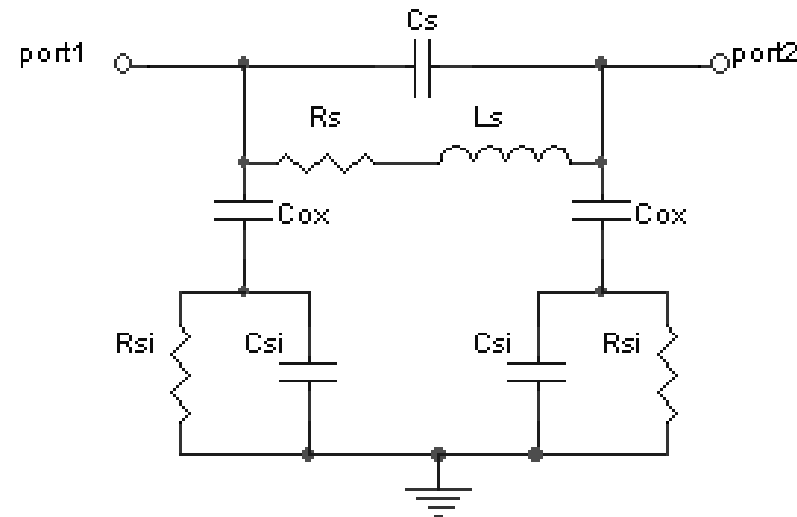
- Inductance value
- Quality factor
- Self resonance frequency
- Area, number of turns and width.
- Dependent on the technology characteristics:
 - » Number of metal layers
 - » Inductor metal thicknesss
 - » Resistivity of the substrate



IV. Inductors Design

- ◆ Modelling
 - Lumped inductor model:
 - » Mohan's inductance expressions
 - » Yue's model

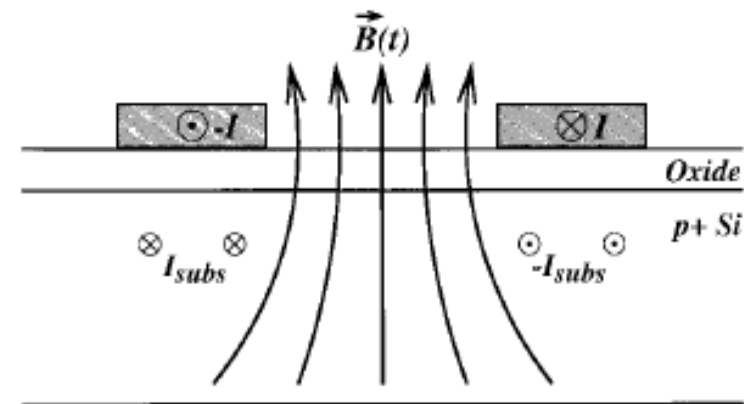
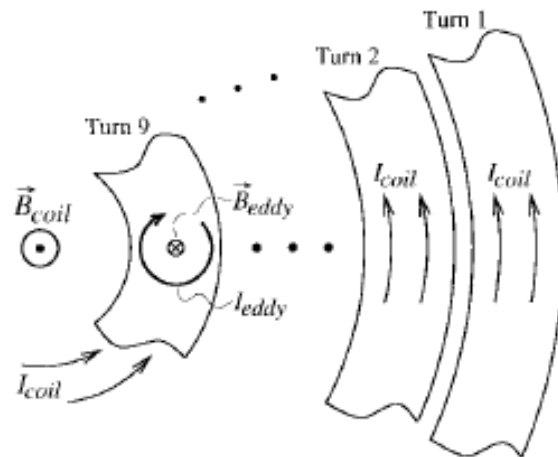
$$Q_L = \frac{\omega_0 L_s}{R_s}$$



π net

IV. Inductors Design

- ◆ Inductor losses
 - Metal losses
 - » Skin effect
 - » Eddy currents in the winding
 - Substrate losses
 - » Eddy currents in the substrate



IV. Inductors Design

◆ Final inductor design

Geometry	Square
Metal	Top metal
Number of turns	4
W	14 μ m
s	1.5 μ m
d _{out}	260 μ m



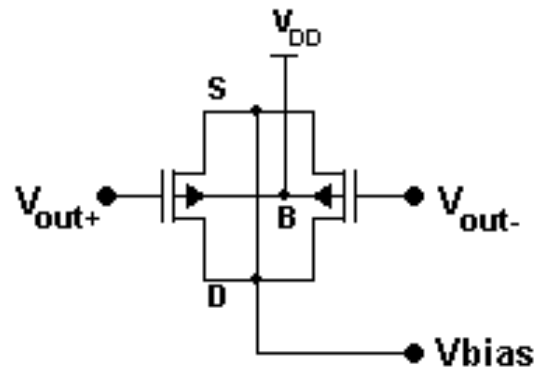
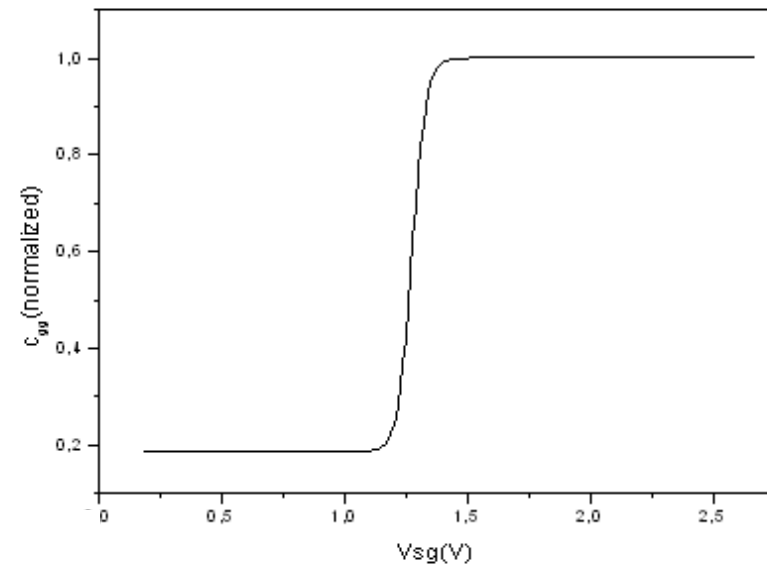
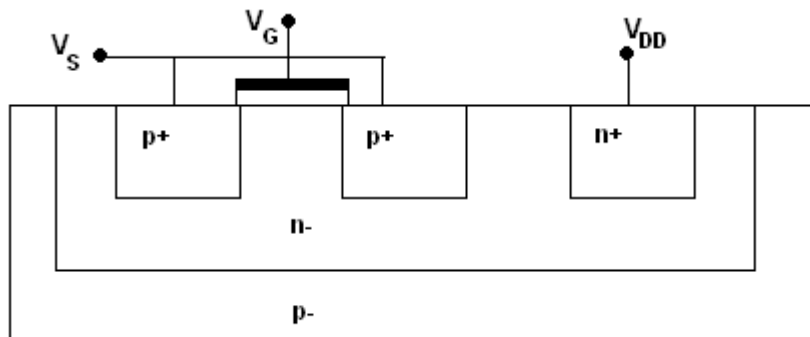
L(nH)
Rs(Ω)
Cs(fF)
Cox
Q

**Characteristics
calculated with 3
tools:**

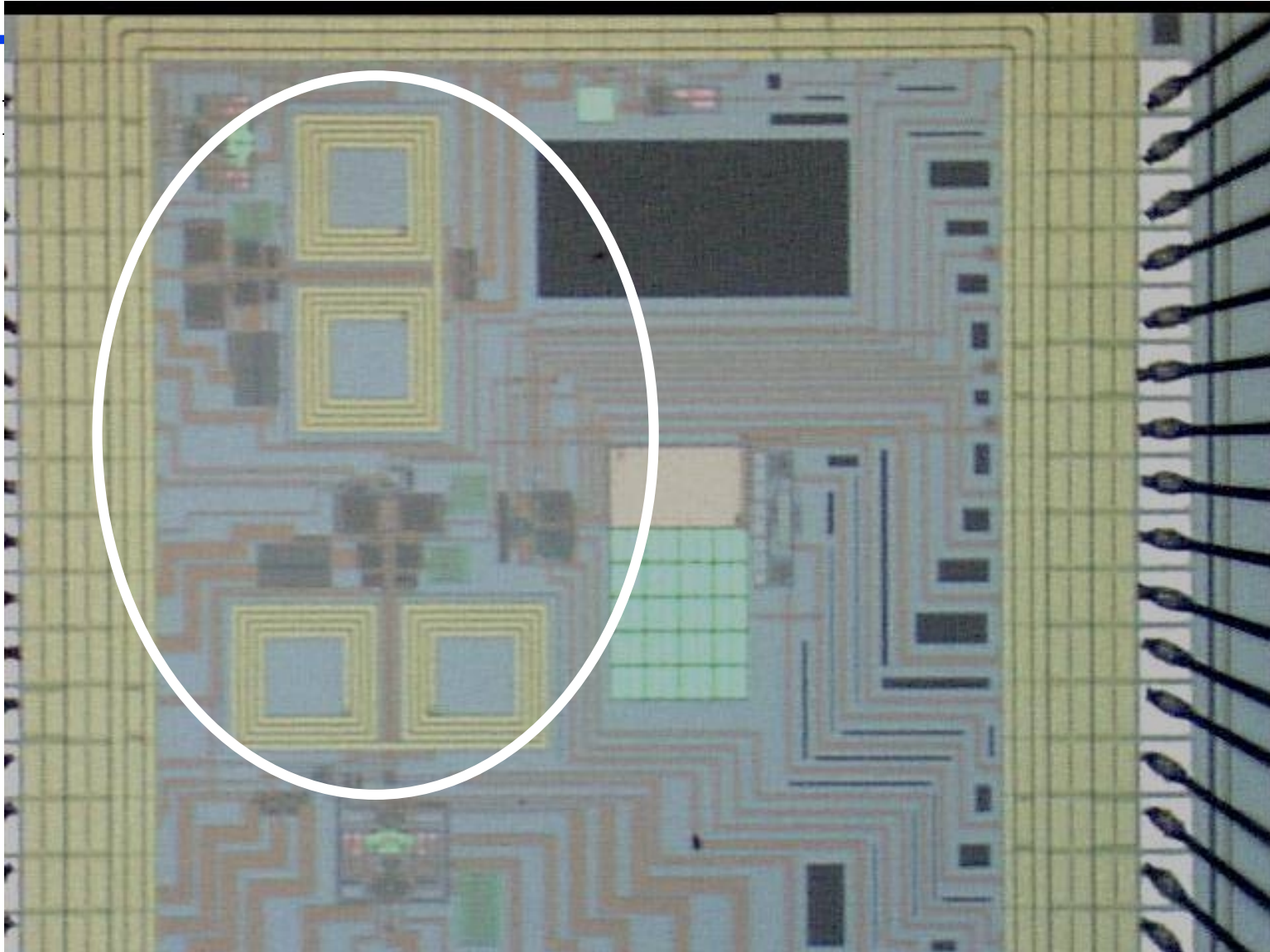
- Matlab
- ASITIC
- Cadence

IV. Varactor

◆ Inversion Mode MOS

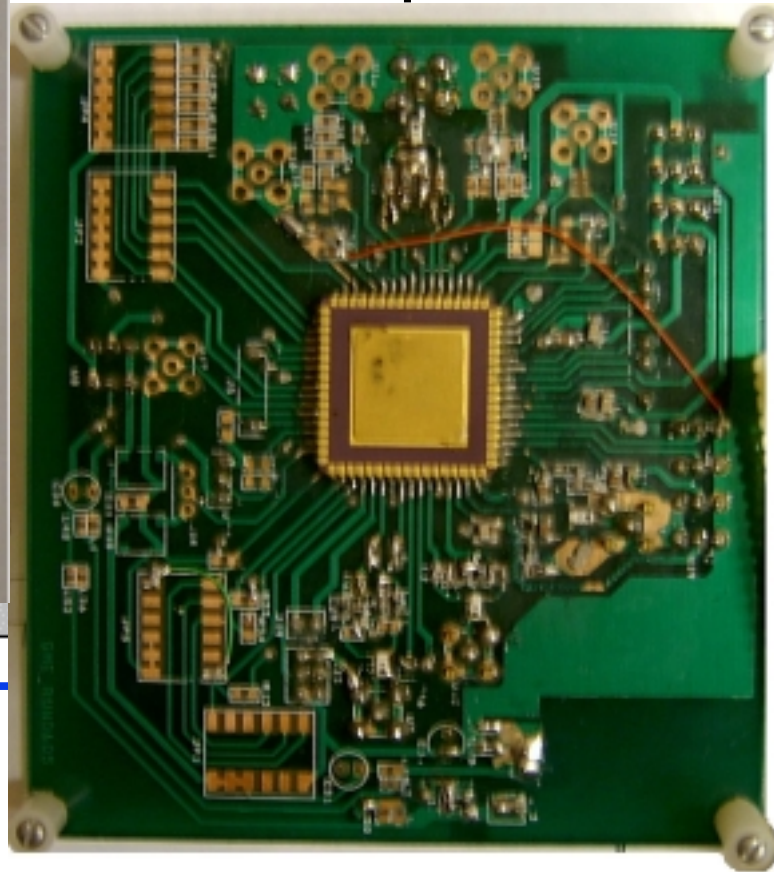
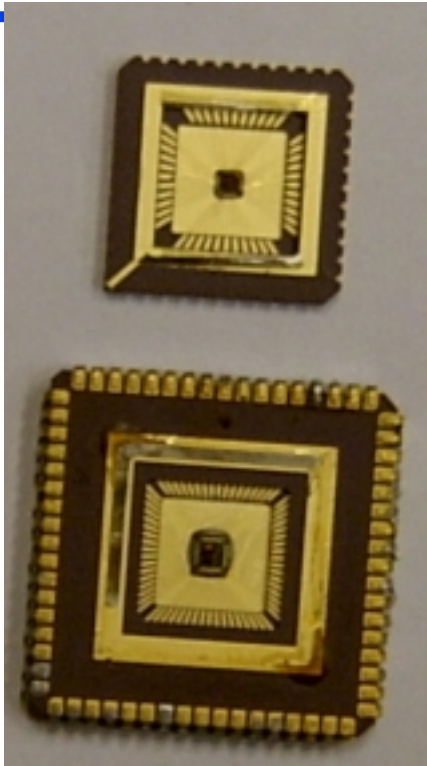


IV. VCO Layout



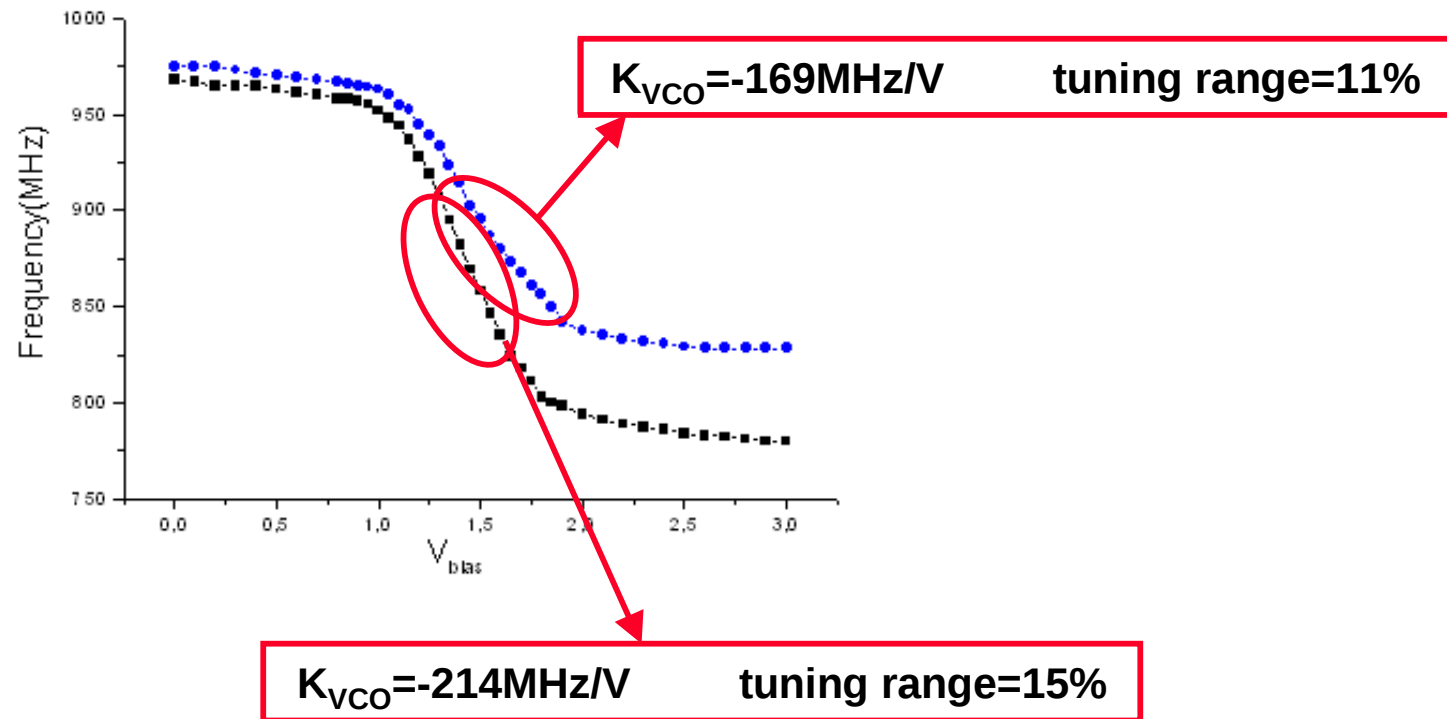
IV. VCO Measurements

ement setup



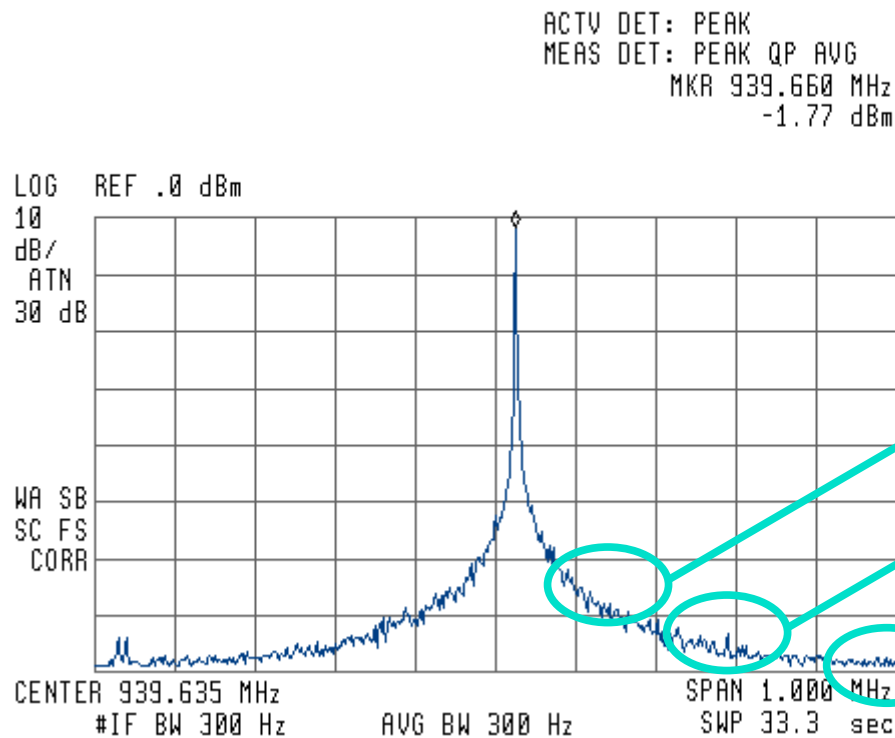
IV. VCO Measurements

- VCO oscillation frequency versus V_{bias}



IV. VCO Measurements

- PSD and phase noise



@ $I_{DD} = 3\text{mA}$, $V_{DD}=3\text{V}$

$L @ 100\text{kHz} = -87\text{dBc/Hz}$
 $L @ 600\text{kHz} = -102\text{dBc/Hz}$
 $L @ 1\text{MHz} = -107\text{dBc/Hz}$

V. Conclusions

- ◆ Inversion level that gives an optimum consumption for a given gain.
- ◆ Matlab tool which helps in the design of low power RF blocks.
- ◆ Feasibility of working in moderate inversion at 910MHz in 0.35 μ m technology. Experience in ultra low power analog design may be reused here.
- ◆ VCO: Moderate inversion provides a good compromise between phase noise and consumption.
- ◆ Layout wiring parasitics and package parasitics strongly affect performance

Thank you !