Introducción a VLSI

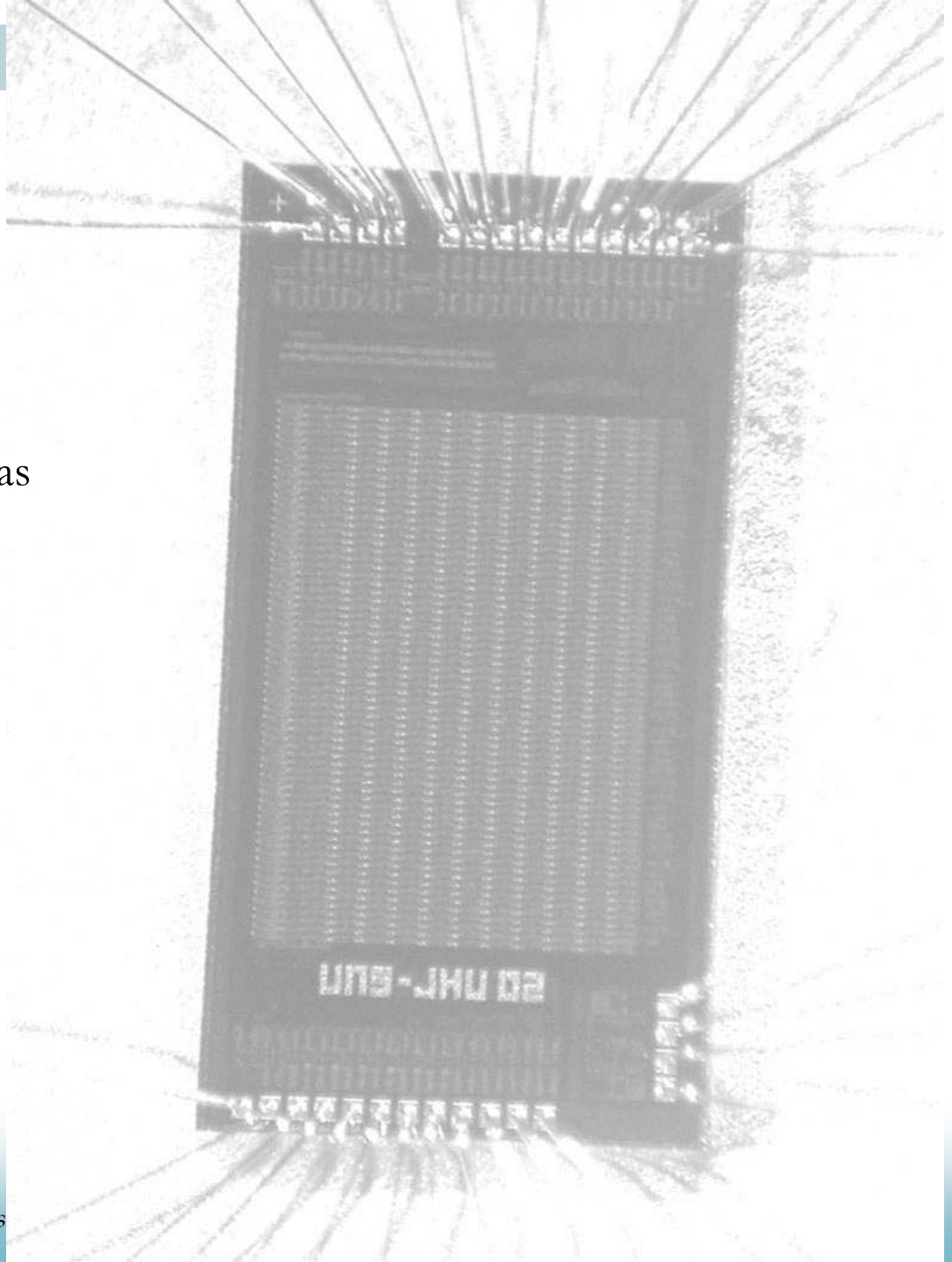
EAMTA 2006

Introducción a VLSI

Clase 2: Layers y layout

Programa

- El Transistor MOS
- **Layers y Layout**
- Lógica Combinacional
- Lógica Secuencial y Subsistemas

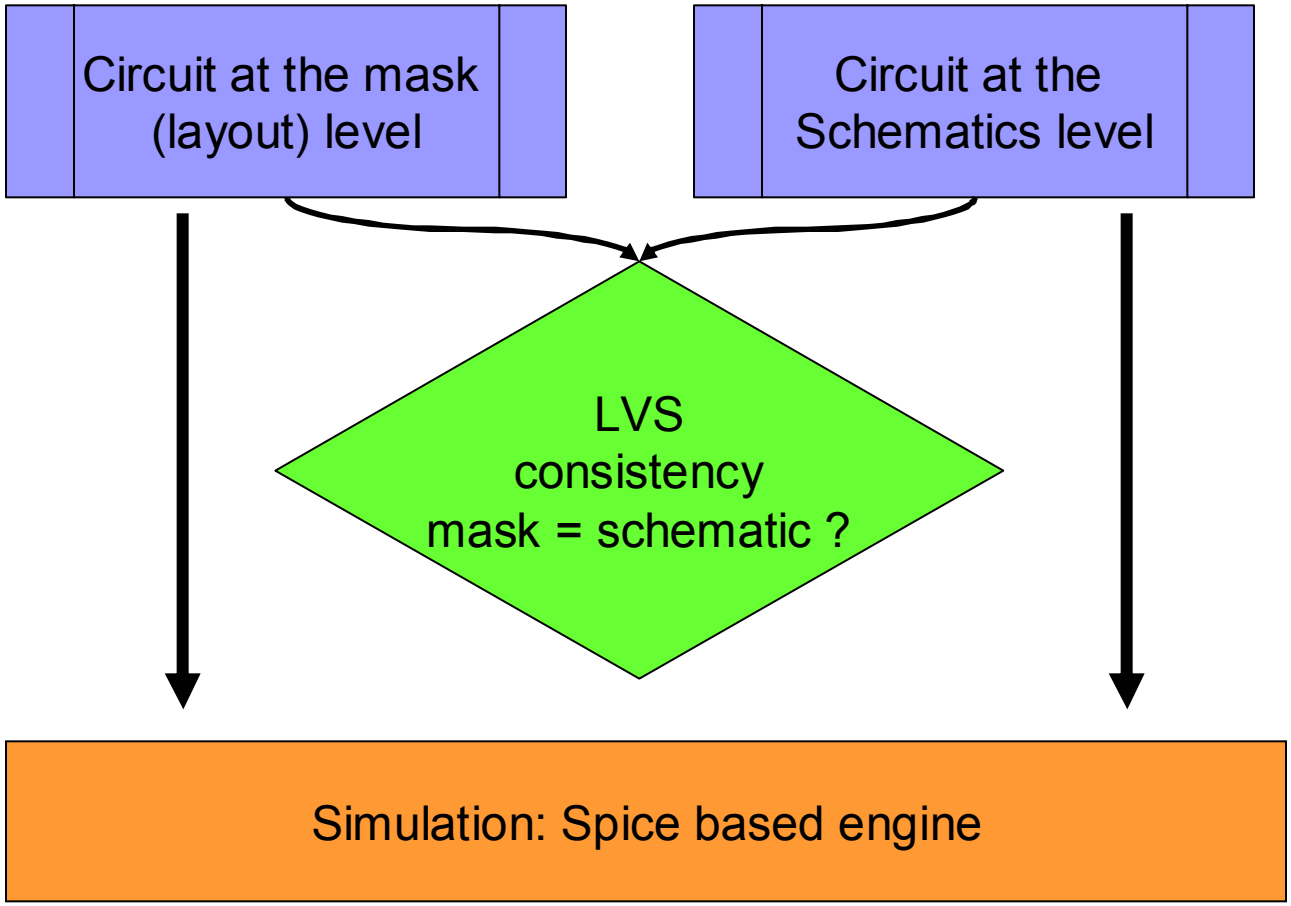


Organización

- Elementos de Software de diseño
- Layers de Procesos
- Reglas de diseño
- Layout de transistores MOS
- Capacidades de un transistor MOS

Elementos de software de diseño

Elementos de Software de Diseño



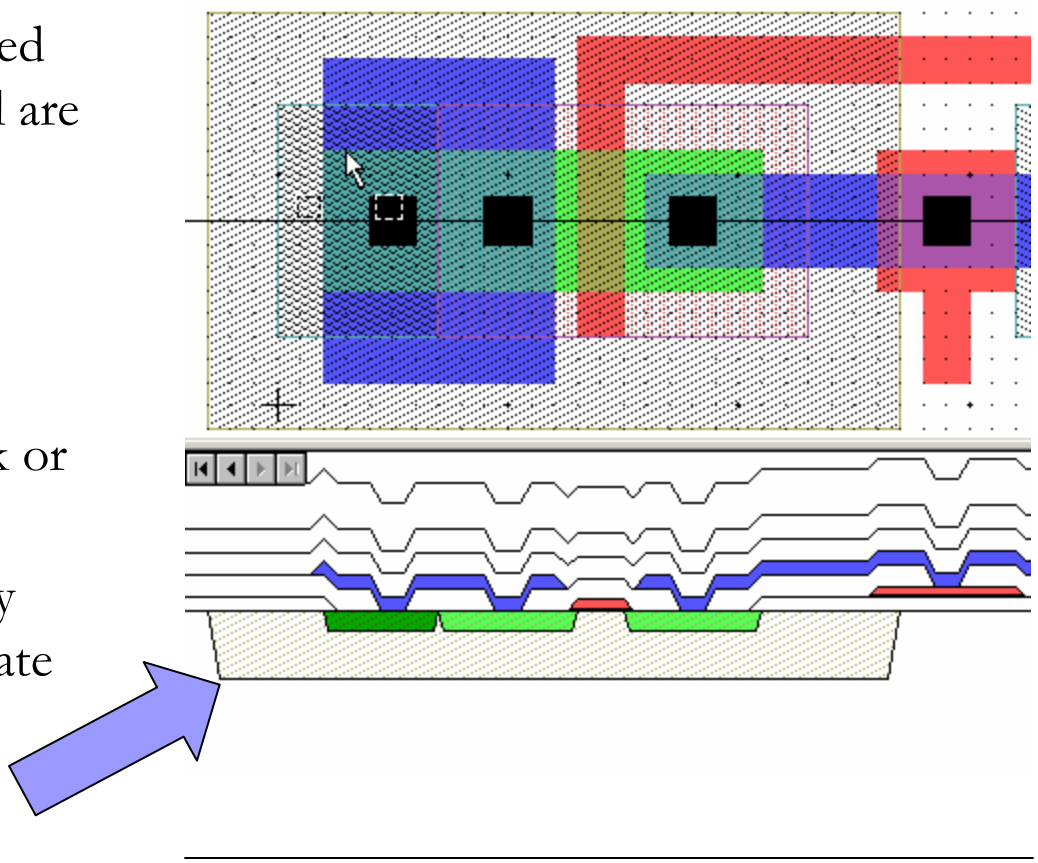
Layers de un Proceso

Layers de un Proceso

- Layer de Nwell
- Layer Activo
- Difusiones (N y P)
- Poly
- Metales

N-Well

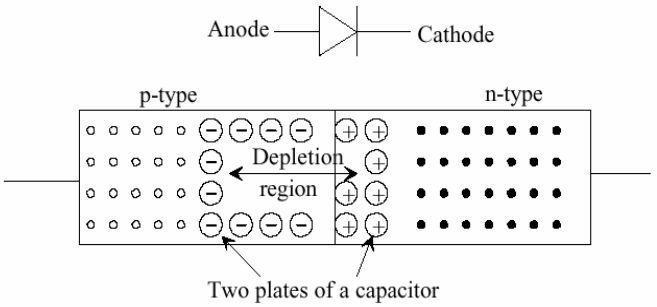
- Assuming a p-type wafer, n-channel transistors are fabricated directly in the wafer; p-channel are fabricated in an "n-well"
- Processes with n-well over p-substrates are called n-well processes
- Substrate is also known as bulk or body
- N-well forms a diode (normally reverse biased) with the substrate



N-well: diode capacitance

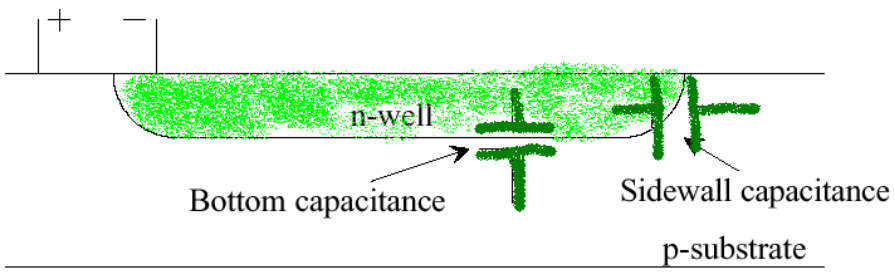
- When the diode is reverse-biased (typical situation)

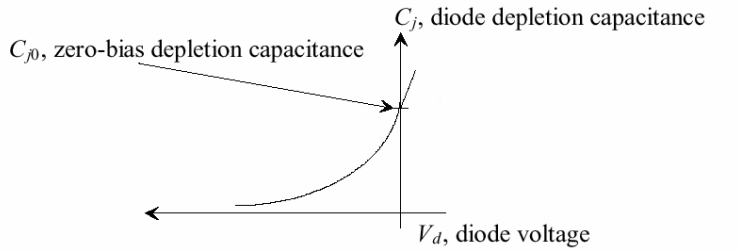
$$C_j = \frac{C_{j0}}{\left(1 - v_d/\varphi_0\right)^m}$$



$$\varphi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

- Two components: bottom capacitance and sidewall capacitance





$C_{j0} = C_{j0b} + C_{j0s}$ $\quad C_{j0b} =$ Capacitance per area × bottom area

$C_{j0s} =$ Capacitance per area × depth of well × perimeter

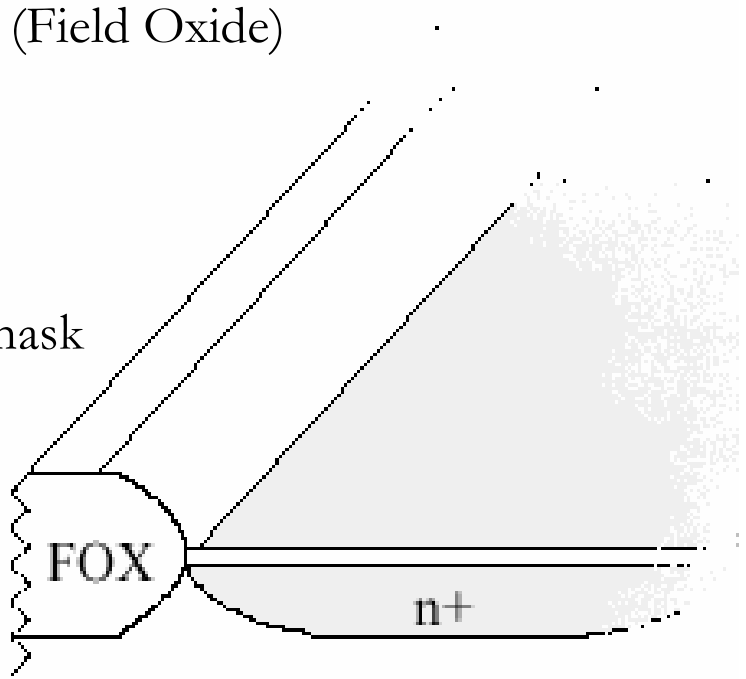
Active and Diffusion Layers

- Active layers, both n+ and p+ are used to make the source and drain of MOSFET's
- Active defines the oxide mask where doping will take place: Regions outside Active have FOX (Field Oxide)

2	Active	Active	

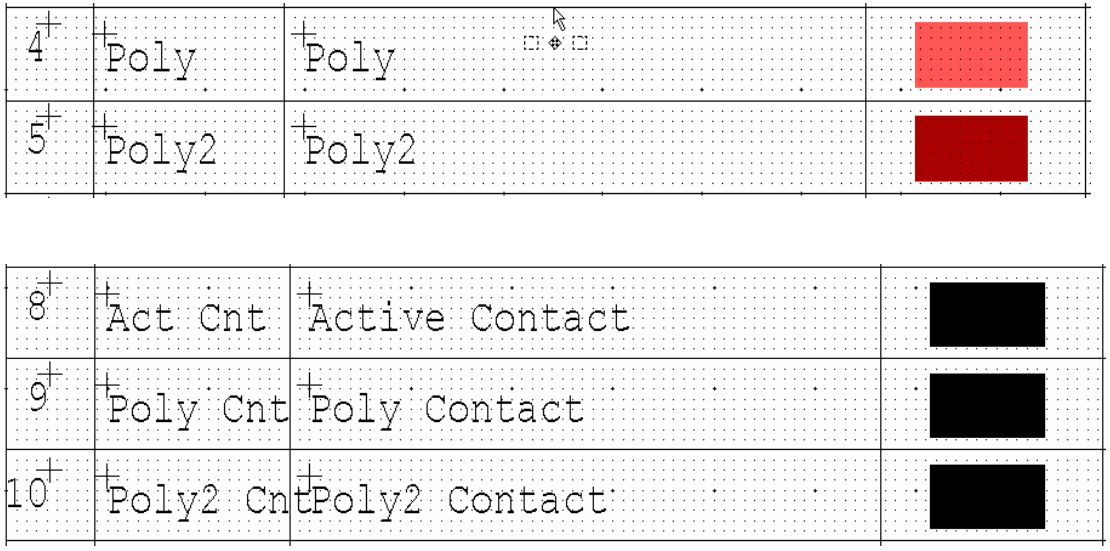
- N select and P select define the doping mask

6	N Select	S/D N+ Implantation	
7	P Select	S/D P+ Implantation	



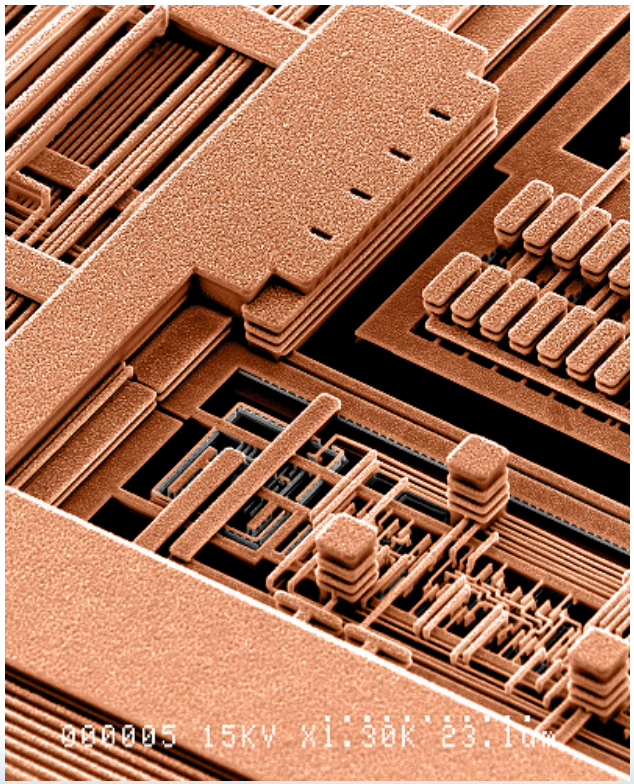
Poly Layer

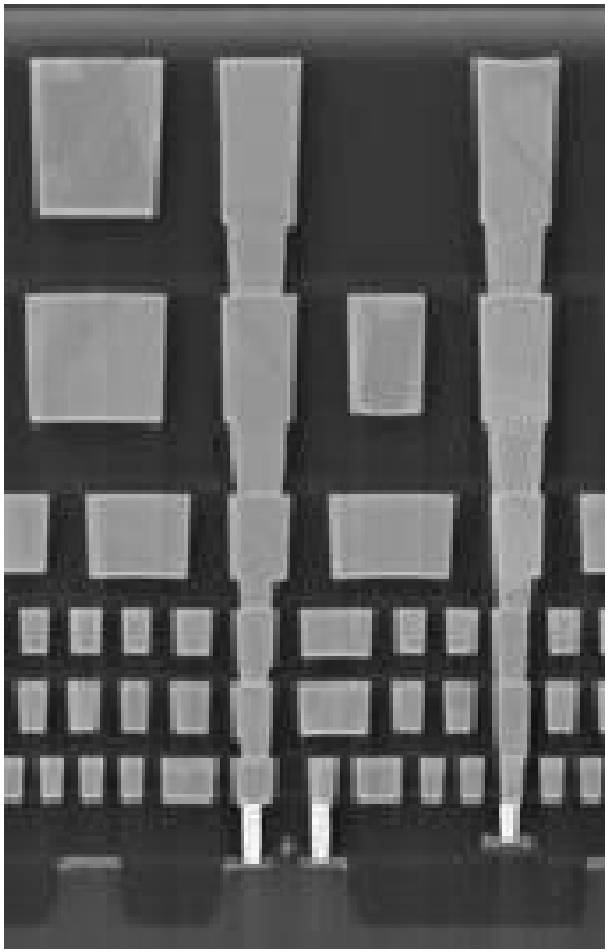
- Polysilicon is made up of small crystalline regions of silicon
- Poly is used for the gates of MOS transistors
- They can make resistors and local connections for transistors



Metal layers

- Metal layers are used to interconnect devices (transistors, resistors, inductors and capacitors)
- Vias are used to interconnect the different metal layers

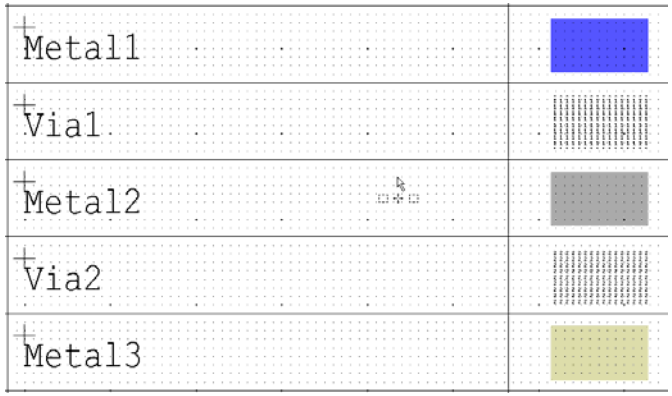




Metal parasitics: R

- Resistance

	M1	M2	M3
Rs	0.09Ω/□	0.09 Ω/□	0.05 Ω/□

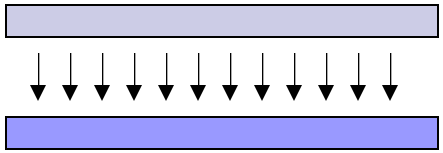


- A line of minimum width and 1mm long (1100 and 666 □ long, resp.)

	M1	M2	M3
Rs	100 Ω	100 Ω	33 Ω

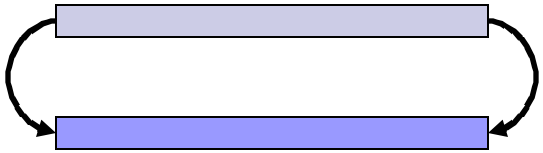
Metal parasitics: C

- Area capacitance (all values in aF/μm^2)



	M1	M2	M3
substrate	32	16	10
M1		31	13
M2			31

- Fringe capacitances (all values in aF/μm)

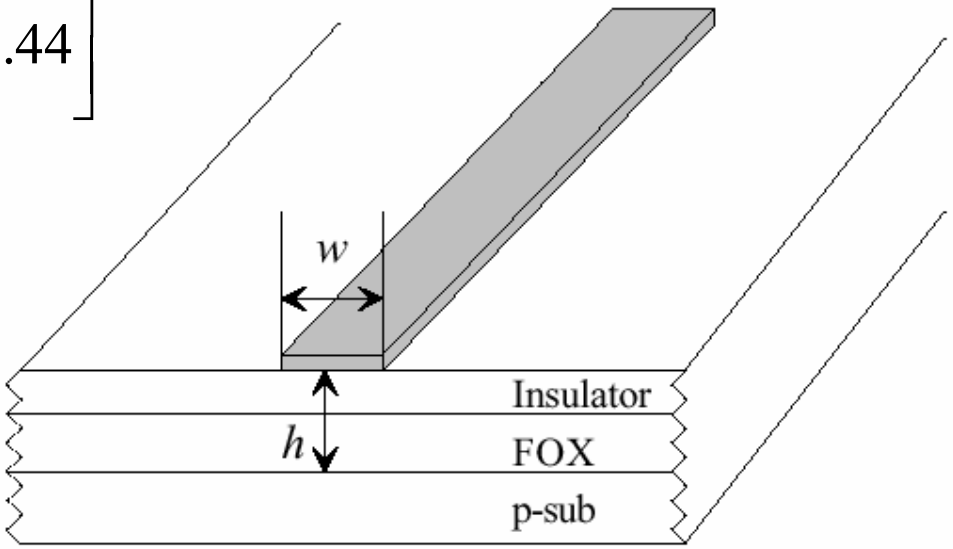


	M1	M2	M3
substrate	76	59	39
M1		51	33
M2			52

Metal Parasitics: L

- A metal line exhibits an inductance that can be estimated as:

$$L = \frac{1.25}{\frac{w}{h} + 1.393 + 0.667 \ln\left[\frac{w}{h} + 1.44\right]} \quad (nH/mm)$$

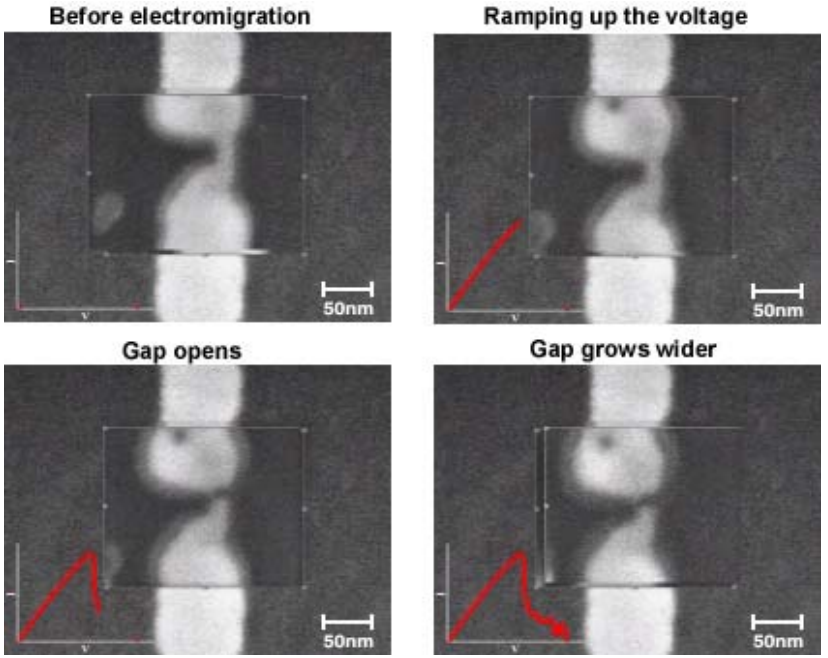


- Assumption: w > h

Metal: Current Capacity

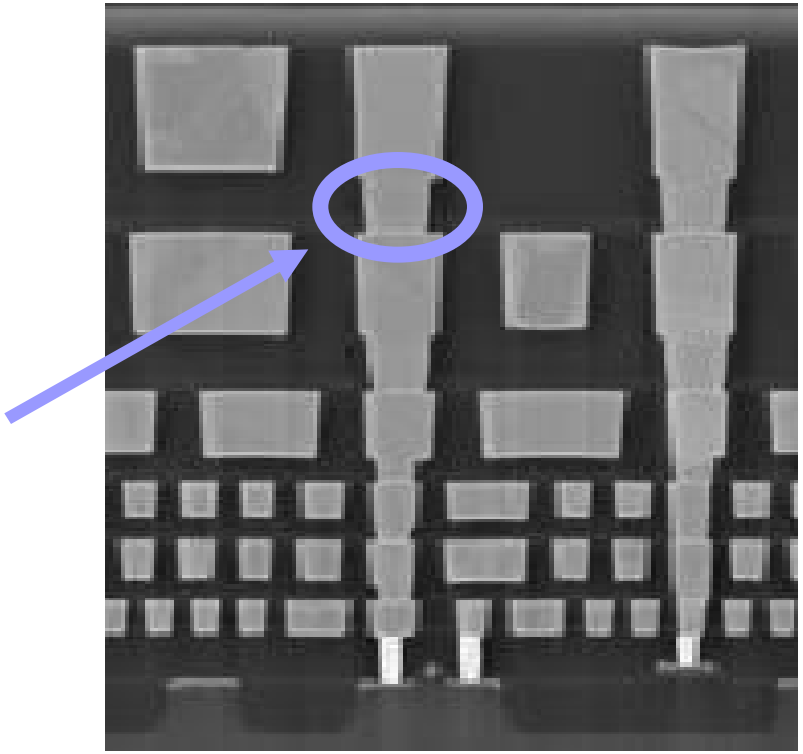
- Due to electromigration wires can be damaged
- For Aluminum, the maximum current density (rule of thumb) is:

$$1\left[\frac{mA}{\mu m}\right]$$



Vias

- Connection between different metal layers
- Can be stackable in modern processess
- Vias exhibit a contact resistance given by the process
- They also have a current limitation given by the electromigration phenomenom. Typically, 0.5mA/cnt

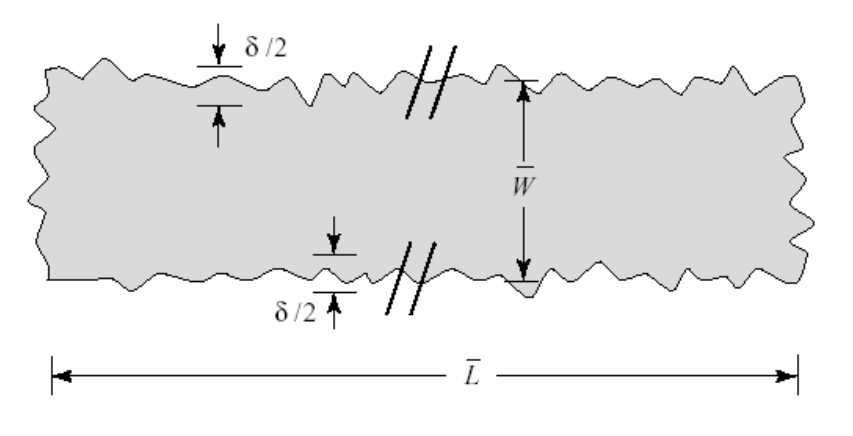


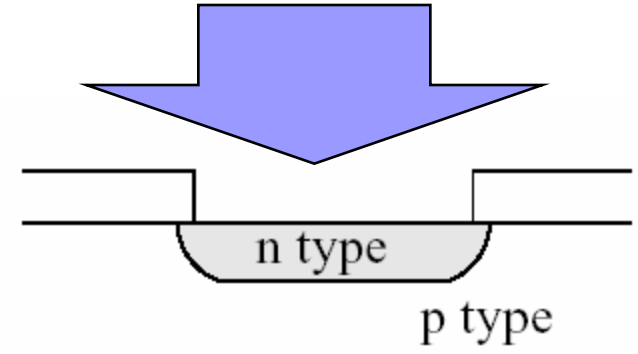
	P+	N+	Poly	M1	M2	M3
Contact R [Ω]	126	57.5	16	□	0.82	0.79

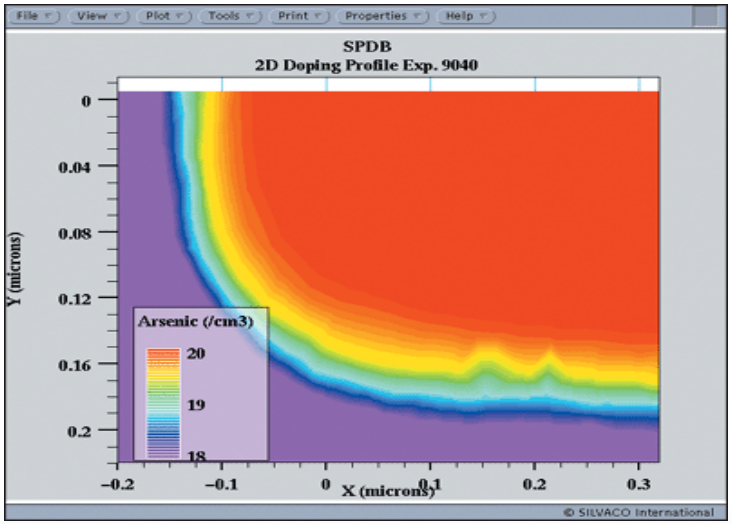
Design Rules

Reglas de Diseño

- Necesidad
  - Proceso fotolitográfico tiene imprecisiones
  - Sucesivos pasos de procesos fotolitográficos tienen errores de alineación
  - Difusiones se extienden más allá de los límites







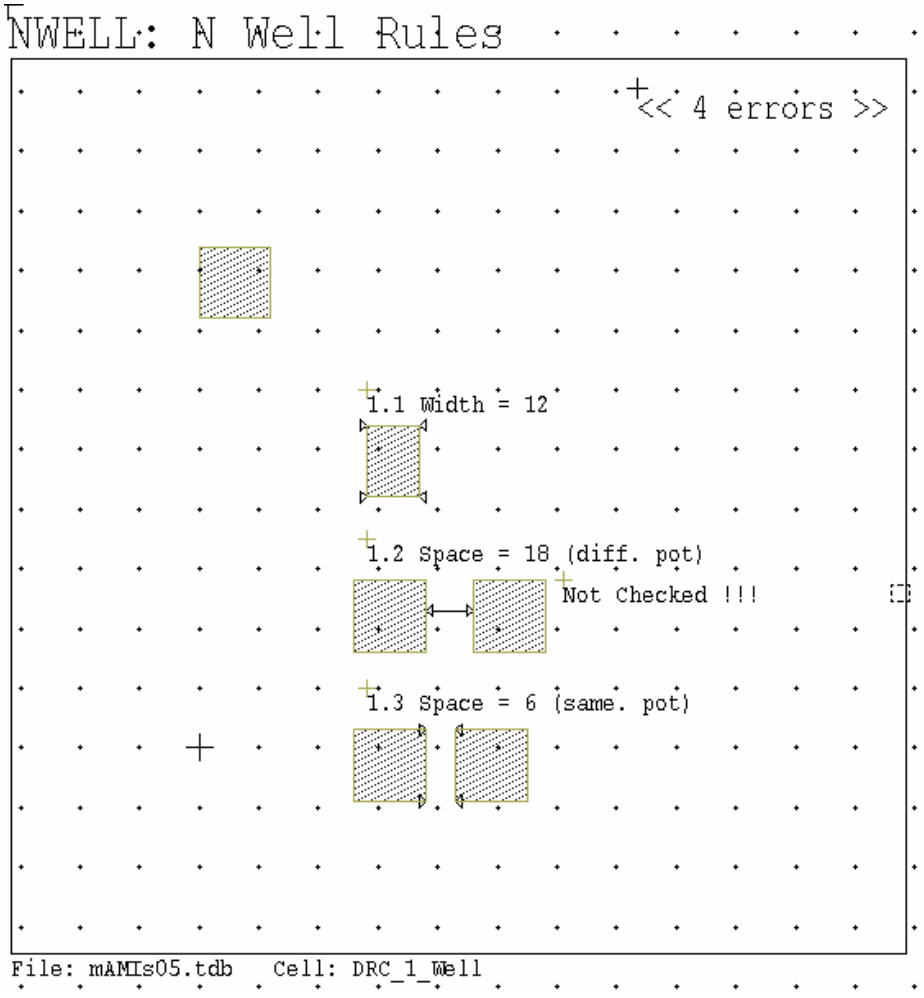
Scalable Design rules (SCMOS)

- Scalable CMOS (SCMOS) is a set of logical layers together with their design rules
  - process- and metric-independent interface to all CMOS processes
- The designer works in the abstract SCMOS layers and metric unit ("lambda").
- In the SCMOS rules, circuit geometries are specified in the Mead and Conway's lambda based methodology [1].
  - Unit of measurement: lambda

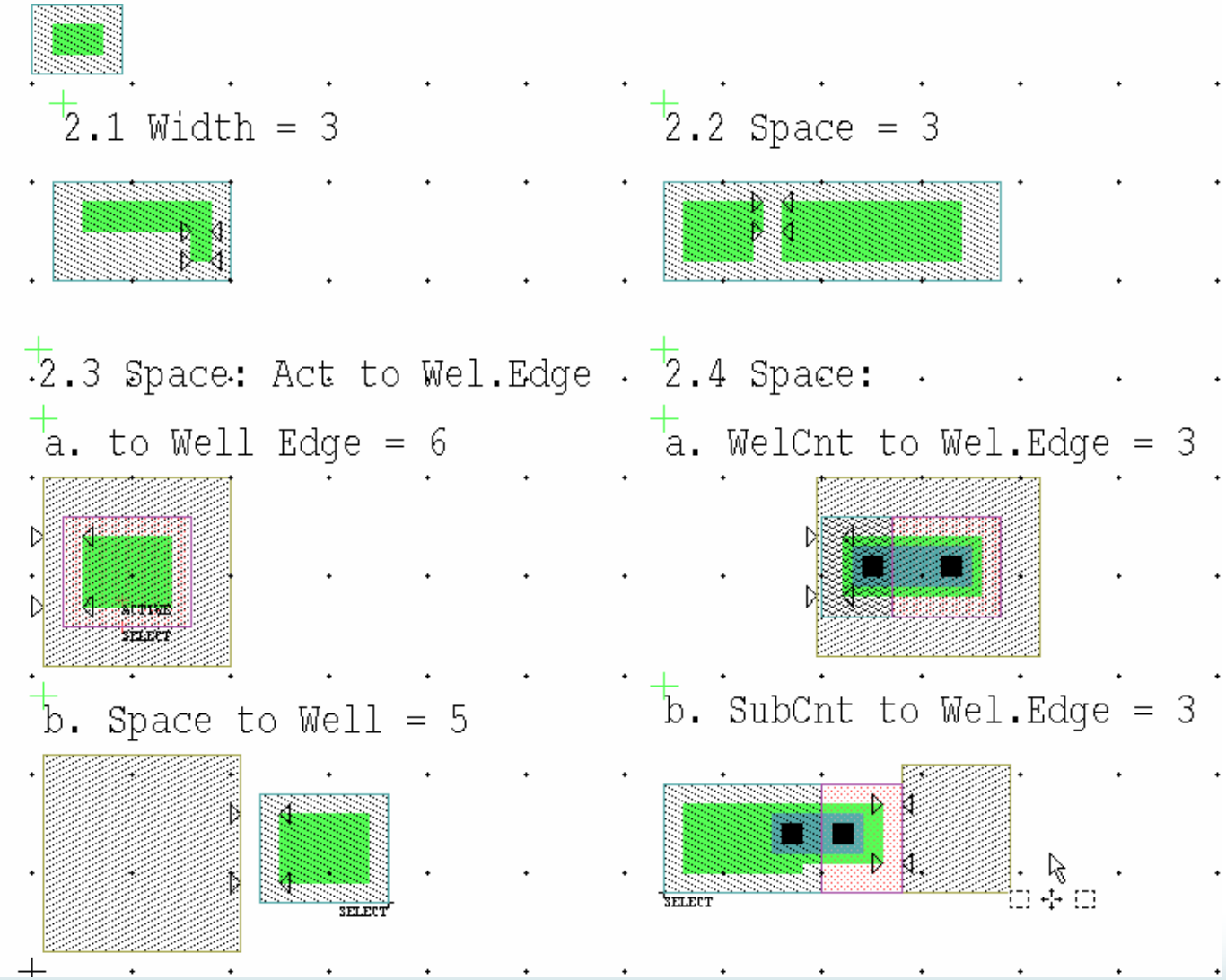
Reglas de diseño

- Hay varios tipos de reglas de diseño
  - Reglas de separación
  - Reglas de tamaño mínimo
  - Reglas de tamaño exacto
  - Reglas de cubrimiento (overlap)

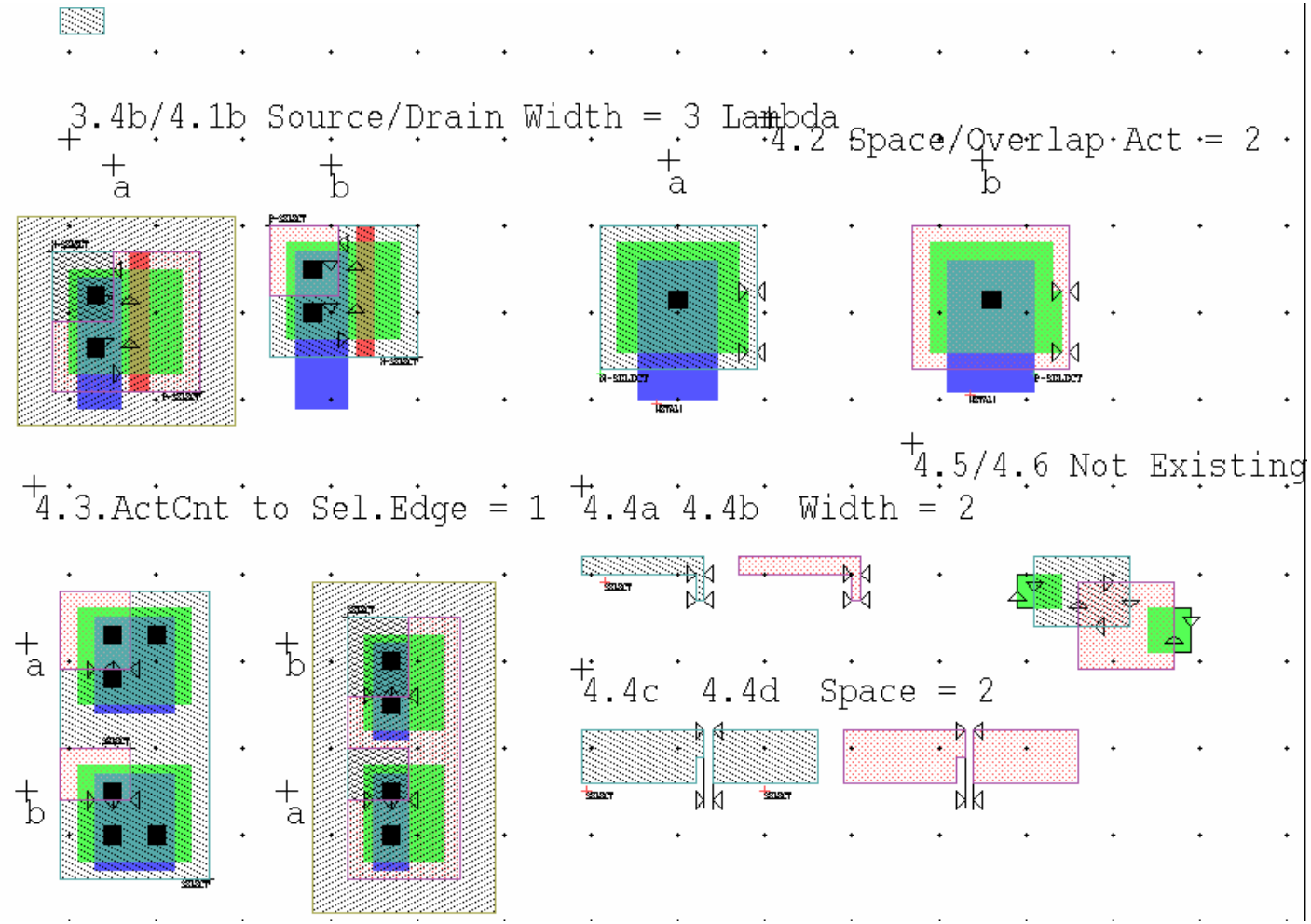
N-Well: Design rules



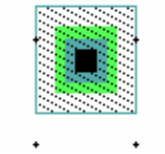
Act Design Rules



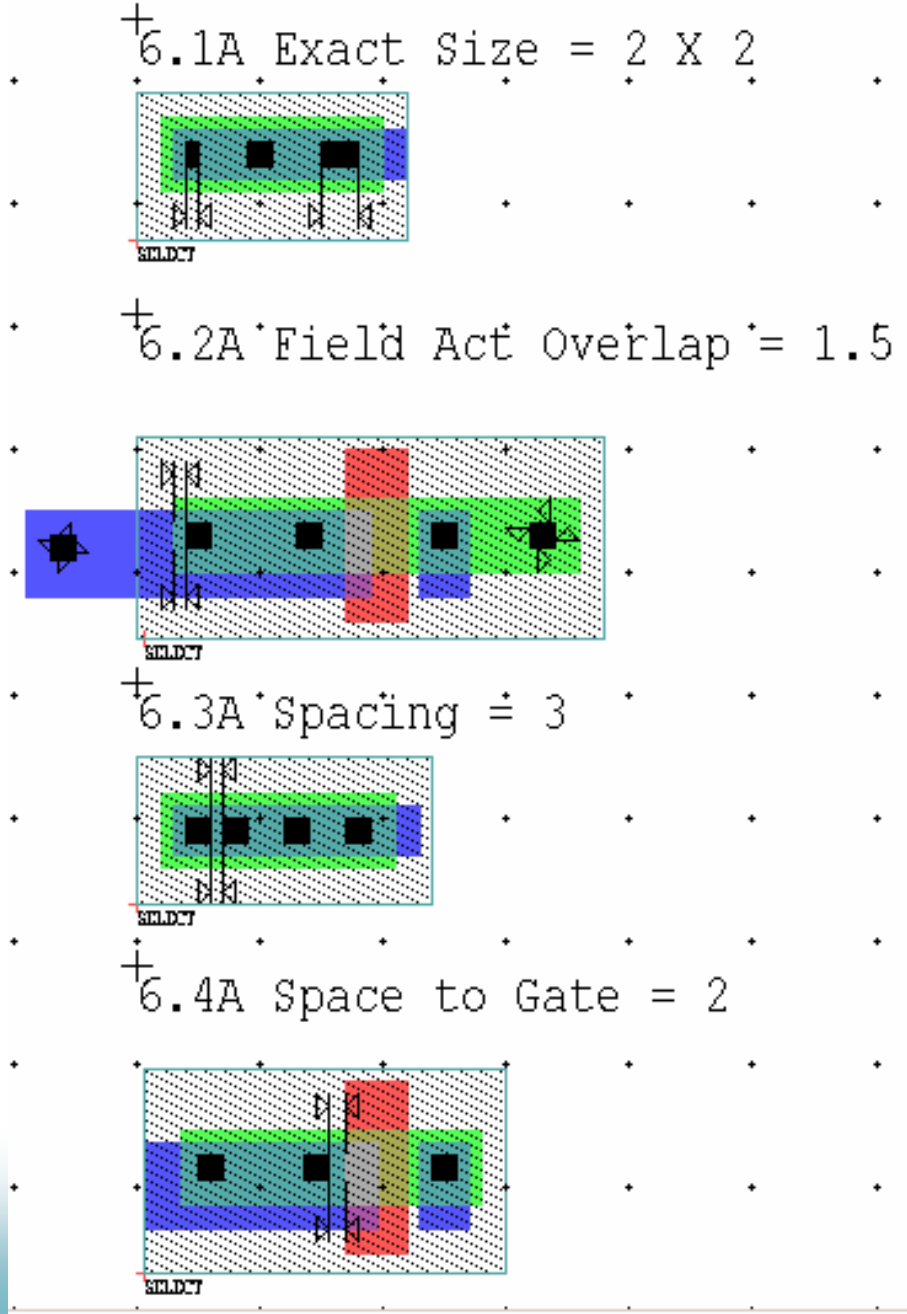
N+ and P+ rules


3.4b/4.1b Source/Drain Width = 3 Lambda
4.2 Space/Overlap Act = 2
a
b
a
b
4.5/4.6 Not Existing
4.3.ActCnt to Sel.Edge = 1
4.4a 4.4b Width = 2
a
b
b
a
4.4c 4.4d Space = 2

Act contact rules

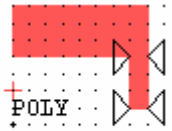


- In this case, there is a special contact to join metal and active

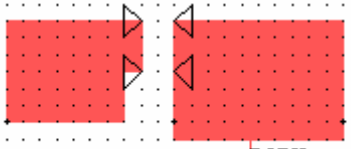


Poly rules

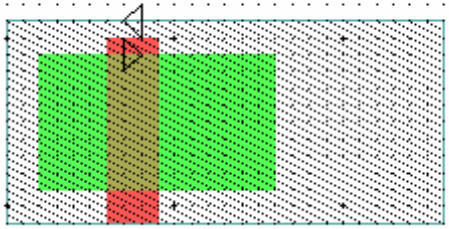
3.1 Width = 2



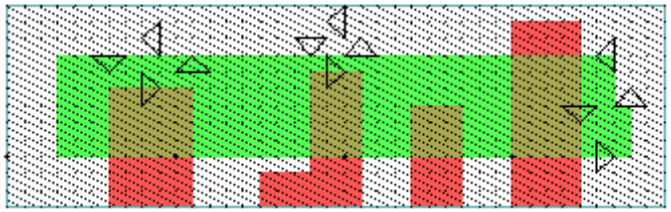
3.2 Space = 2



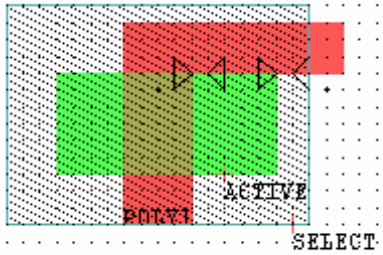
3.3 Gate Extend out Act =2



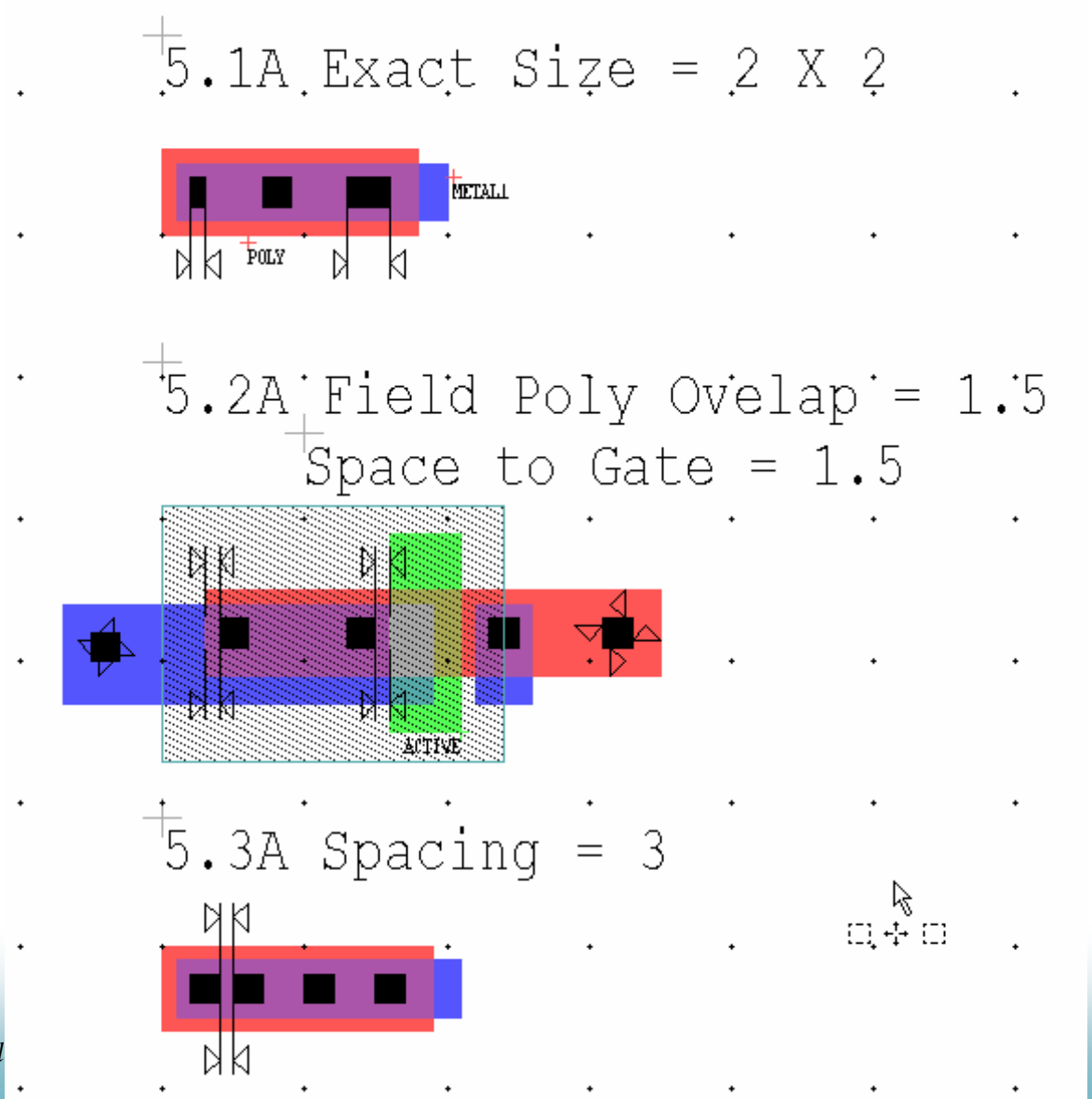
3.4 Source/Drain Width = 3



3.5 Poly to Act Space = 1

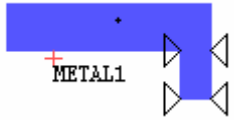


Poly contact rules

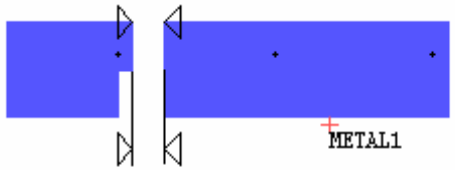


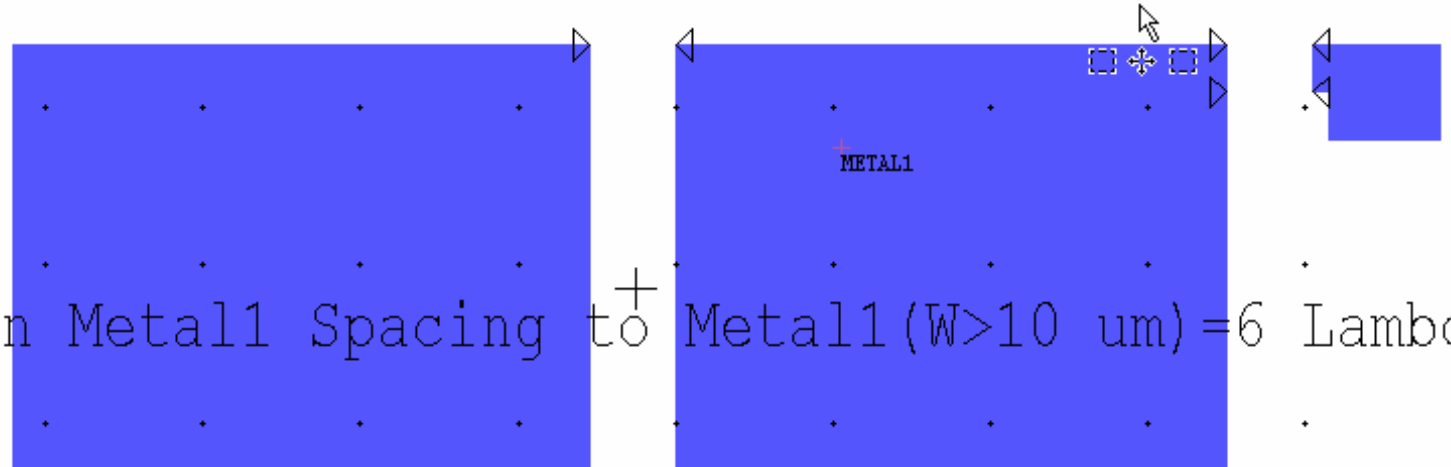
Metal 1 Design Rules: Separation

7.1 Width = 3



7.2 Spacing = 3

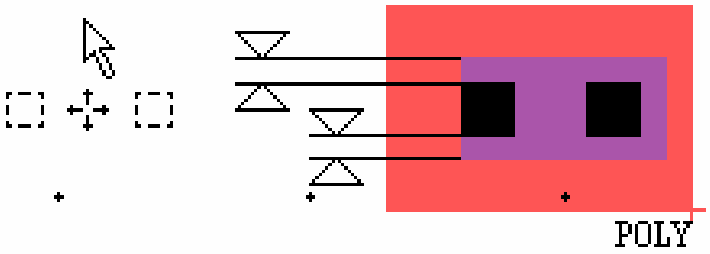




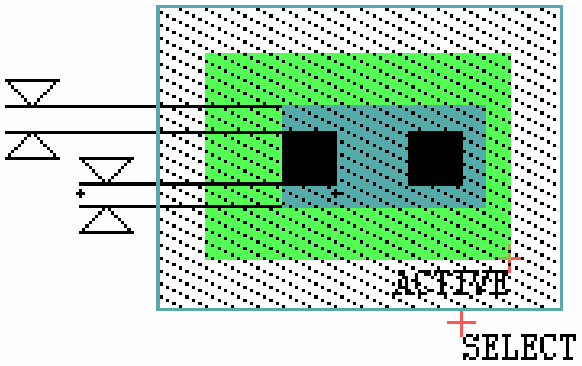
7.4 Min Metal1 Spacing to Metal1(W>10 um) =6 Lambda

Metal 1 Design Rules: Cnt Overlap

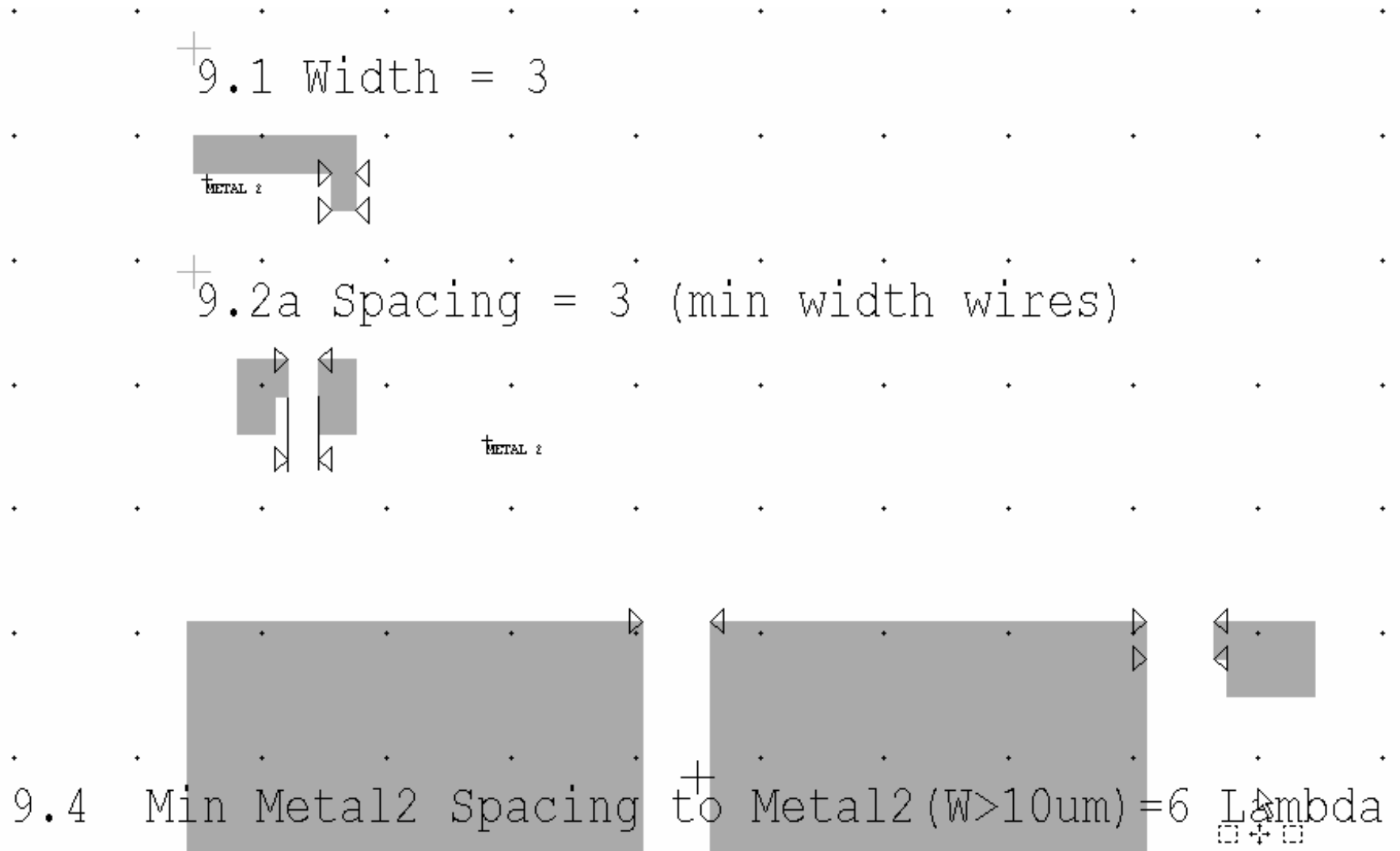
7.3 Overlap of PolyCnt = 1



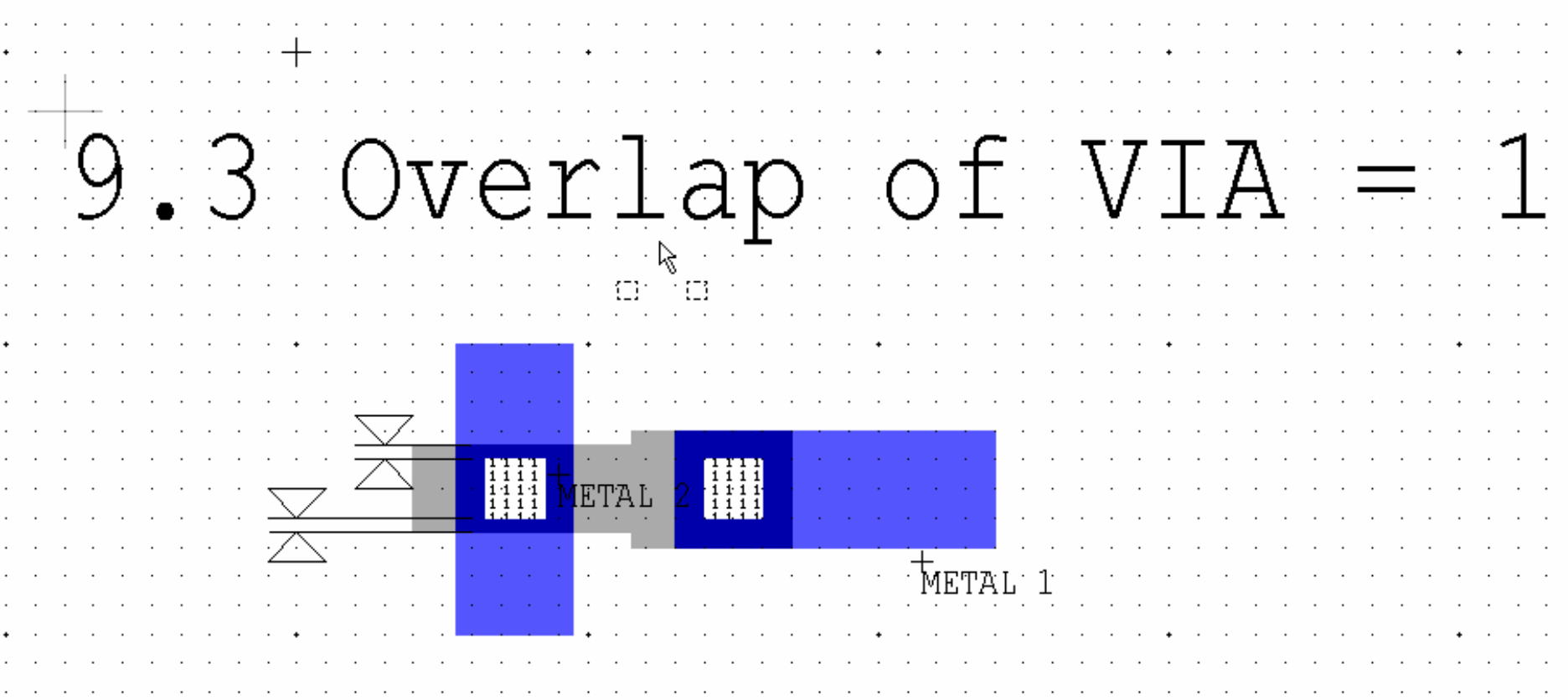
7.4 Overlap of ActCnt = 1



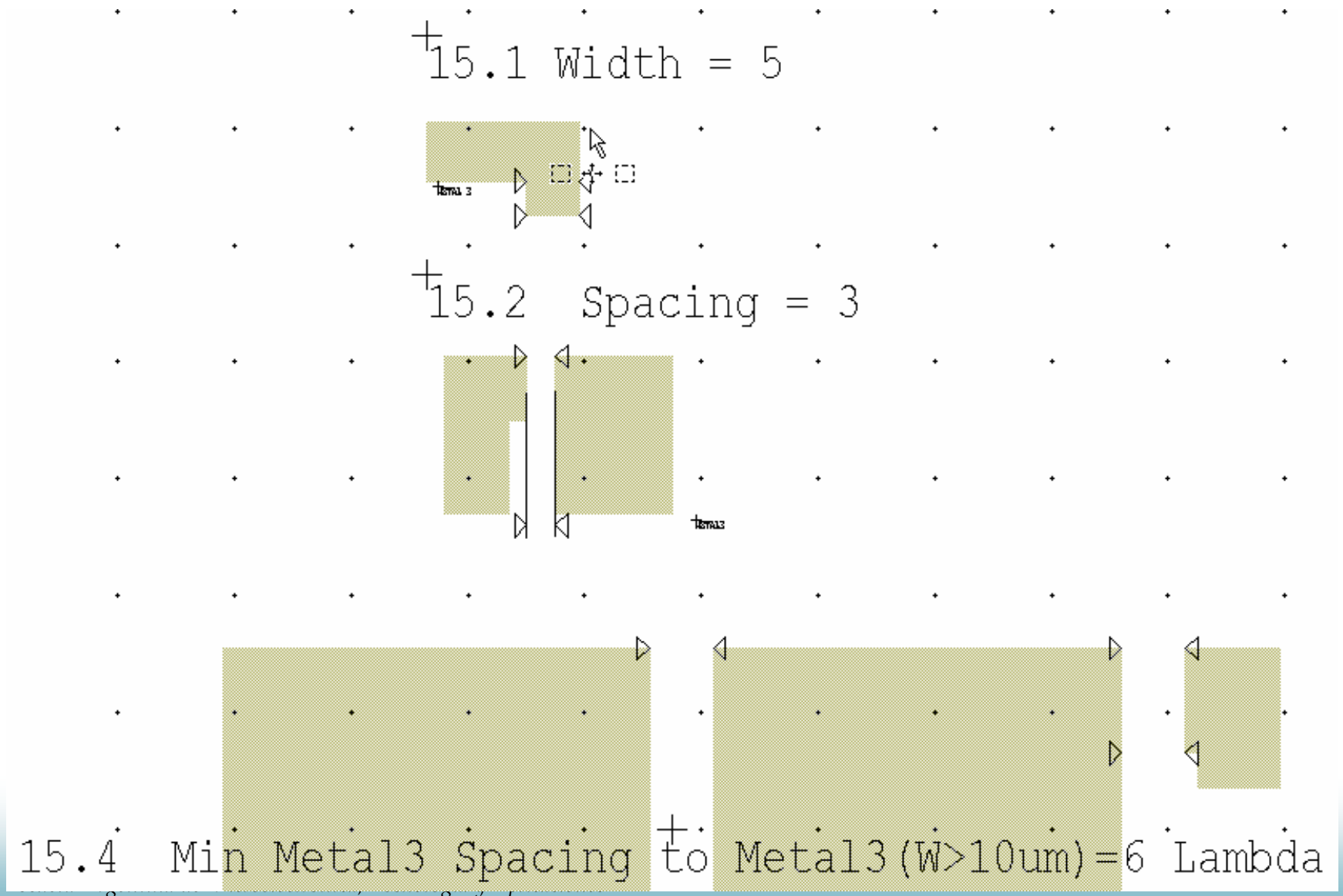
Metal 2 rules: Separation



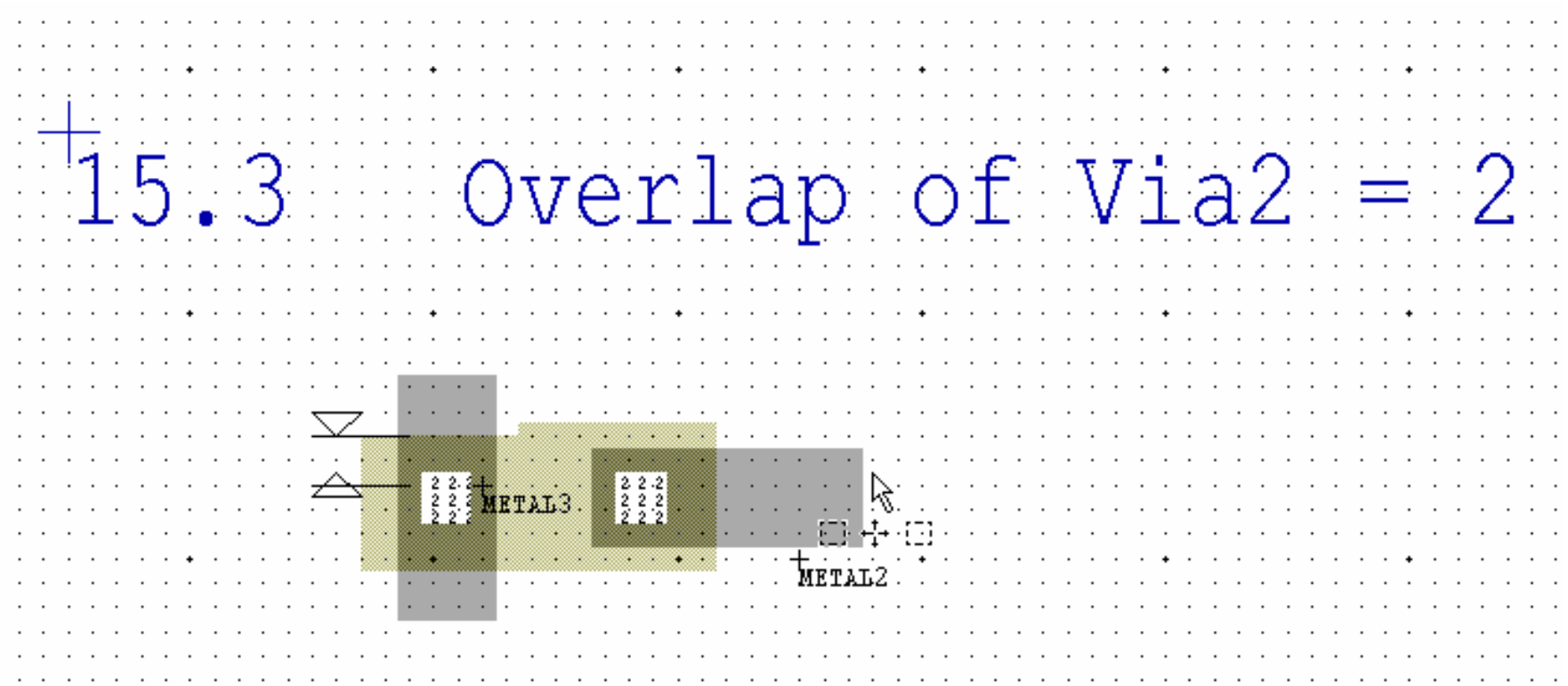
Metal 2 Design Rules: via1 Overlap



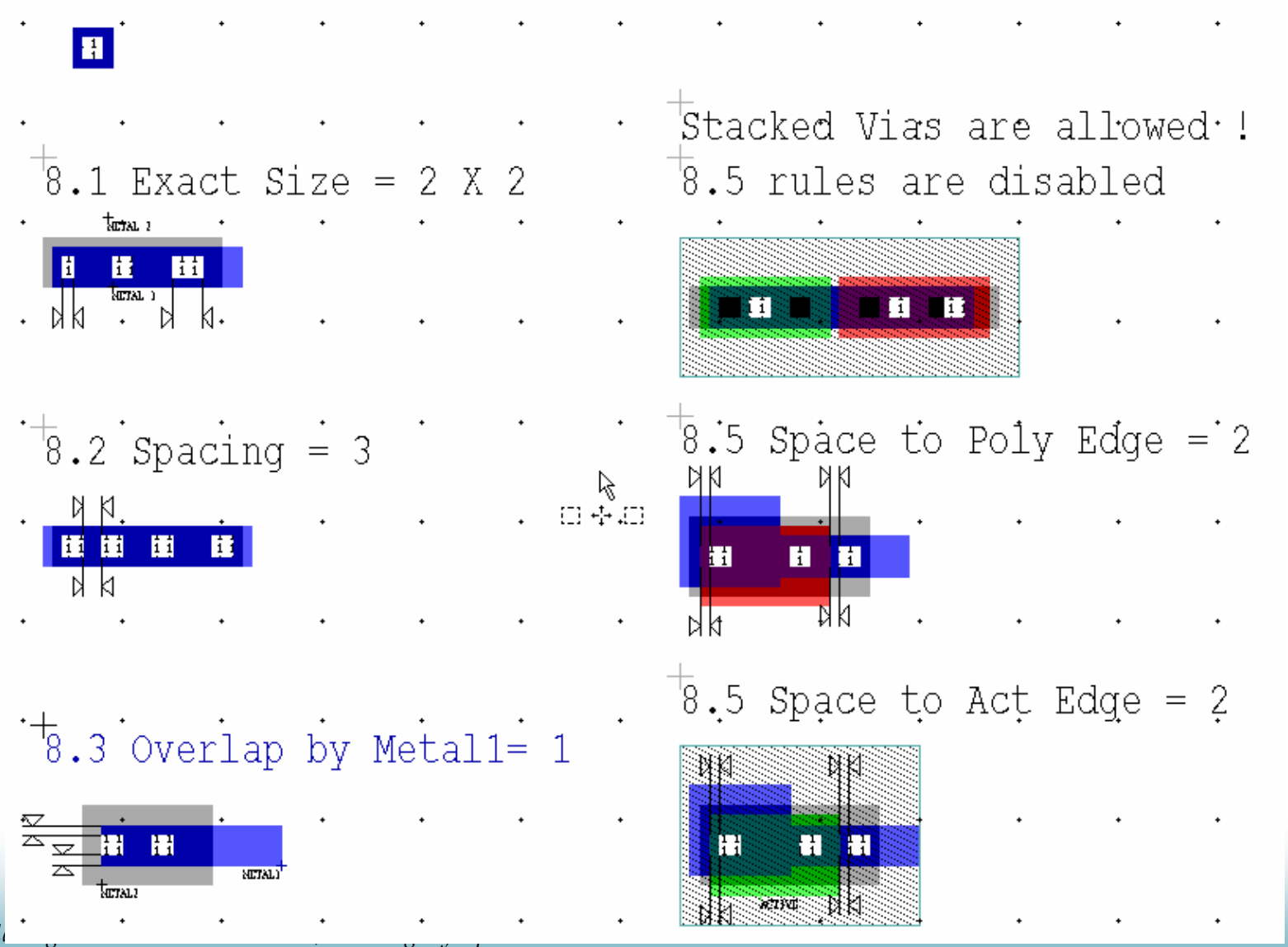
Metal 3 rules: Separation



Metal 3 Design Rules: via2 Overlap

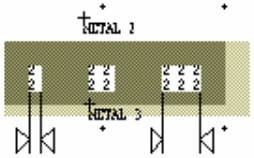


Via 1 rules

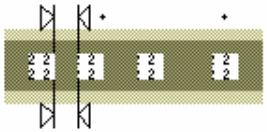

8.1 Exact Size = 2 X 2
8.2 Spacing = 3
8.3 Overlap by Metal1= 1
Stacked Vias are allowed !
8.5 rules are disabled
8.5 Space to Poly Edge = 2
8.5 Space to Act Edge = 2

Via 2 rules

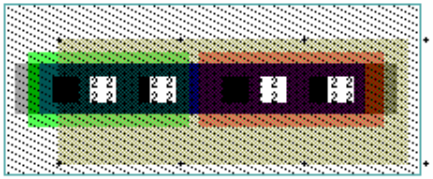
14.1 Exact Size = 2 X 2



14.2 Spacing = 3

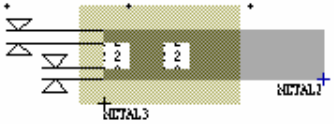


Stacked Vias are allowed !



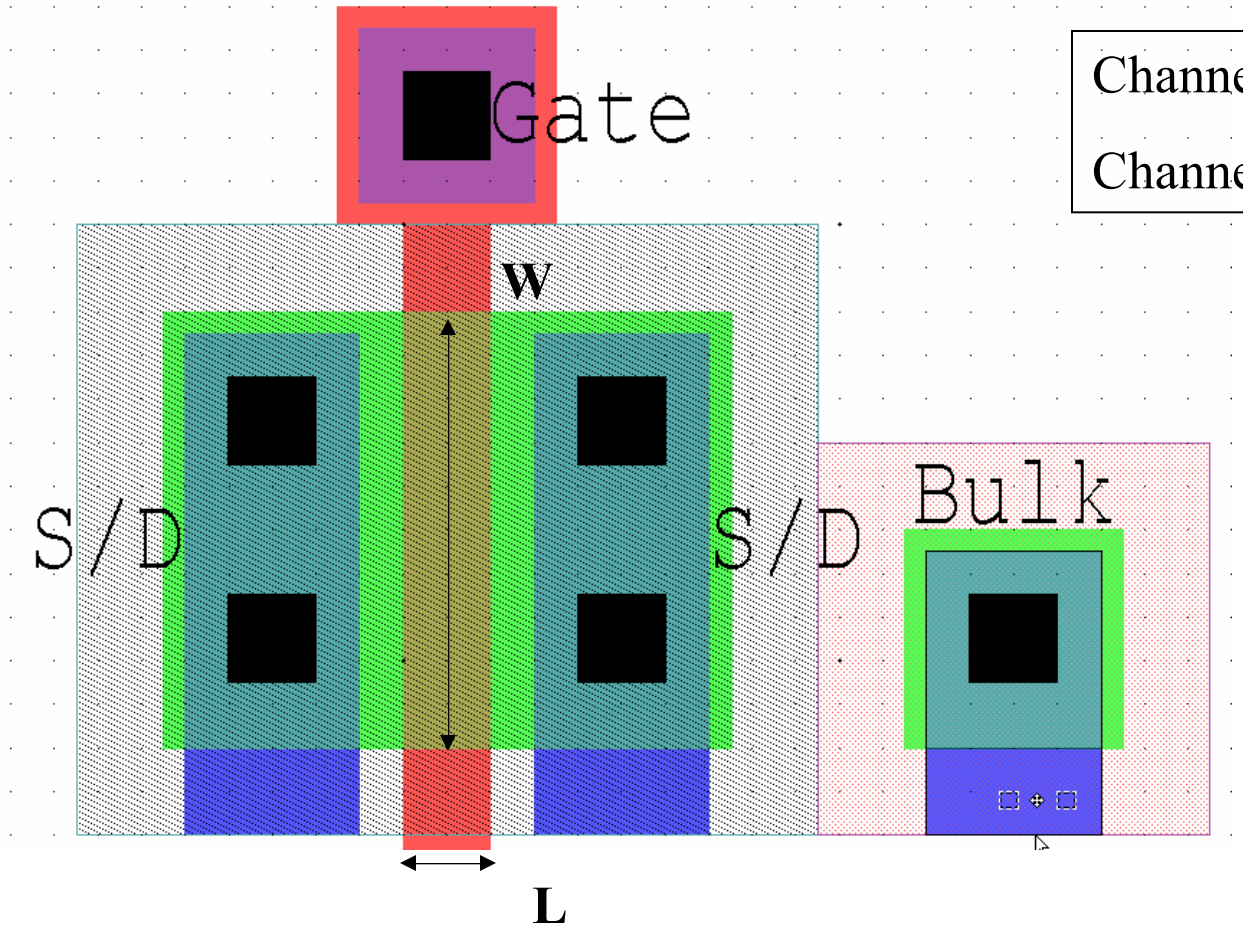
Vias over Contacts are allowed

14.3 Overlap by Metal2= 2



Layout de Transistores MOS

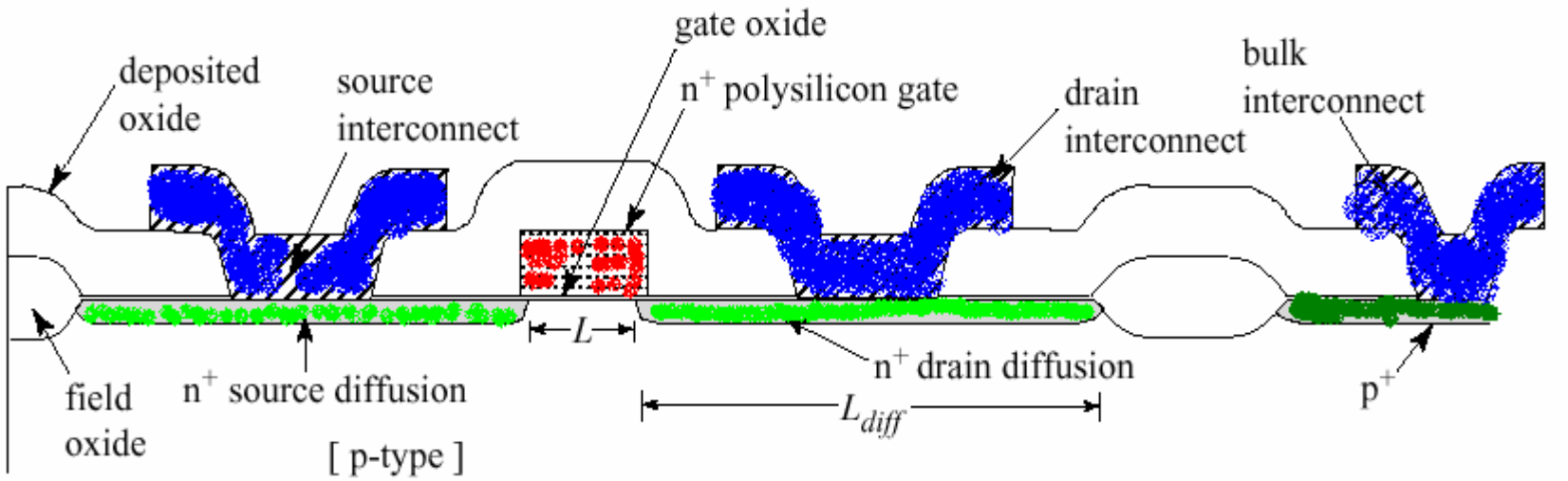
N-Channel MOSFET



Channel width: W

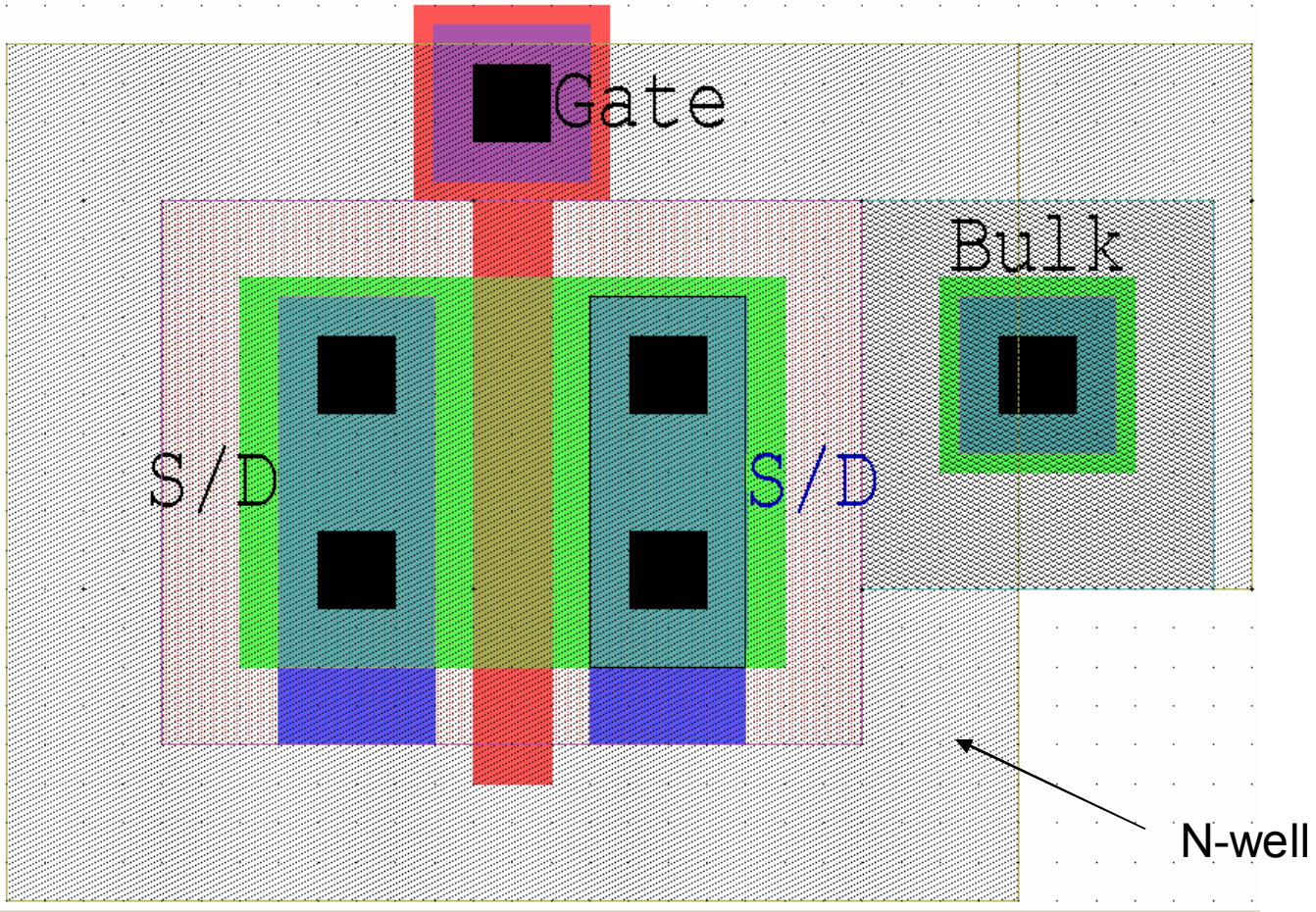
Channel length: L

N-channel MOS

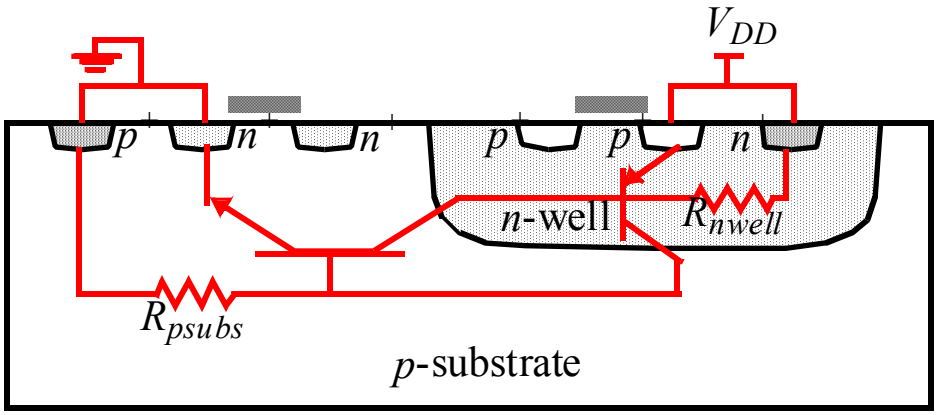


- Diffusions are equal. Potential on them will define S and D

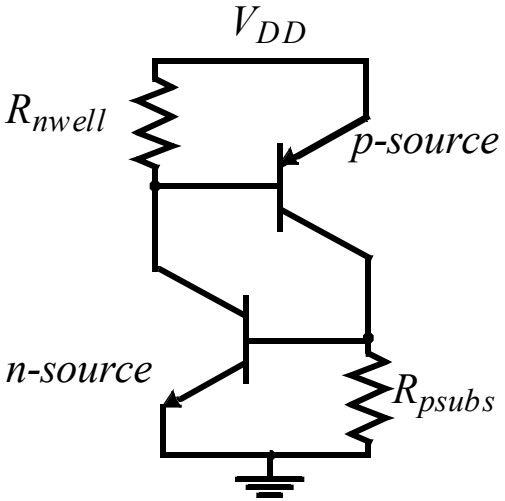
P-channel MOS



Latchup

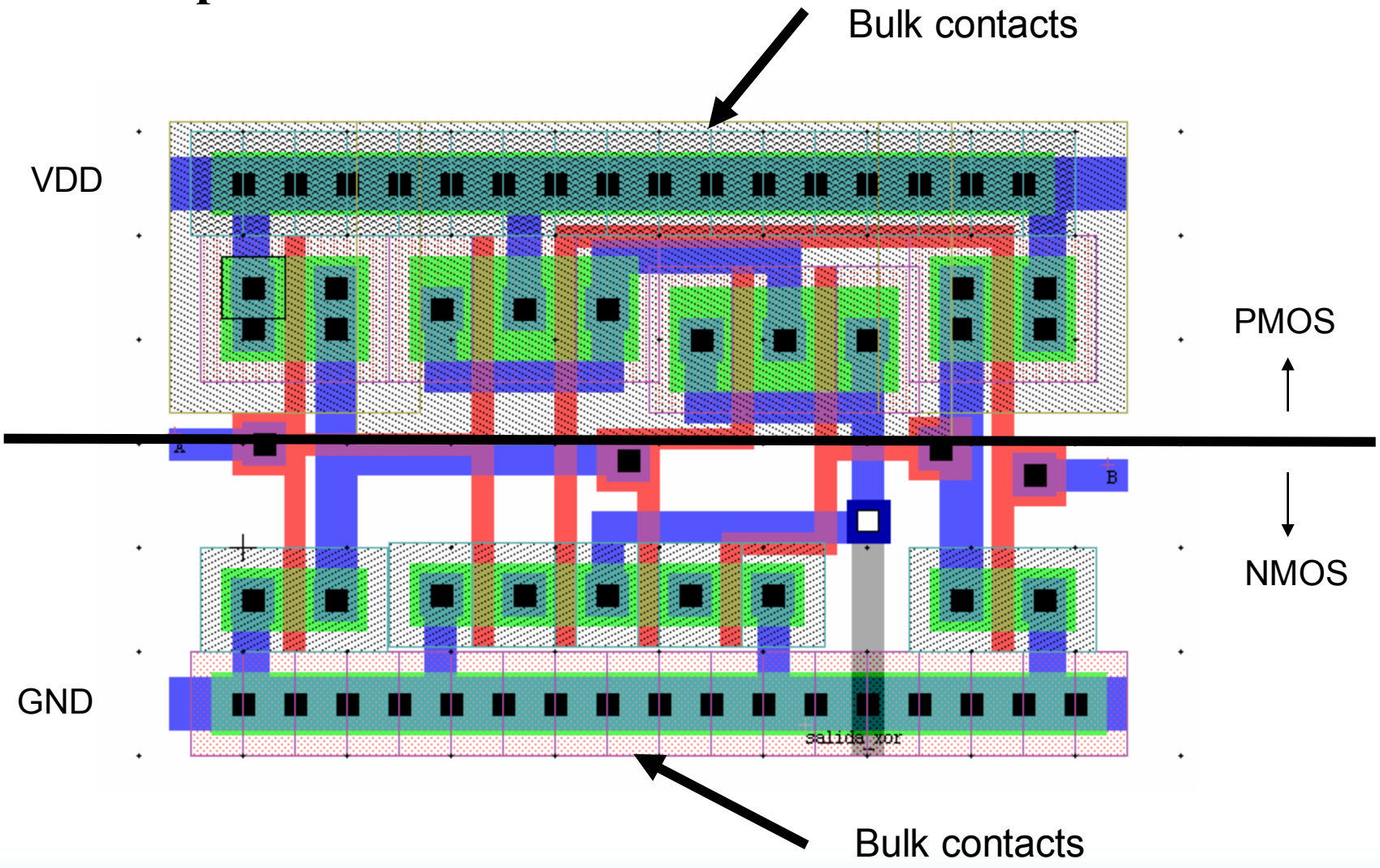


(a) Origin of latchup



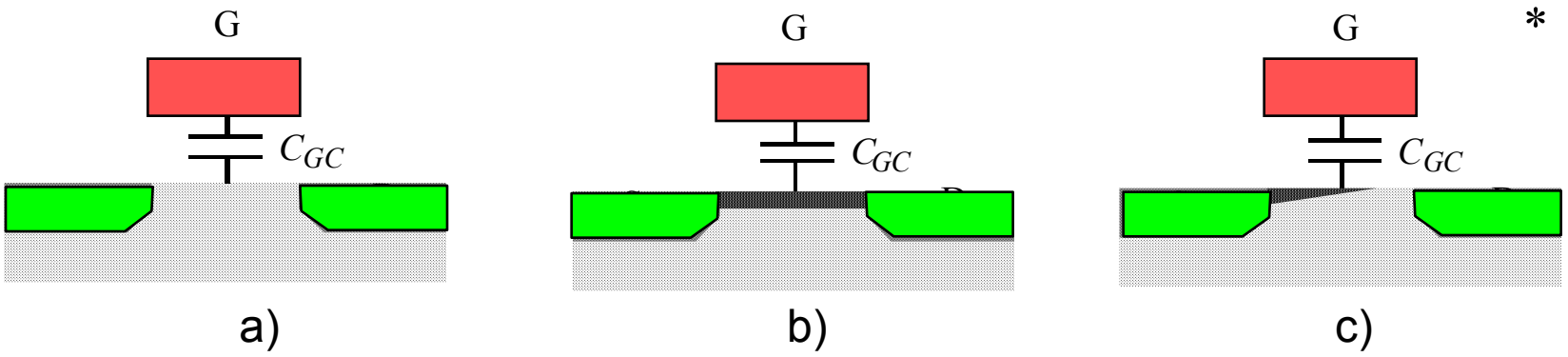
(b) Equivalent circuit

Latchup: solution



Transistor MOS: Capacidades

MOSFET Capacitances: Gate-Bulk



*

- Gate-Bulk capacitance dominates
- Depending on the operation mode this capacitance changes
  - a) cut-off: no charge. Appers directly as Cgb
  - b) resistive: channel acts as a shield, Cgb=0. Capacitance distributes between drain and source
  - c) saturation: Cgd and Cgb are zero. All capacitance is Cgs
- Digital Design: Saturation and cut-off are the most important

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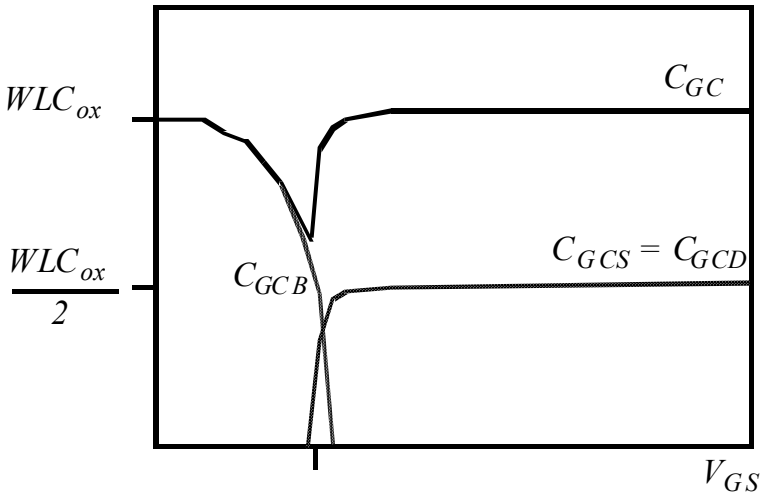
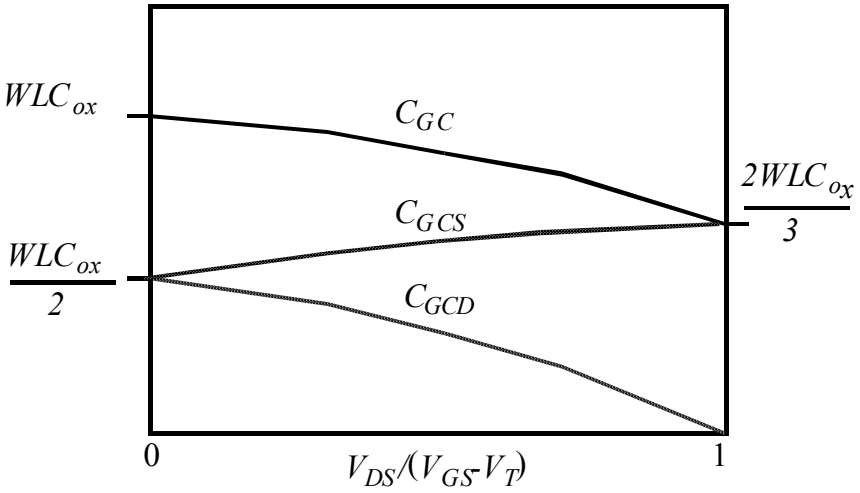
Gate Capacitance Behavior



Capacitance as a function of VGS (with VDS = 0)



Capacitance as a function of the degree of saturation

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Gate Capacitance Summary

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

- In cutoff, linear capacitor
- In triode, this C is splitted between S and D
- In saturation it is necessary to integrate the charge in the channel

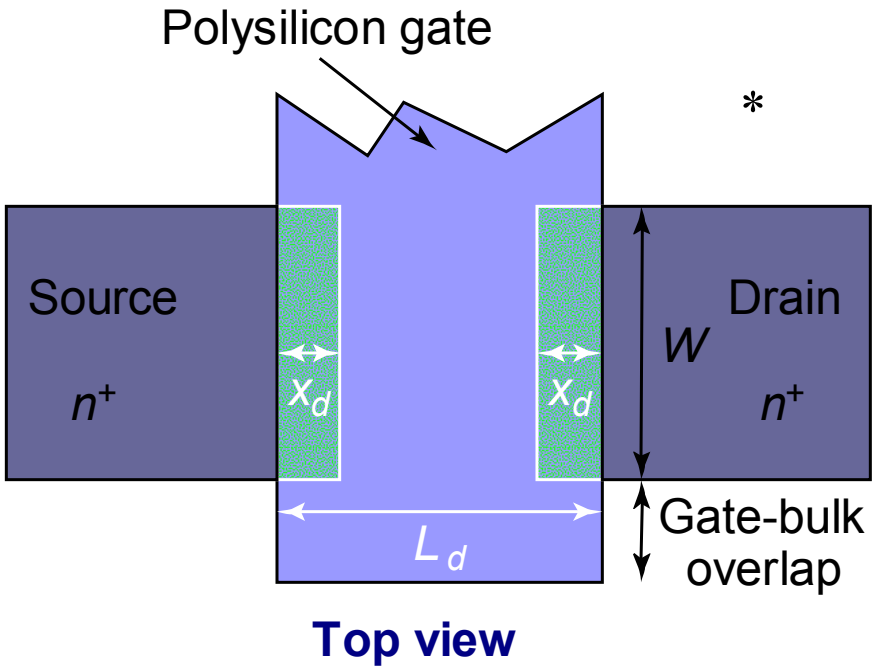
MOSFET Capacitances: Overlap

- Overlap capacitances are Cgso and Cgdo

$$C_{GSO} = C_{ox} x_d W$$
$$C_{GDO} = C_{ox} x_d W$$

- Values are given by unit width:

$$C_{gso} = C_{GSO} / W = C_{ox} x_d$$
$$C_{gdo} = C_{GDO} / W = C_{ox} x_d$$



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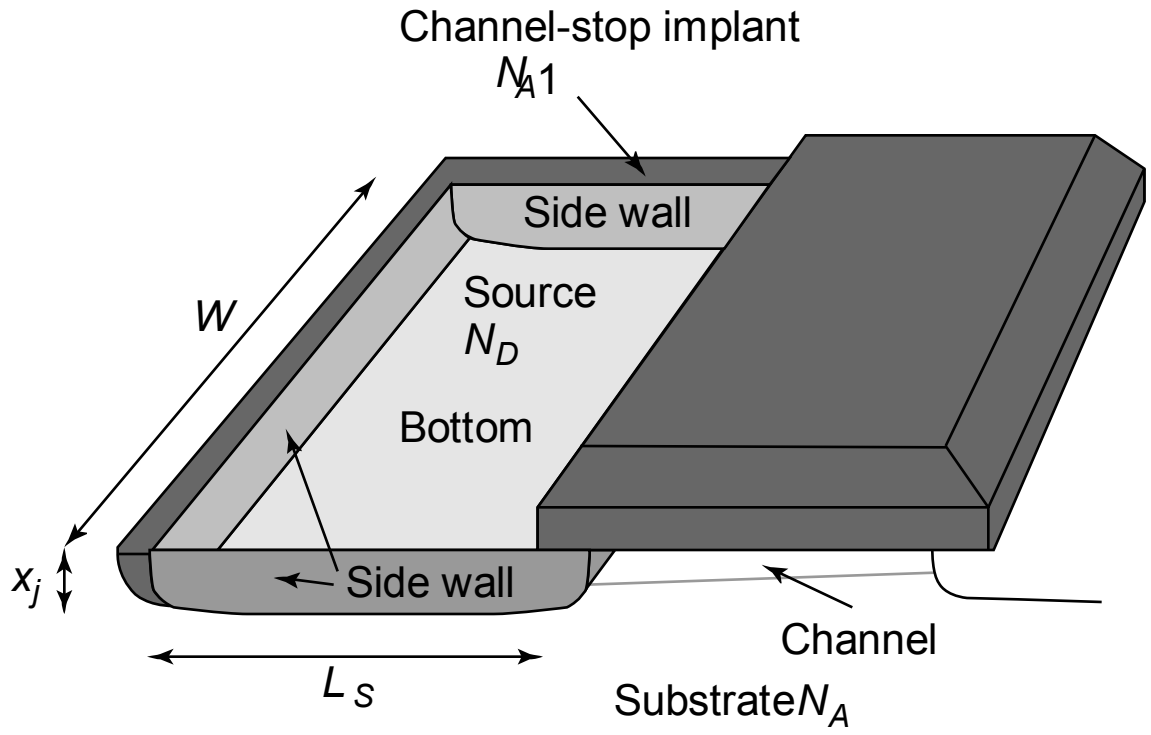
MOSFET Capacitances: Diffusion



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

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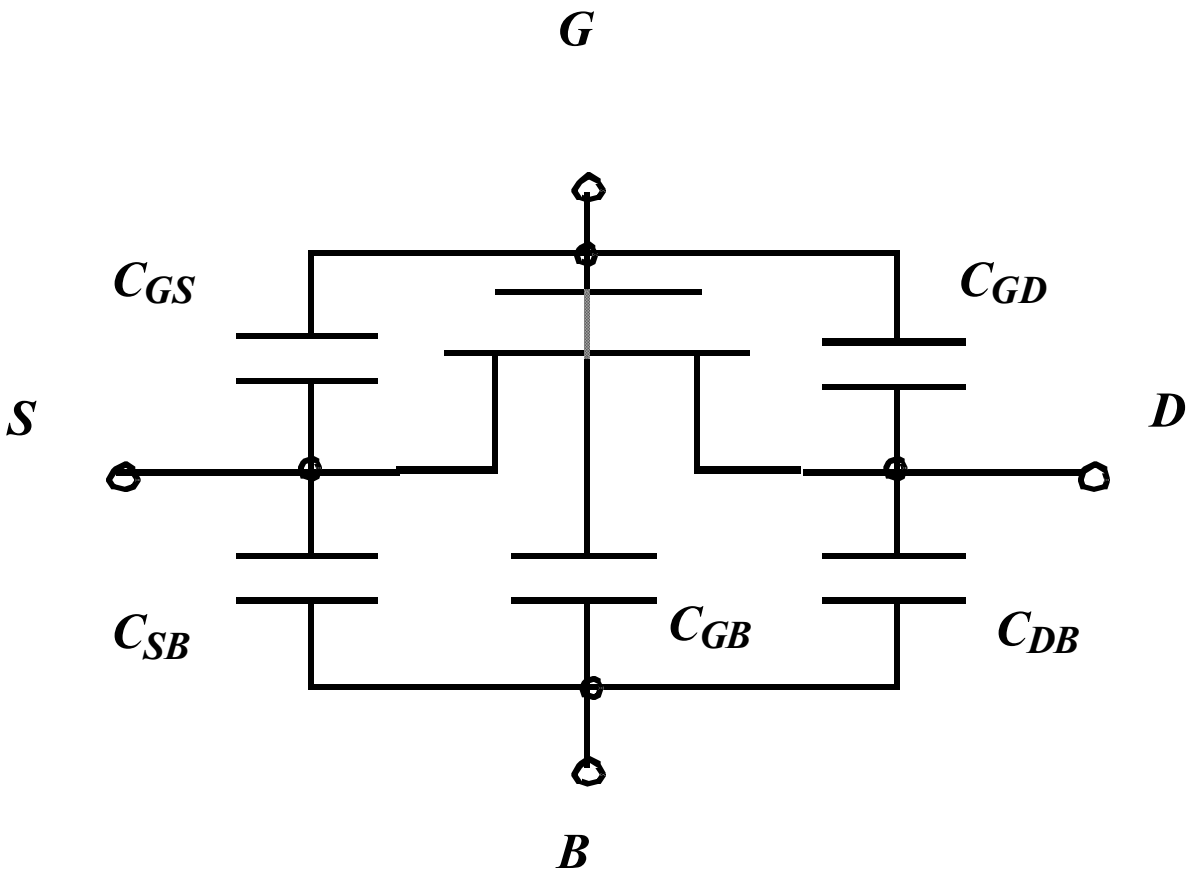
MOSFET Capacitances



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Referencias

- C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley, 1980
- N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A System Perspective*, Addison-Wesley, 2nd edition, 1993

Appendix

SPICE MODELS

- Level 1: Long channel equations – very simple
- Level 2: Physhical model – includes velocity saturation and thresholds variations
- Level 3: Semi-emperical- based on curve fitting to measured devices
- Level 4: (BSIM) Emperical – simple and popular

AMI 0.5 typical parameters (T36s)

MOSIS PARAMETRIC TEST RESULTS

RUN: T36S VENDOR: AMI
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	81.8	102.0	22.5	988	40.4	0.09	0.09	ohms/sq
Contact Resistance	57.5	125.9	15.9		25.6		0.87	ohms
Gate Oxide Thickness	141							angstrom

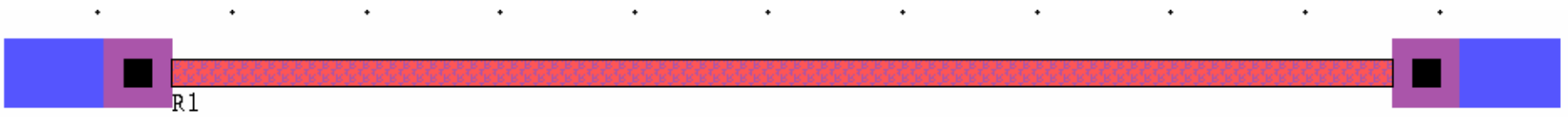
PROCESS PARAMETERS	MTL3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	820	810	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	424	730	87		32	16	10	40	aF/um^2
Area (N+active)			2450		36	16	11		aF/um^2
Area (P+active)			2360						aF/um^2
Area (poly)				858	57	16	9		aF/um^2
Area (poly2)					52				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	310	251			76	59	39		aF/um
Fringe (poly)					61	38	28		aF/um
Fringe (metal1)						51	33		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			201						aF/um
Overlap (P+active)			262						aF/um

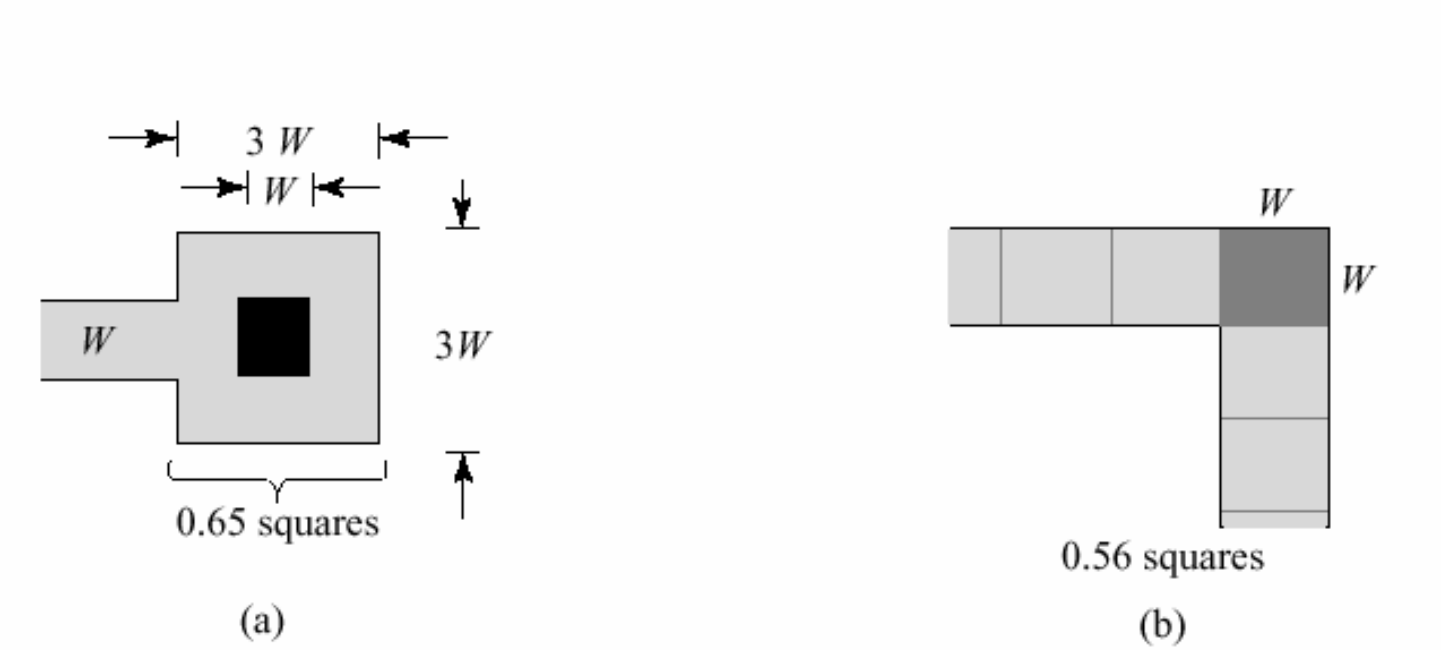
Poly Resistor

- MOSIS webpage data for AMI 0.5 R(N_Well) = 22Ω/□
- Exercise: Layout and extract a resistor (minimum width) of 1K. Try to make a square design
- Number of squares to achieve the desired resistance = 1000/22 □ = 45.5
- Setting W = 2 λ then L = 91 λ
- Run DRC, extract and verify



Equivalent size of corners and dogbones

- Folding the resistor leads to compact designs
- Squares and corners contribute partially to the material resistance



Metal parasitics: C

- Example: Two lines of M1 and M2 of 1mm running on top of each other

- A pad is typically 100μm × 100μm of M2 on top of M1 on top of substrate. Calculate total capacitance:

Ejercicio

- Realizar el Layout del siguiente circuito
- Extractar
- Correr LVS con el archivo generado por SPICE (provisto)