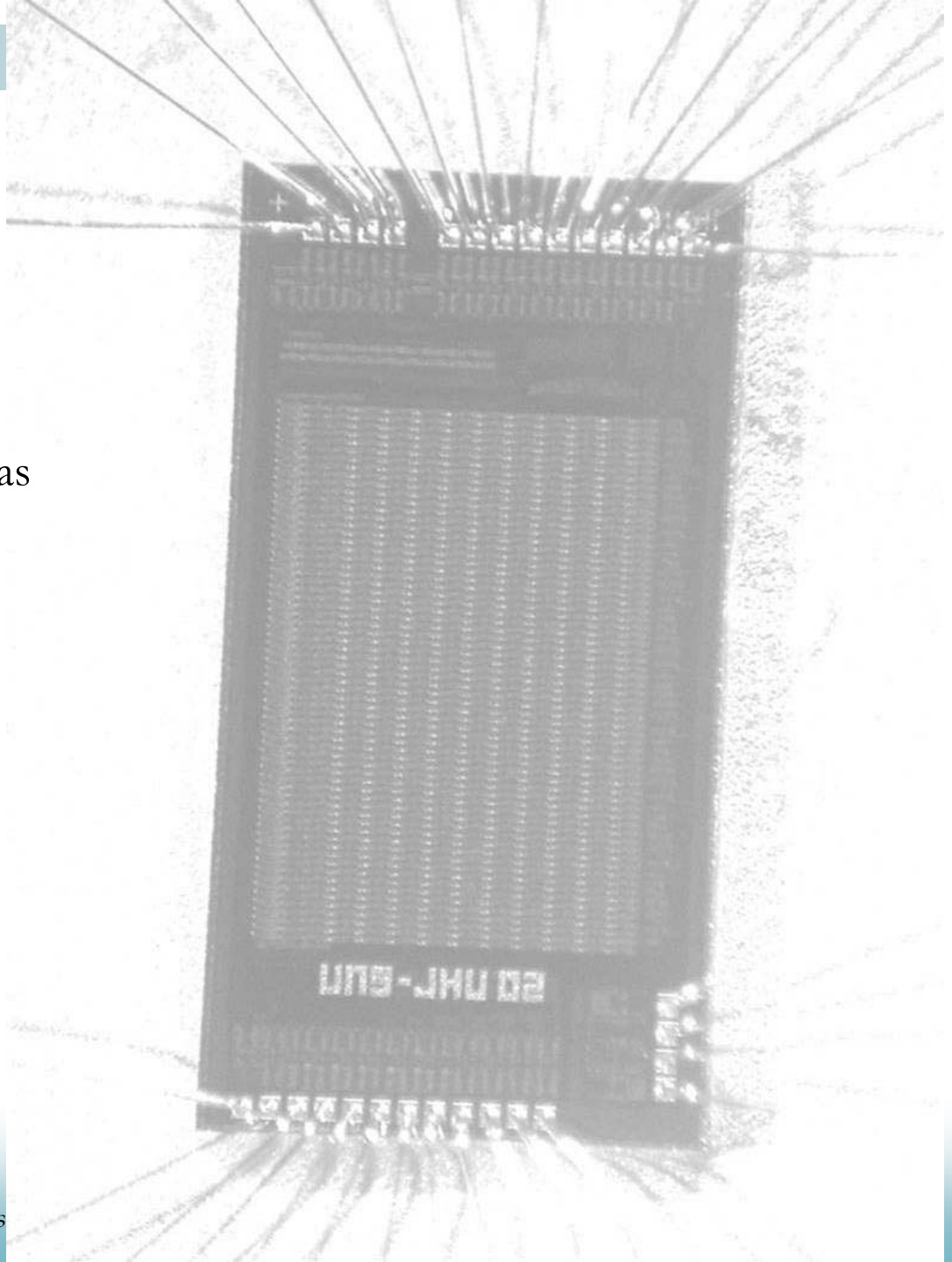
Introducción a VLSI

EAMTA 2006

Programa

- **El Transistor MOS**
- Layers y Layout
- Lógica Combinacional
- Lógica Secuencial y Subsistemas



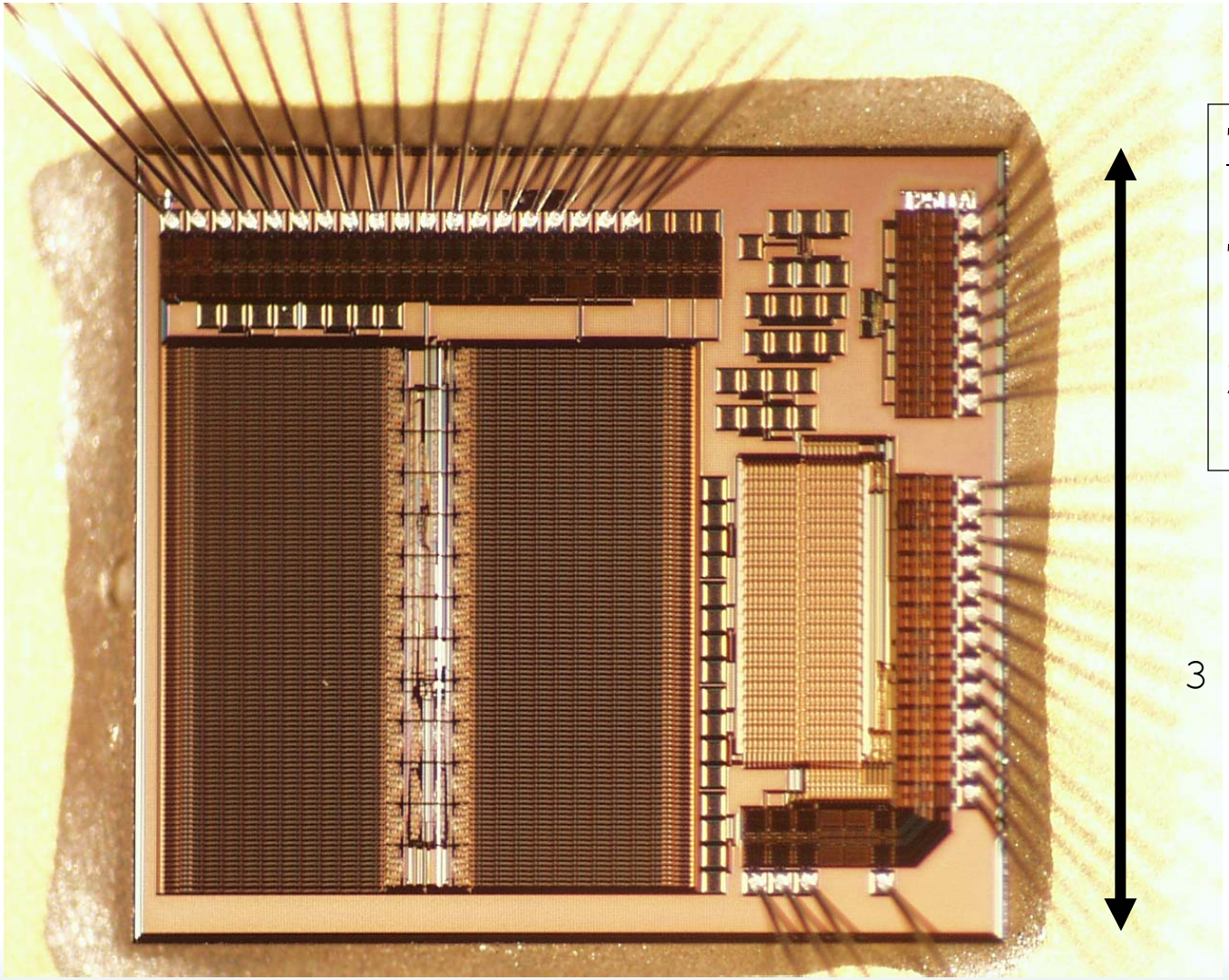
Clase 1: El transistor MOS

Organización

- Ejemplo de Motivación
- Modelo del transistor MOS
- El inversor CMOS
- El transistor como llave

Motivación

Ejemplo “autóctono”

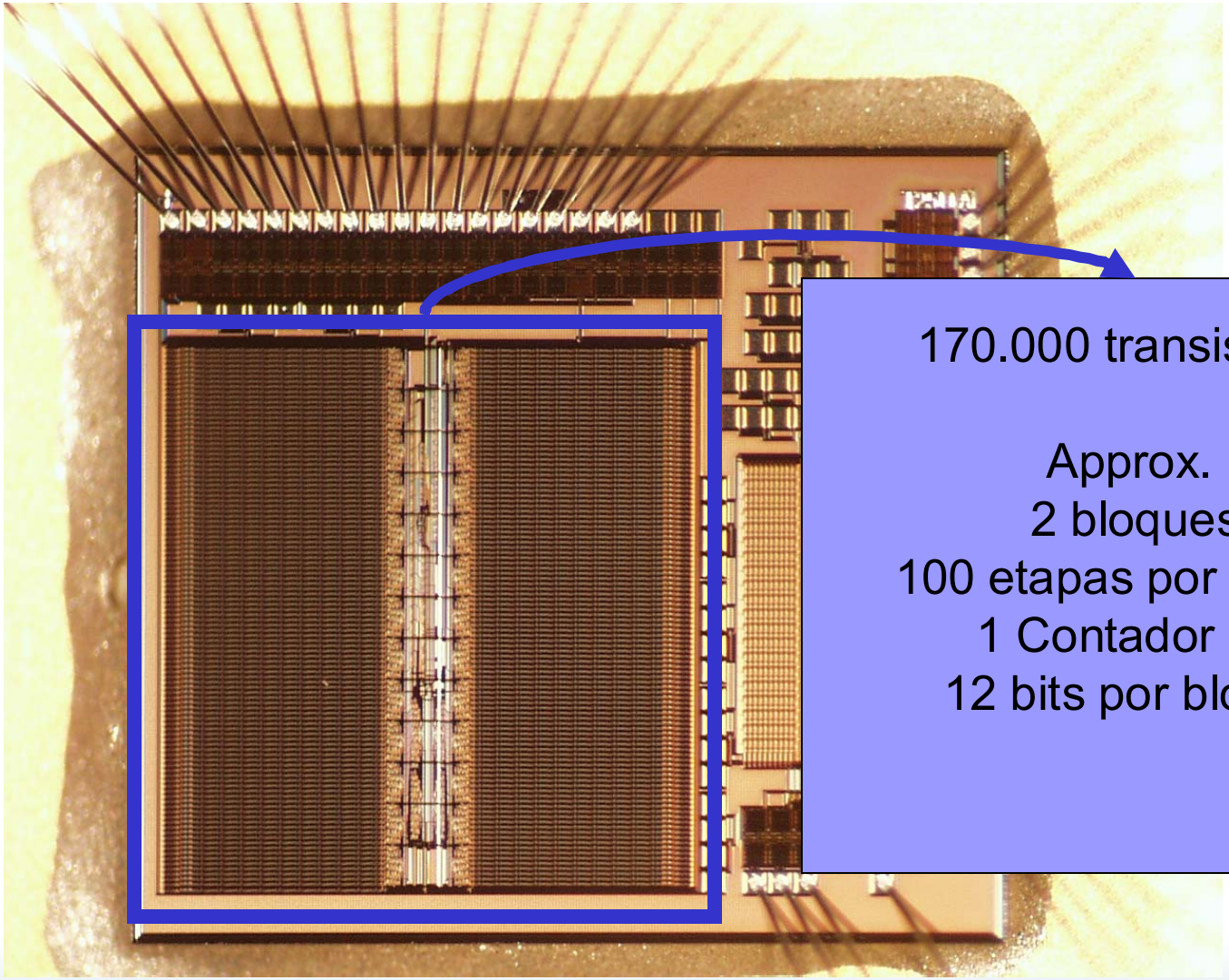


Tecnología

TSMC 0.35 μm

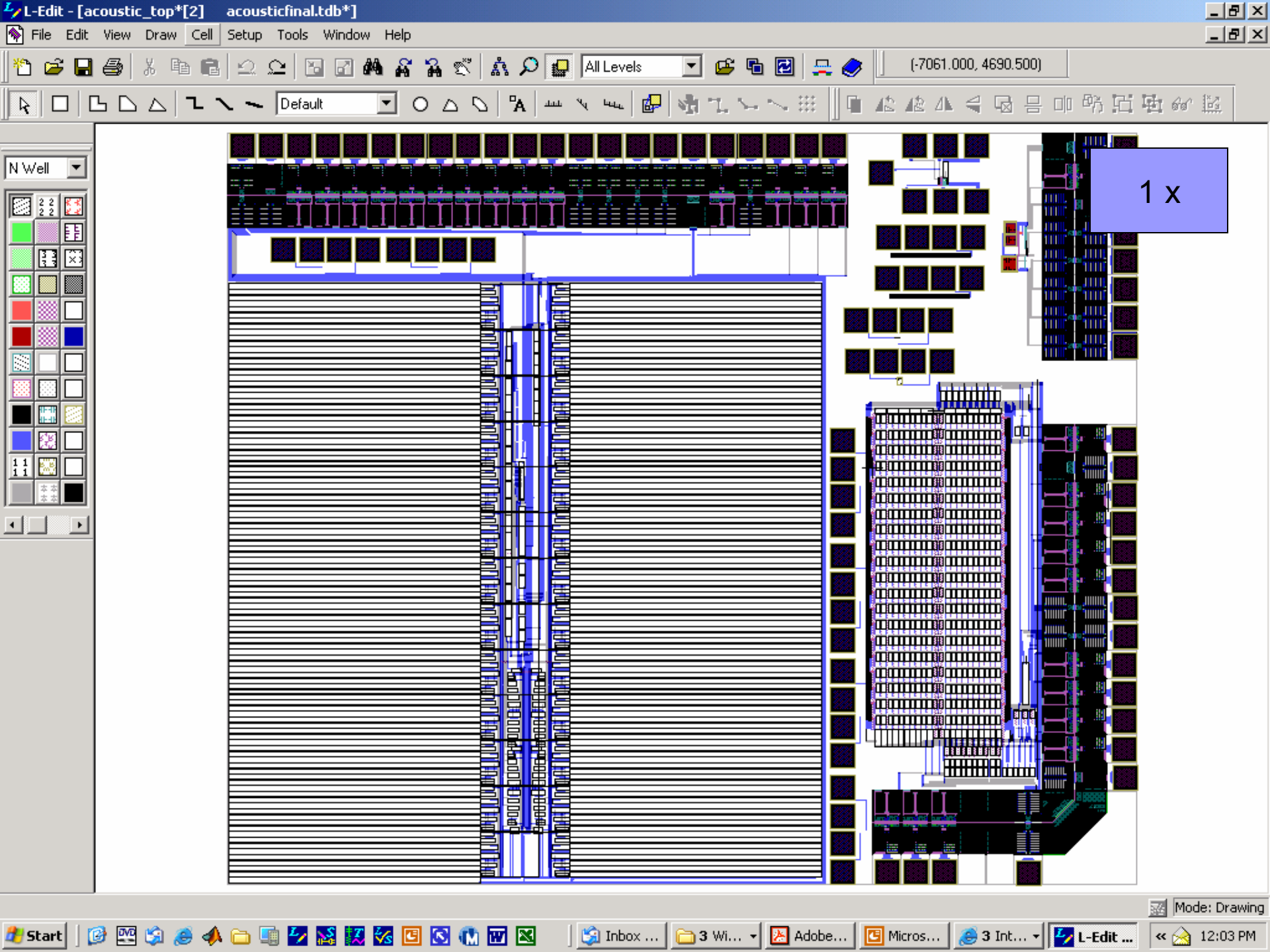
λ = 0.2 μm

Ejemplo “autóctono” (2)



170.000 transistores

Approx.
2 bloques
100 etapas por bloque
1 Contador de
12 bits por bloque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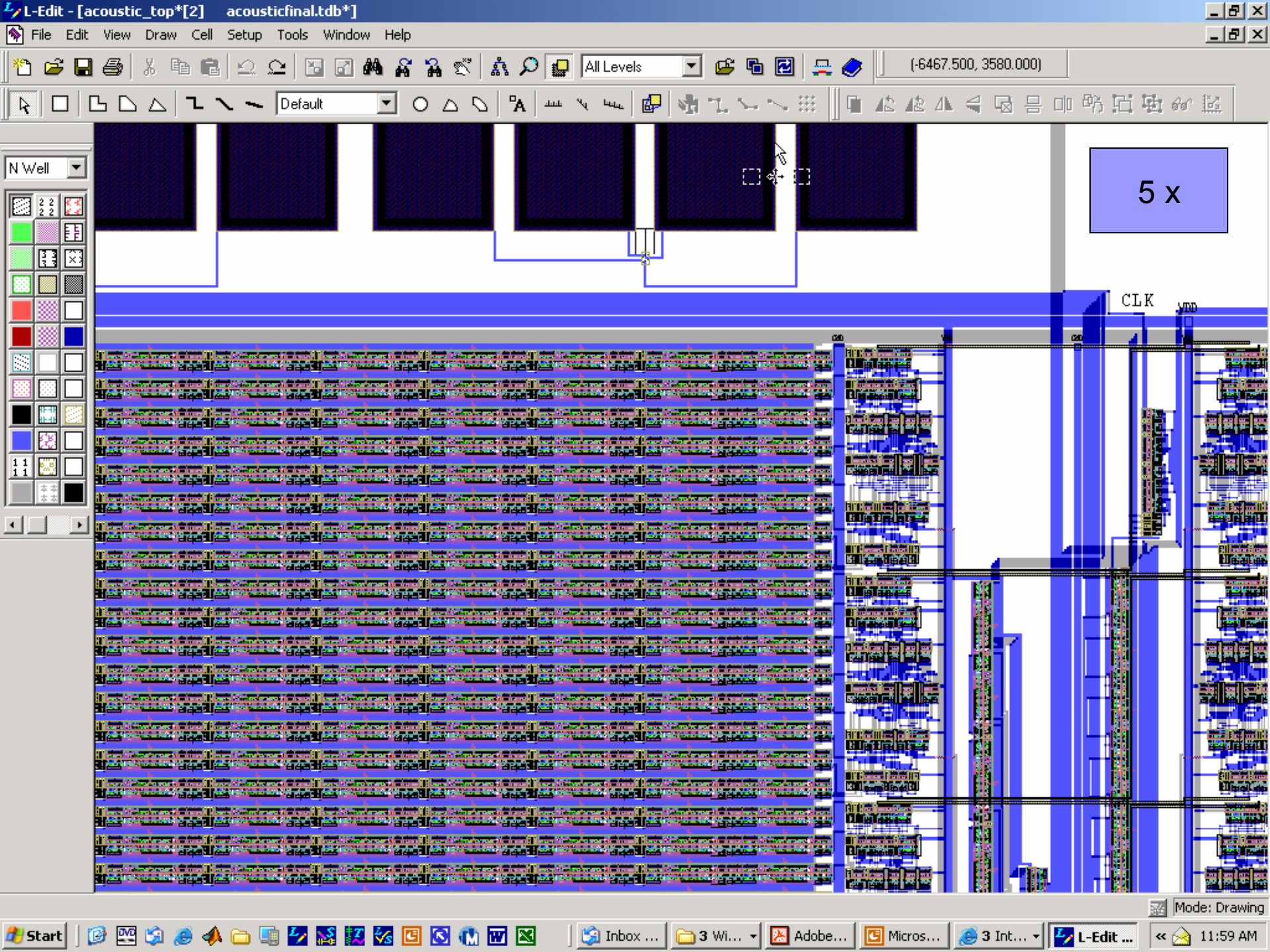
3 Wi...
Adobe...
Micros...
3 Int...
L-Edit ...
12:03 PM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VDD
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Micros...
3 Int...
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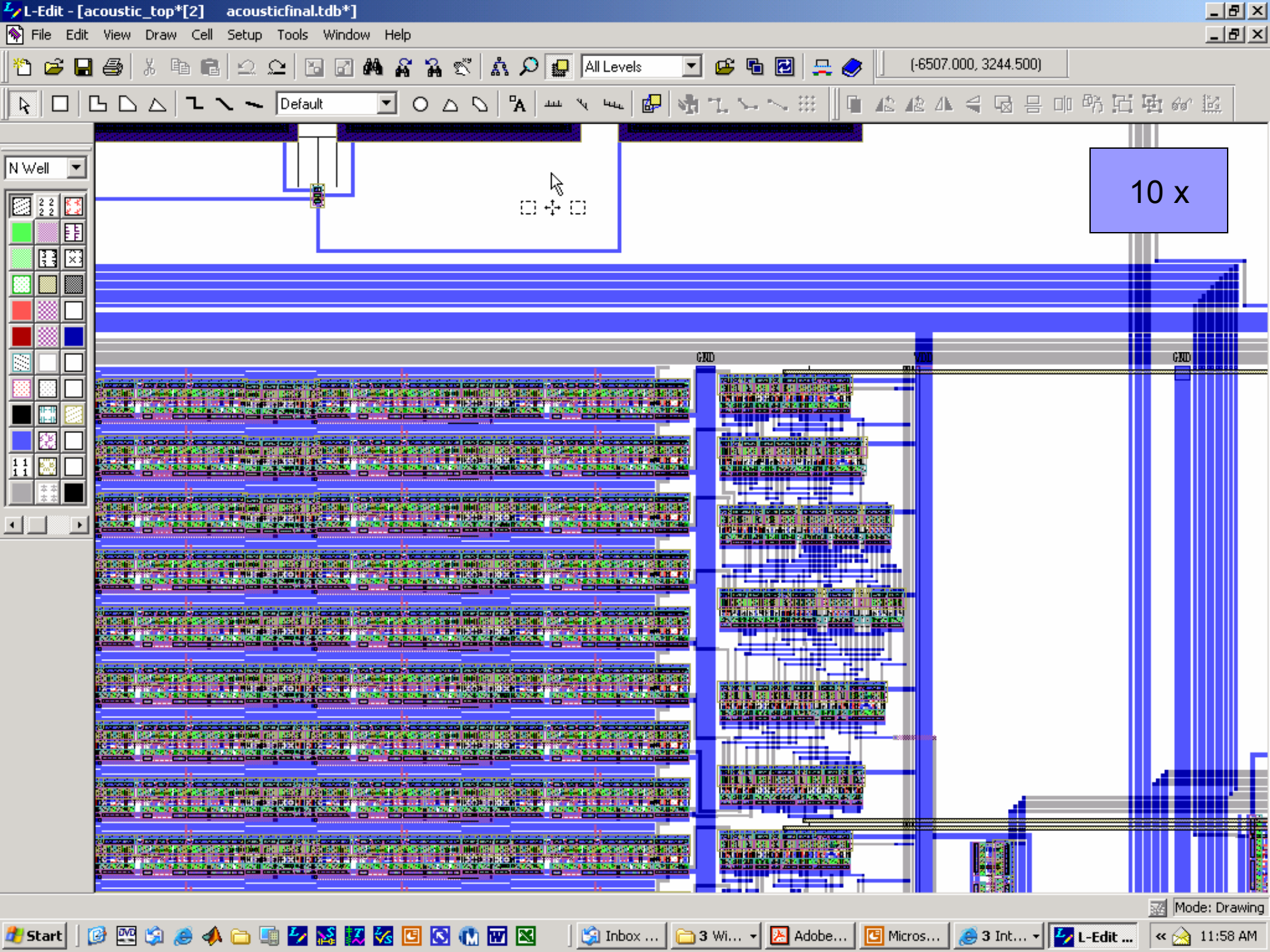
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10 x
GND
VDD
GND
Mode: Drawing
Start
Inbox ...
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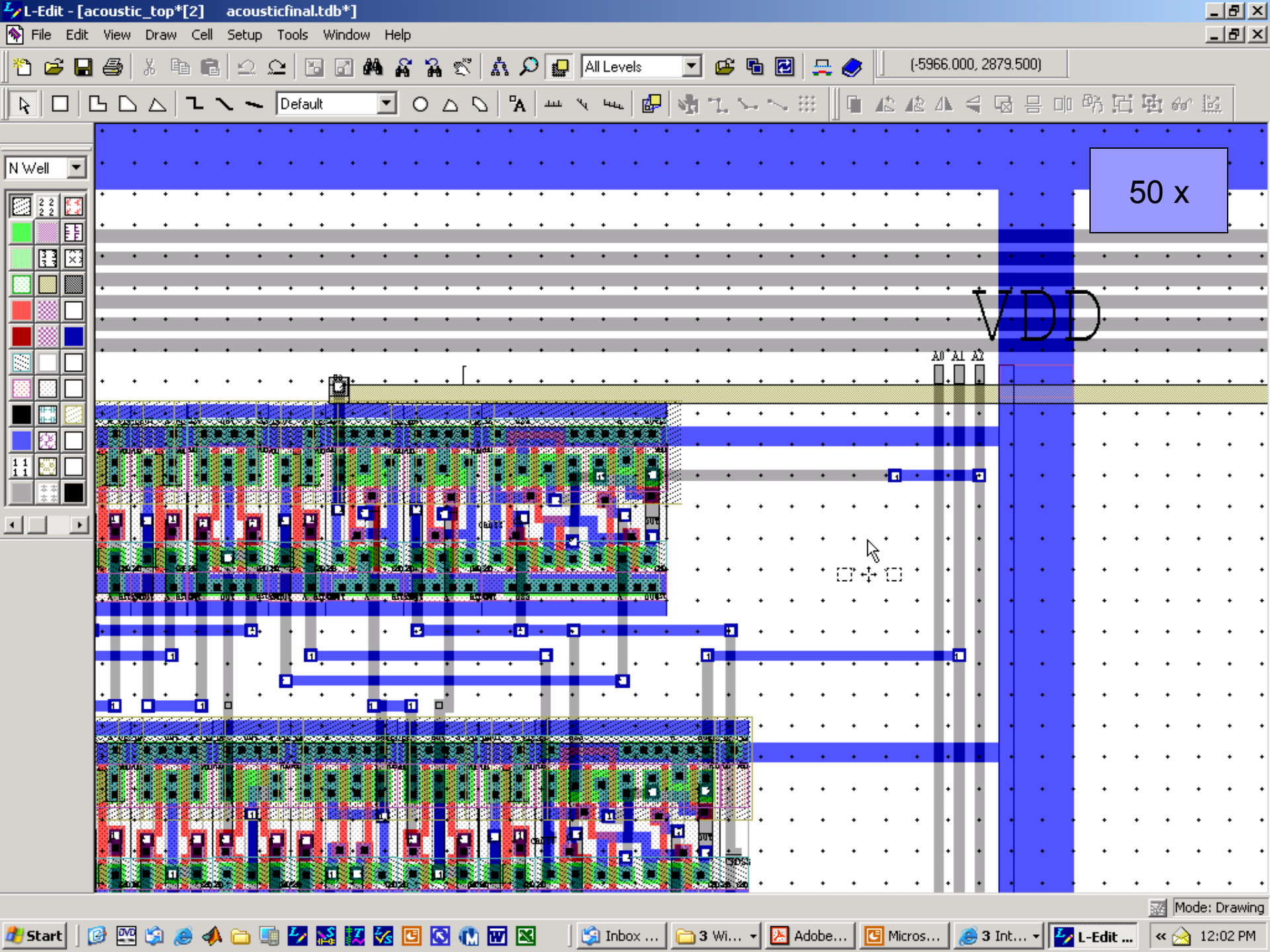
Adobe...
Micros...
3 Int...
L-Edit ...
11:58 AM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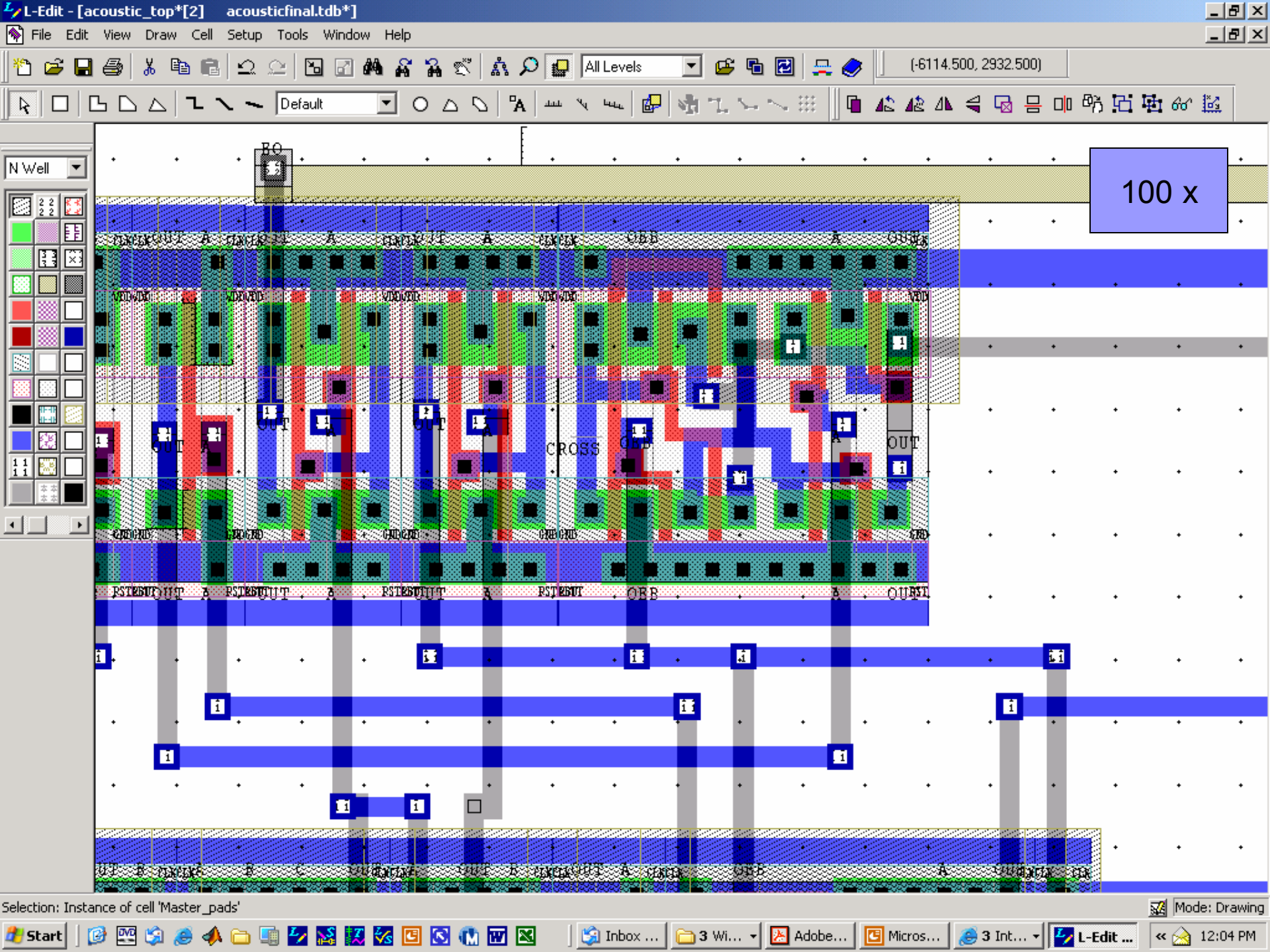
All Levels
(-5966.000, 2879.500)
Default
N Well
50 x
VDD
A0 A1 A2
Mode: Drawing
Start
Inbox ...
3 Wi...
Adobe...
Micros...
3 Int...
L-Edit ...
12:02 PM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All Levels
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Default
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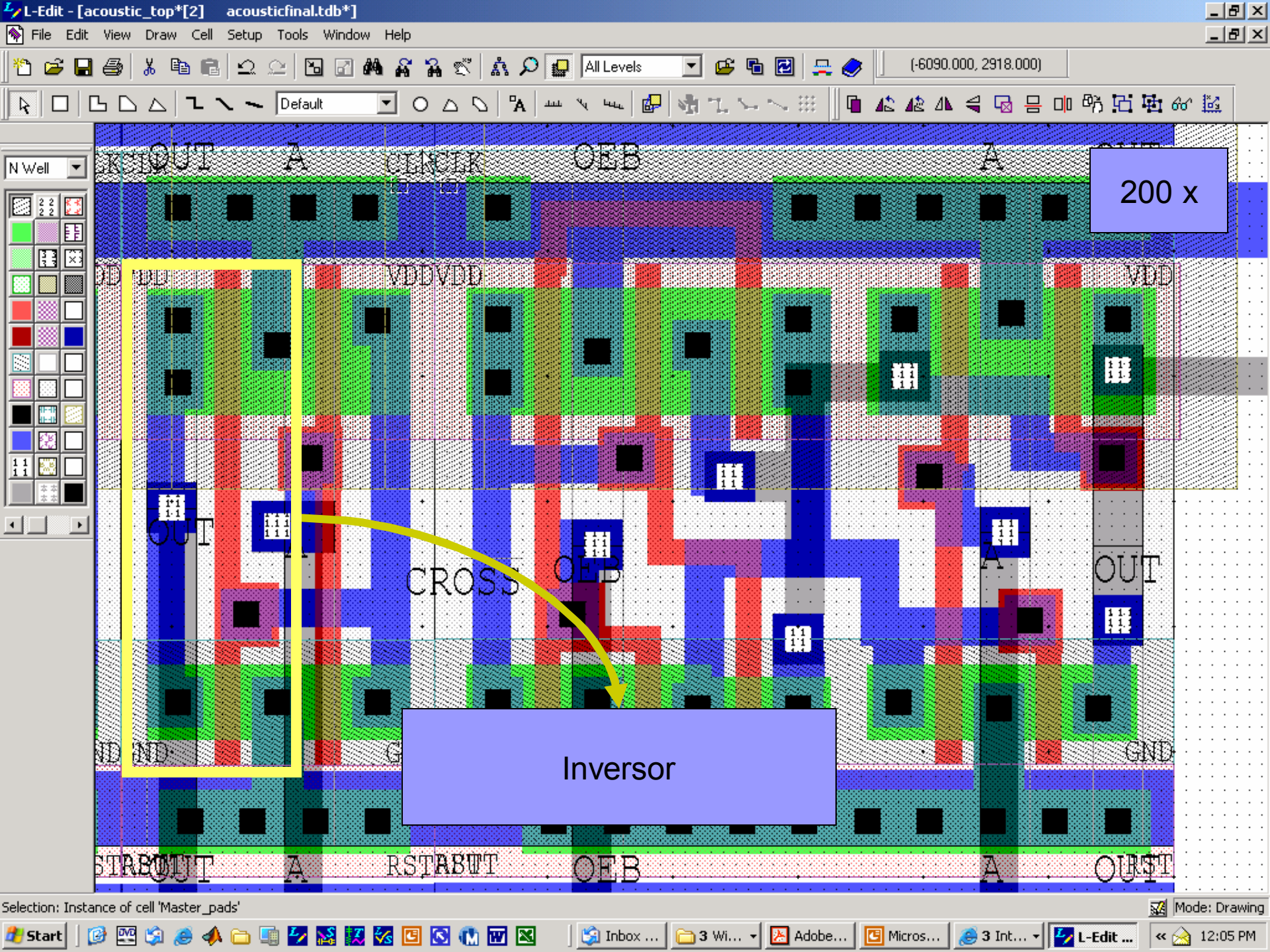
100 x
Selection: Instance of cell 'Master_pads'
Mode: Drawing
Start
Inbox ...
3 Wi...
Adobe...
Micros...
3 Int...
L-Edit ...
12:04 PM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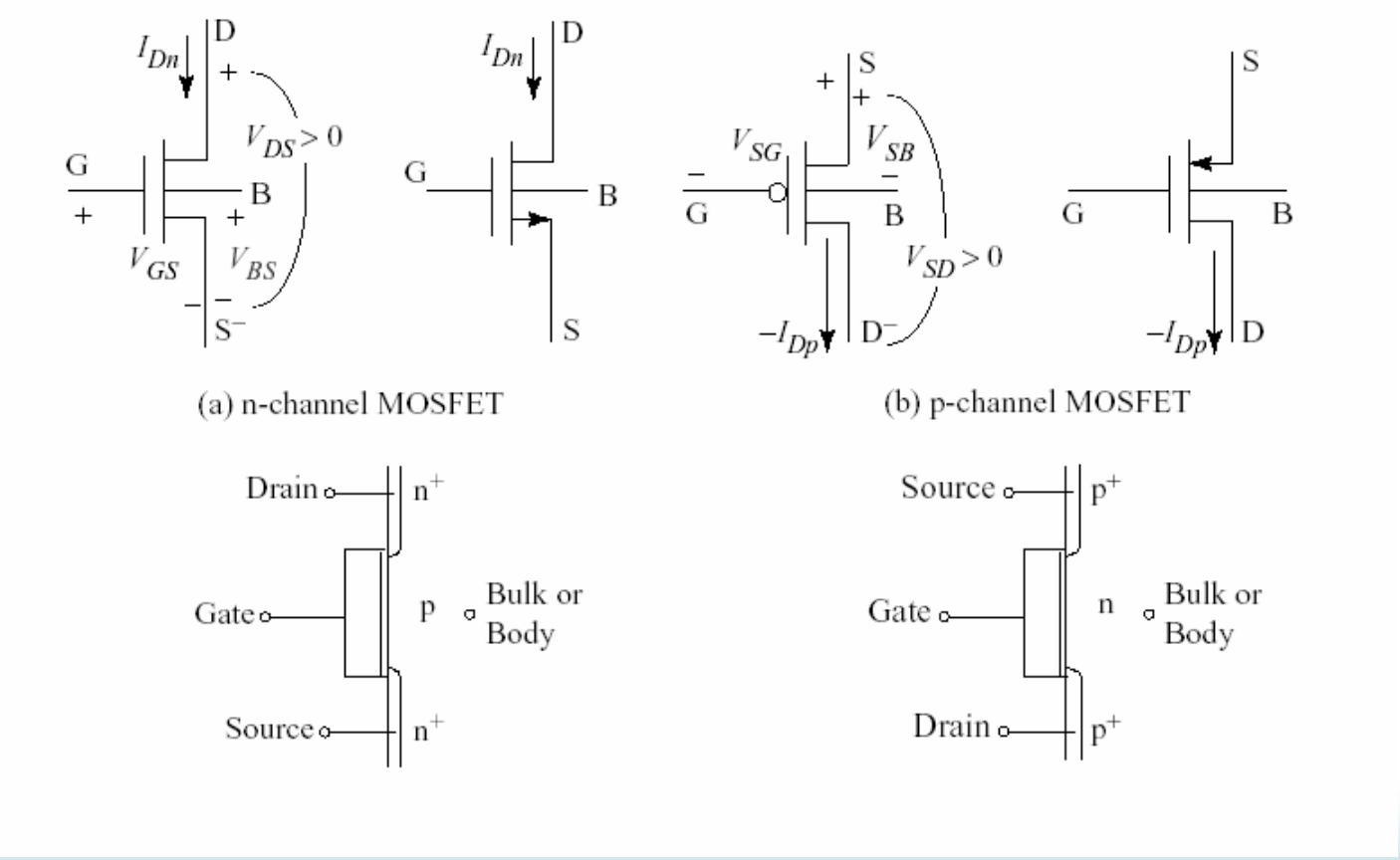
File Edit View Draw Cell Setup Tools Window Help
All Levels
(-6090.000, 2918.000)
Default
N Well
200 x
Inversor
Selection: Instance of cell 'Master_pads'
Mode: Drawing
Start
Inbox ...
3 Wi...
Adobe...
Micros...
3 Int...
L-Edit ...
12:05 PM

El transistor MOS

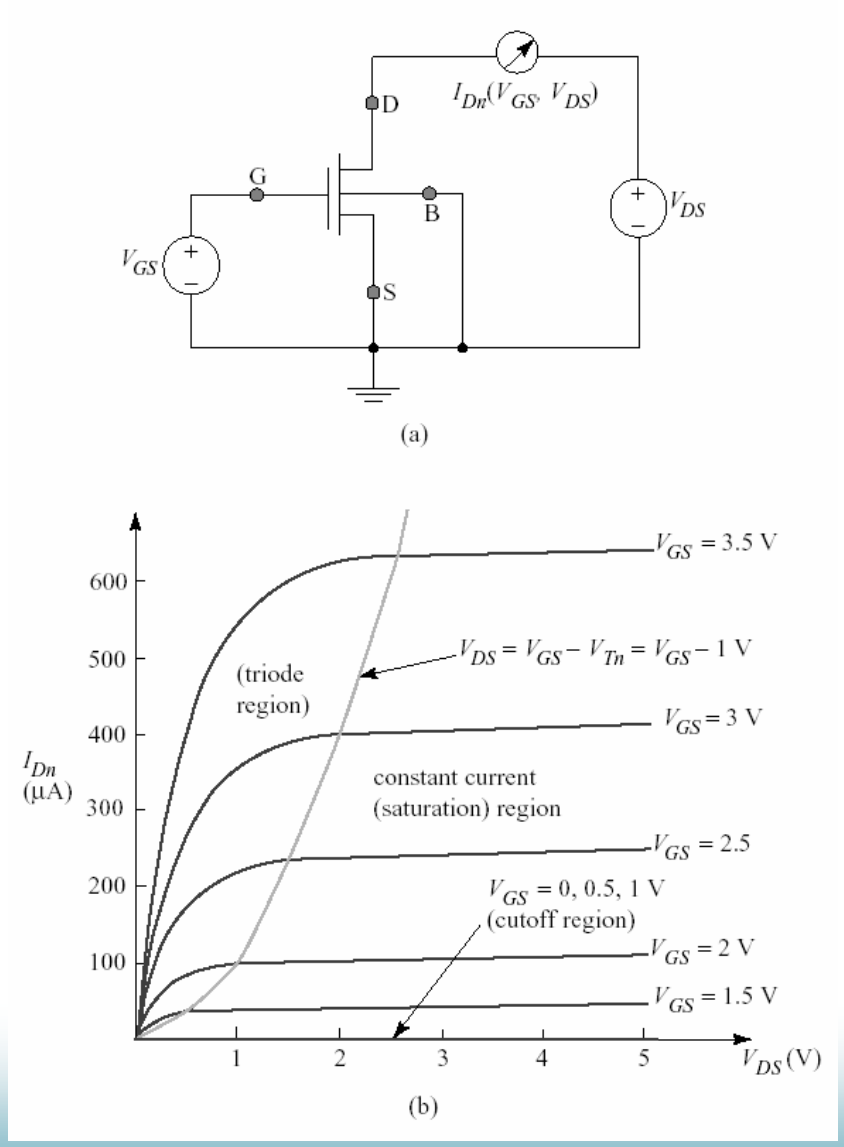
Transistores MOS

- Canal N (sobre sustrato P)
- Canal P (sobre sustrato N)



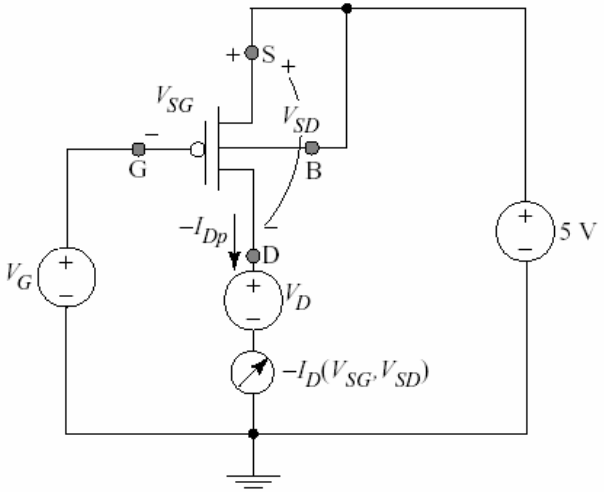
NMOS: Características de Drain

- Ig=0
- Vdb=Vds >0 para que las juntura drain-bulk esté en inversa
- Medición:
  - Bulk a tierra (dispositivo de tres terminales)
  - Se fija Vg
  - Se varía Vds y se mide Id

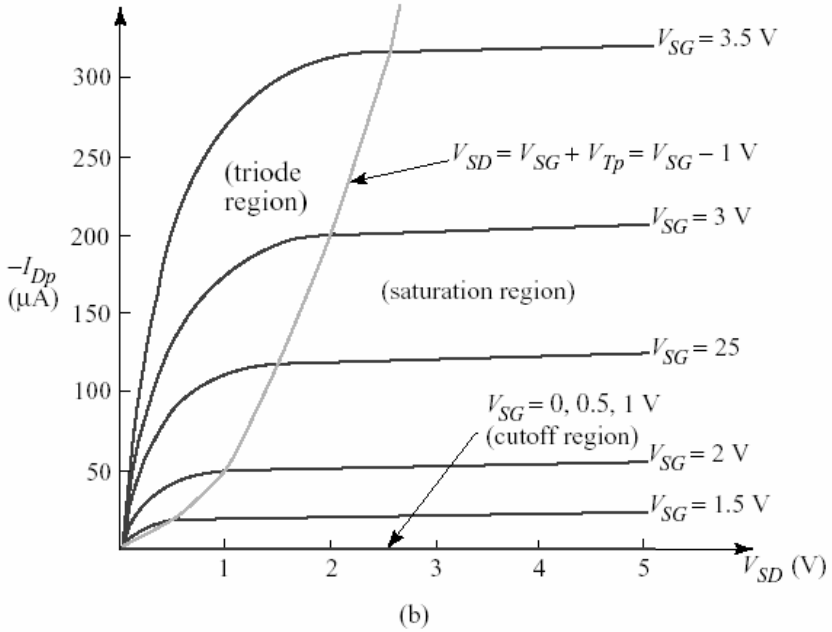


PMOS: Caracterísiticas de drain

- Ig=0
- Vdb=Vds < 0 para que las juntura drain-bulk esté en inversa
- Medición:
  - Bulk a Vdd (dispositivo de tres terminales)
  - Se fija Vg
  - Se varía Vds y se mide Id



(a)



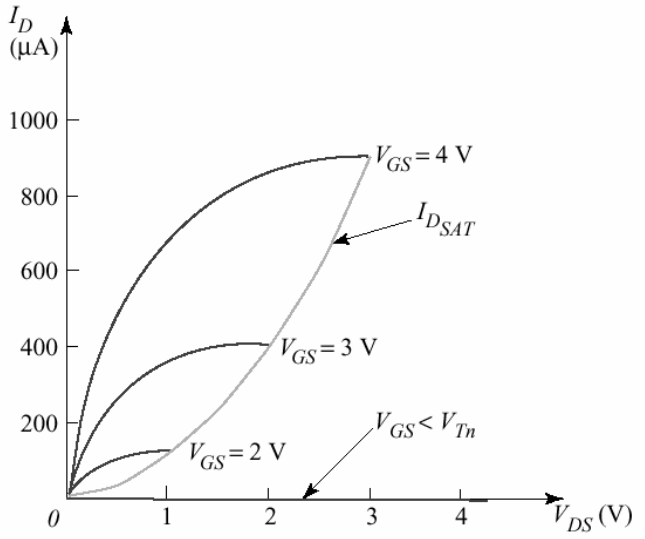
(b)

Regiones de trabajo

- Triodo: Id varía con Vds y Vgs

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn} - V_{DS}/2)V_{DS}$$

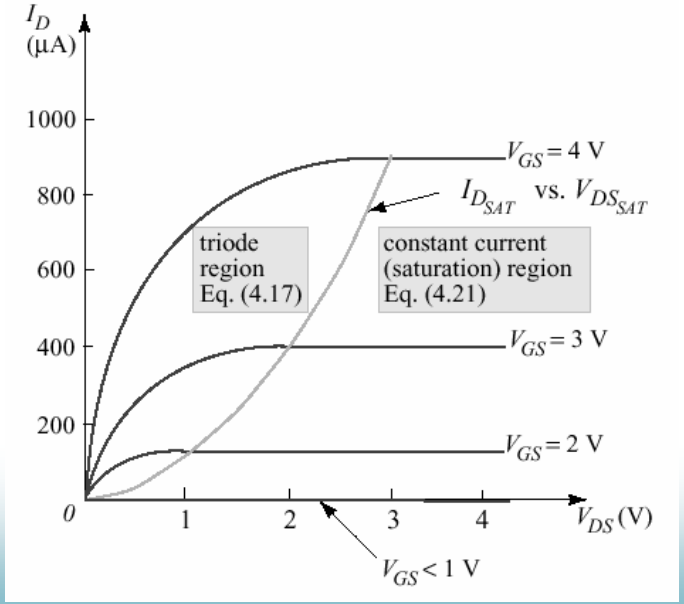
$$V_{GS} - V_{DS} > V_{Tn} \text{ and } V_{GS} > V_{Tn}.$$



- Saturación: Id permanece fija con respecto a Vds

$$I_D = I_{D(sat)} = \mu_n C_{ox}\left(\frac{W}{2L}\right)(V_{GS} - V_{Tn})^2$$

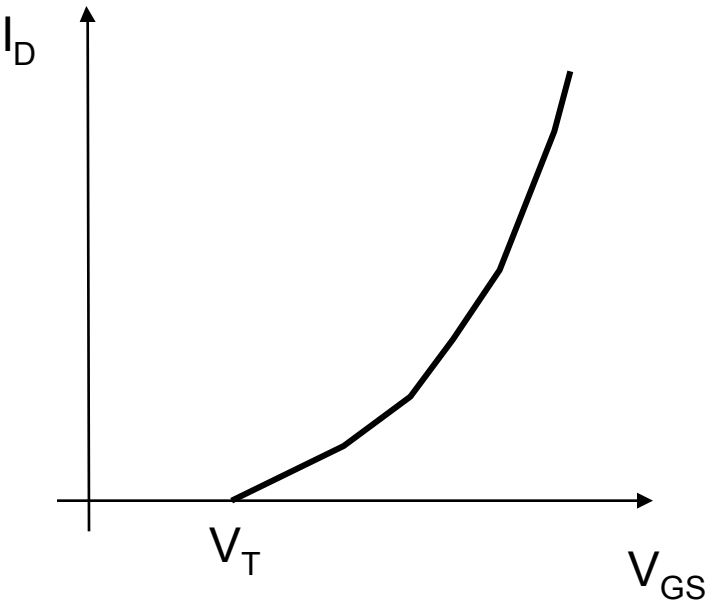
$$V_{GS} > V_{Tn} \text{ and } V_{DS} > V_{DS(sat)} = V_{GS} - V_{Tn},$$



NMOS Transfer curve (Id vs. Vgs)

- Se supone al transistor trabajando en saturación

$$I_D = I_{D(sat)} = \mu_n C_{ox}\left(\frac{W}{2L}\right)(V_{GS} - V_{Tn})^2$$



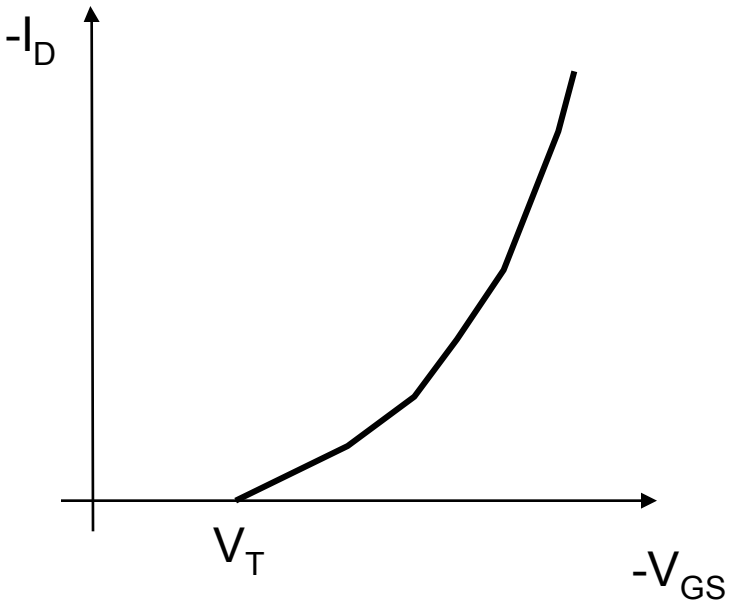
- Para el proceso AMI 0.5 (*)
  - K'n = (Uo*Cox/2)= 55.1 uA/V^2
  - Vgsn=0.75V
  - Si Wn=10um, Ln=2um, Vgs=5V
  - Id = (55e-6)*(10/2)*(5-0.75)^2 = 4.96mA

(*) http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t62r-params.txt

PMOS Transfer curve (Id vs. Vgs)

- Se supone al transistor trabajando en saturación

$$I_D = I_{D(sat)} = -\mu_n C_{ox}\left(\frac{W}{2L}\right)(V_{GS} - V_{Tn})^2$$



- Para el proceso AMI 0.5 (*)
  - K'p = (Uo*Cox/2)= 18.5 uA/V^2
  - Vgsp=-0.93V
  - Si Wp=10um, Lp=2um, Vgs=-5V
  - Id = -18.5e-6*(10/2)*(-5+0.93)^2 = -1.50 mA

(*) http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t62r-params.txt

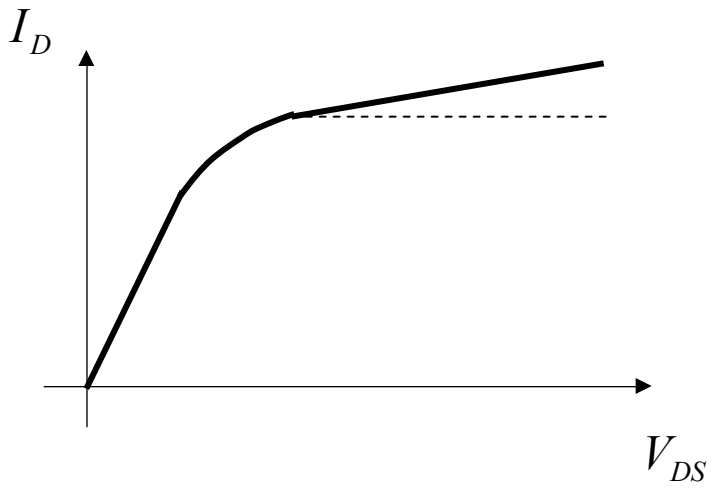
Características de salida

- Expresión corregida:

$$I_D = 1/2 \frac{W}{L} \mu_n C_{ox} (V_{gs} - V_t)^2 (1 + \lambda V_{DS})$$

- La impedancia de salida

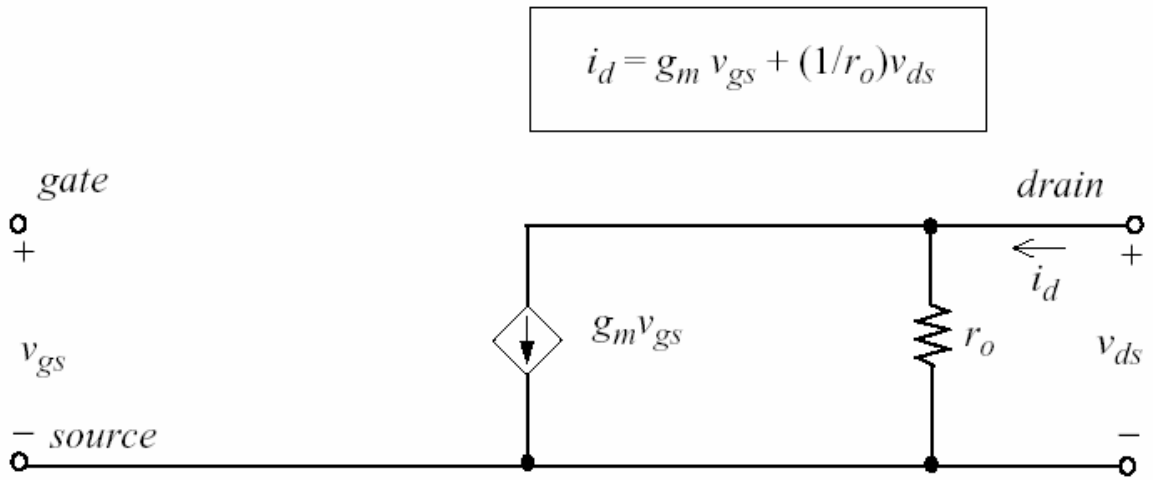
$$\frac{\partial I_D}{\partial v_{ds}} = \lambda I_D$$



$$\lambda = \frac{0.1}{L} [\mu m/V]$$

Cuanto más largo el canal mayor impedancia de salida

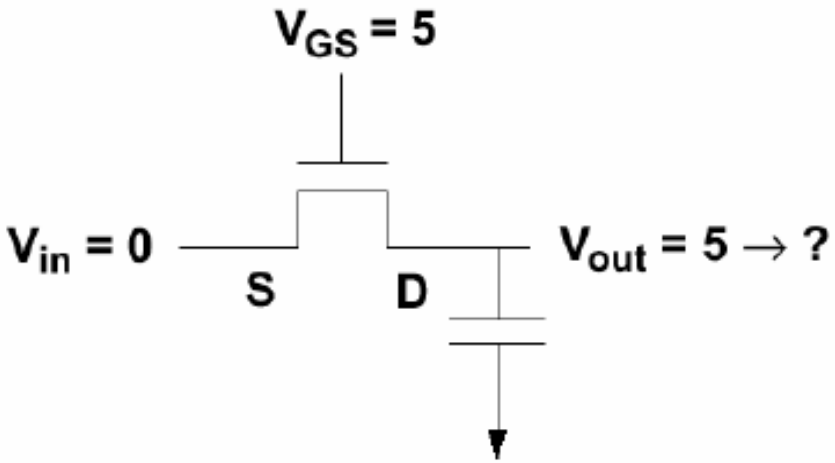
Modelo de pequeña señal

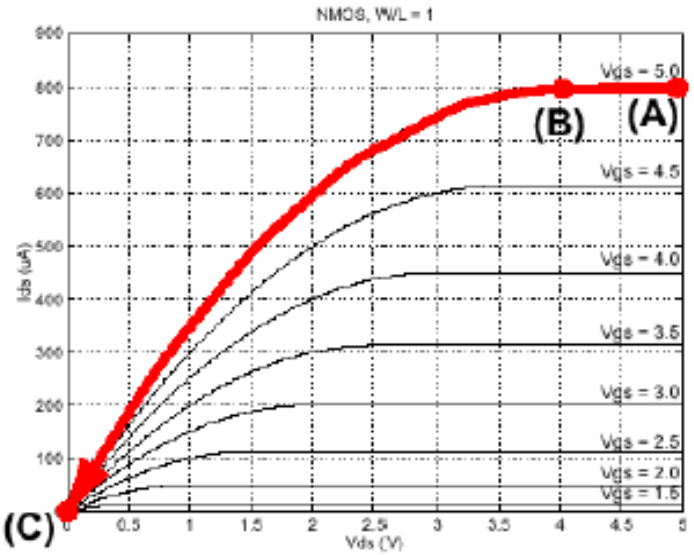


El transistor como llave

Switches

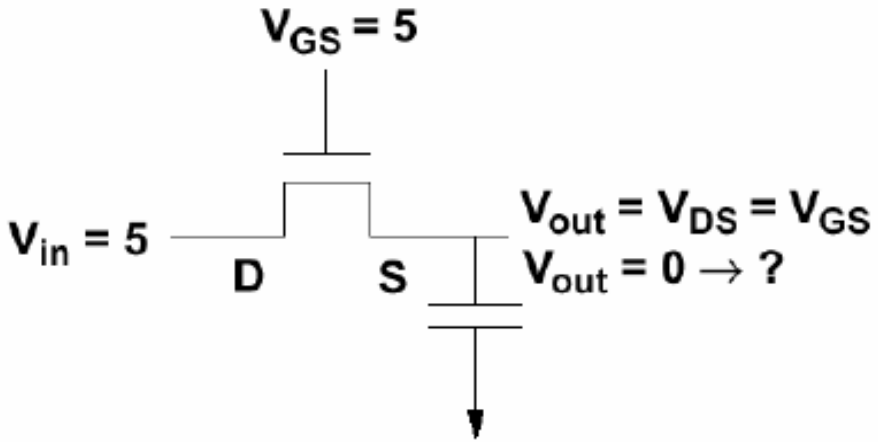
NMOS Pass Transistor—Passing 0

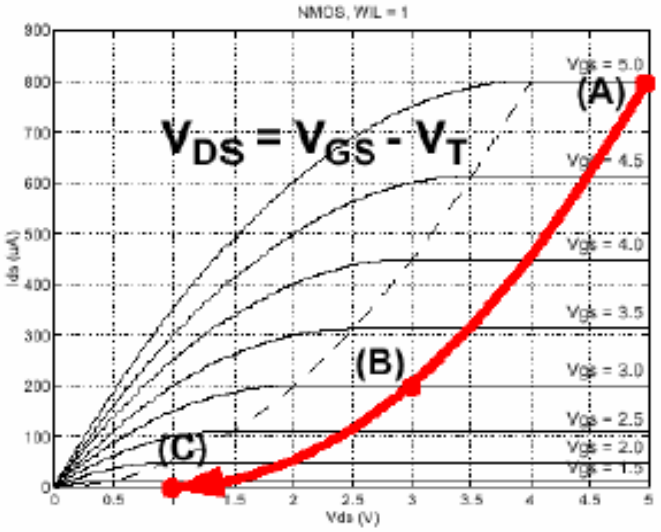




Switches

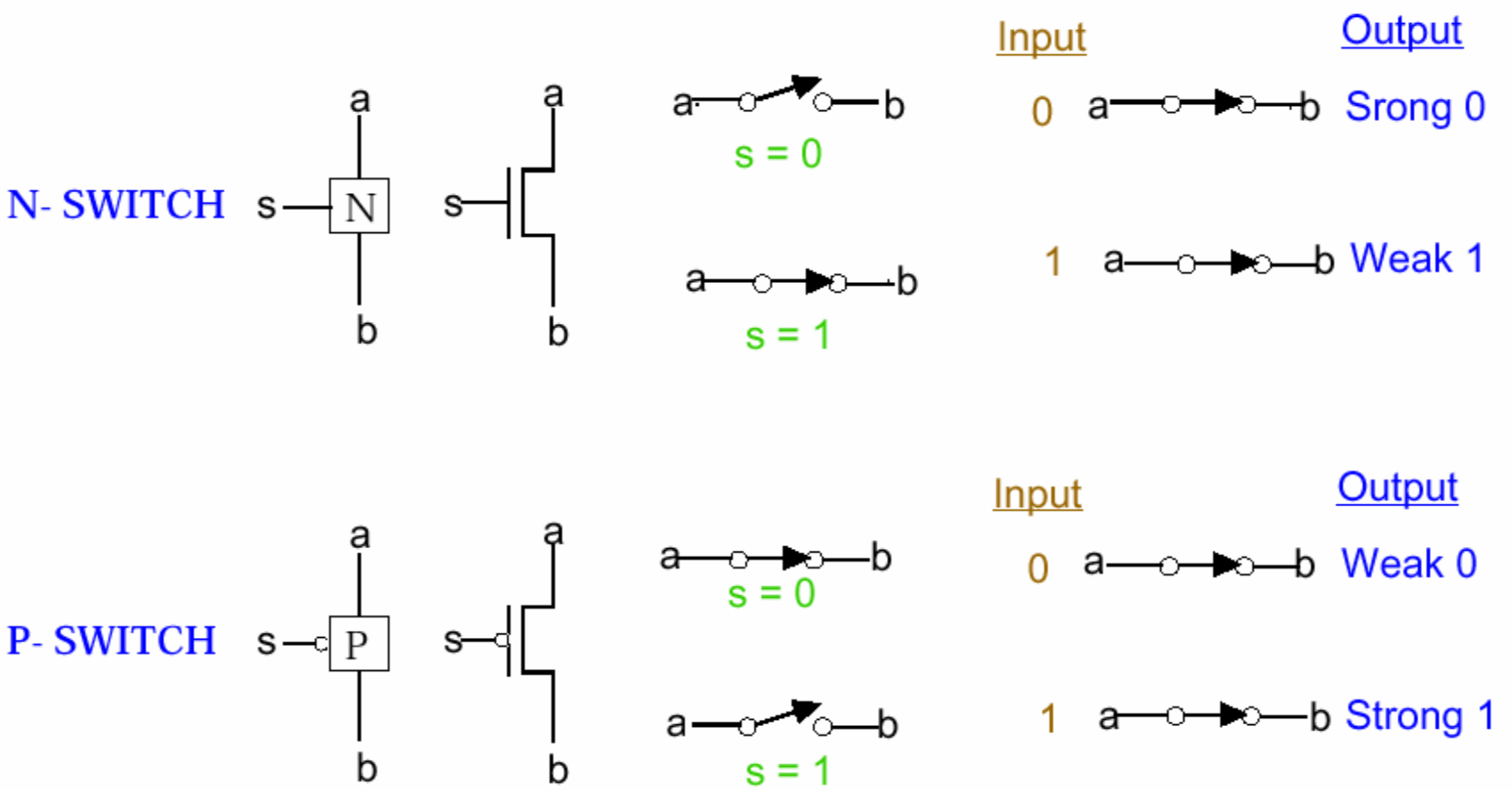
NMOS Pass Transistor—Passing 1





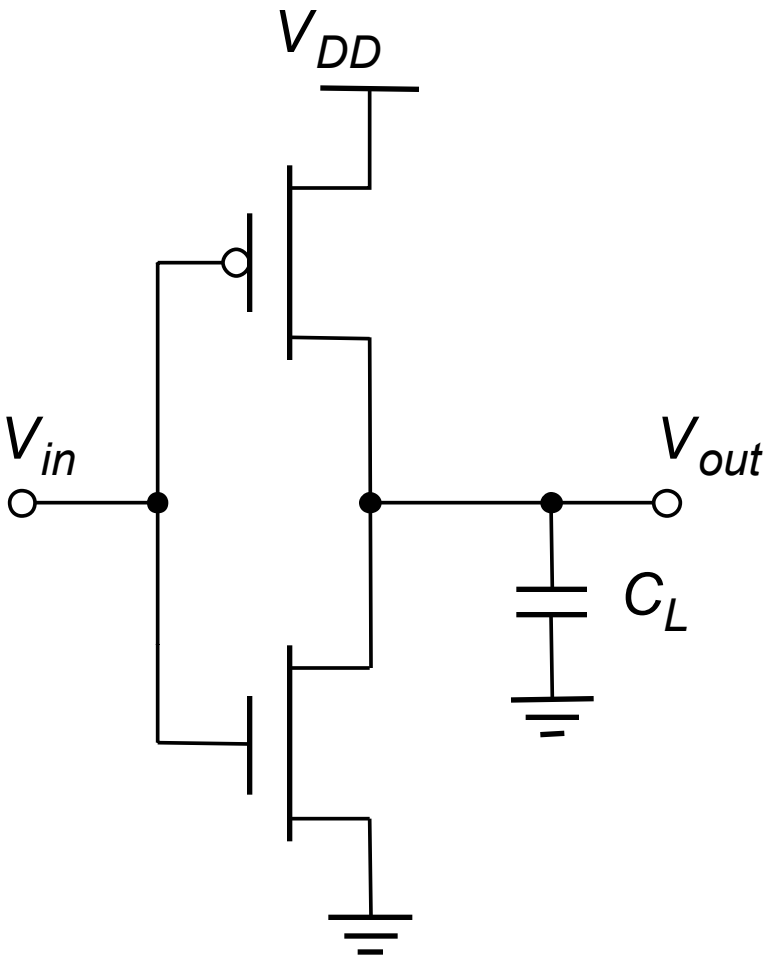
Threshold Drops

Switches


N- SWITCH
s
N
a
b
s = 0
s = 1
Input
Output
0
Srong 0
1
Weak 1
P- SWITCH
P
Weak 0
Strong 1

El inversor

El inversor CMOS

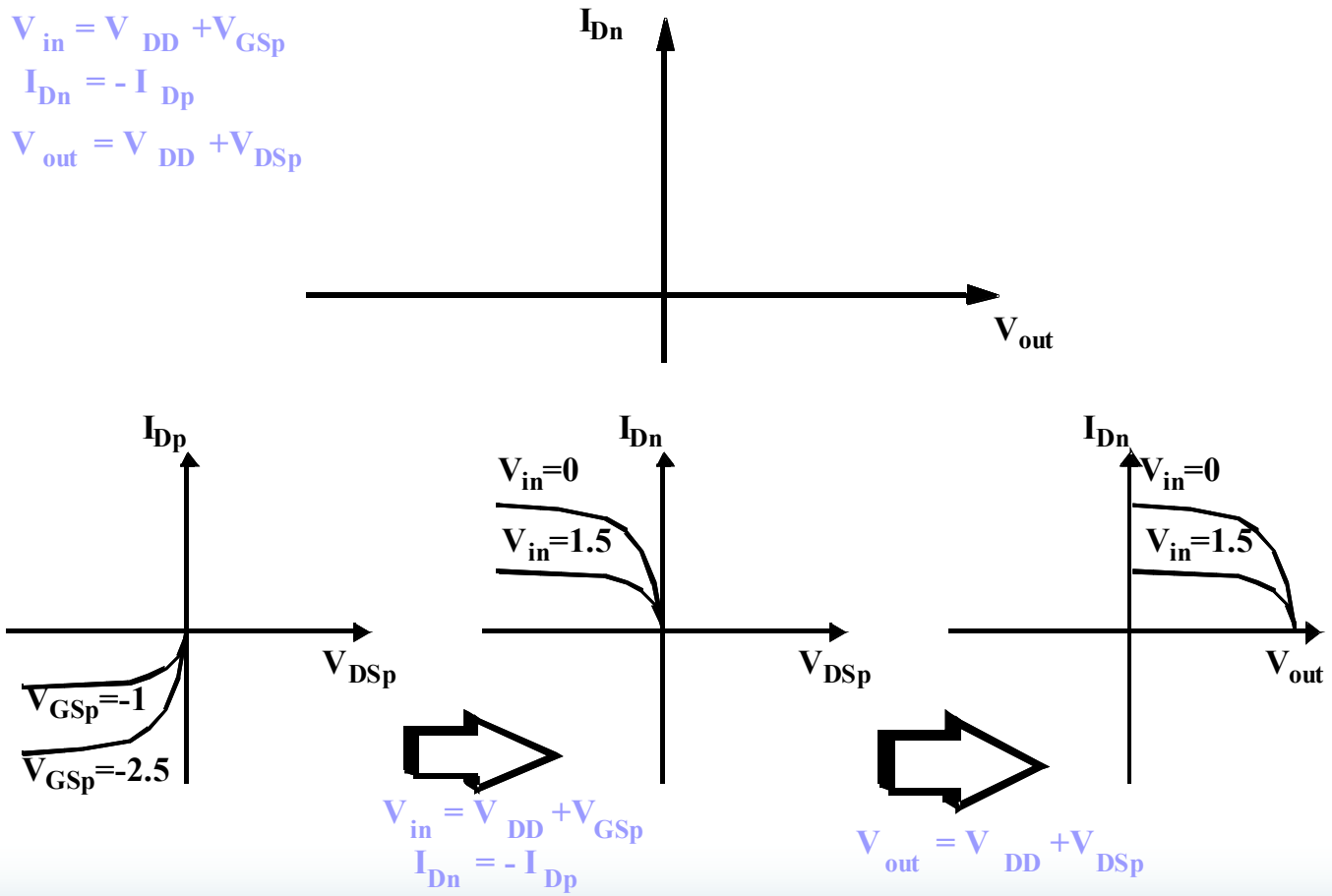


Rectas de carga de un PMOS

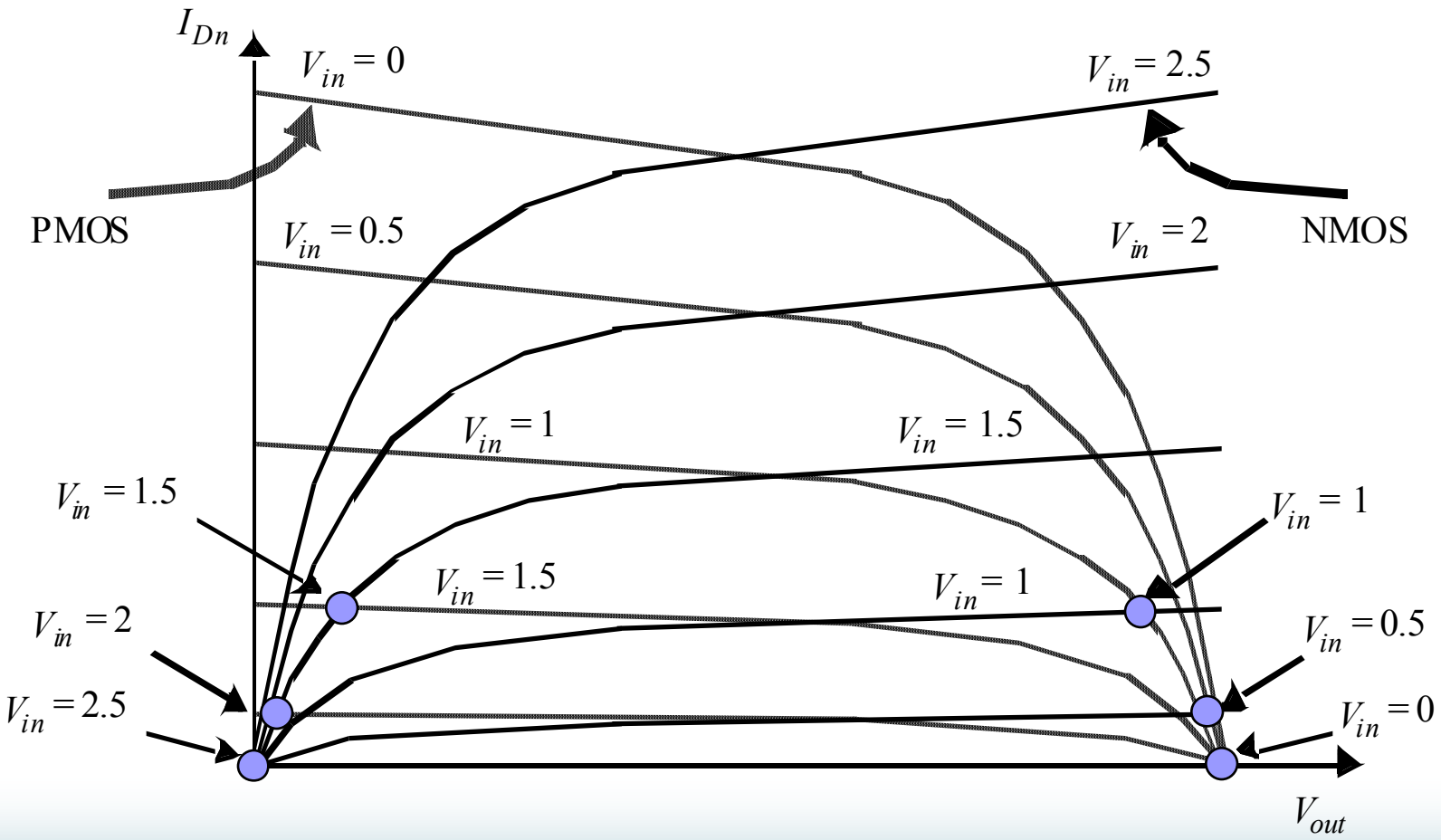
$V_{in} = V_{DD} + V_{GSp}$

$I_{Dn} = -I_{Dp}$

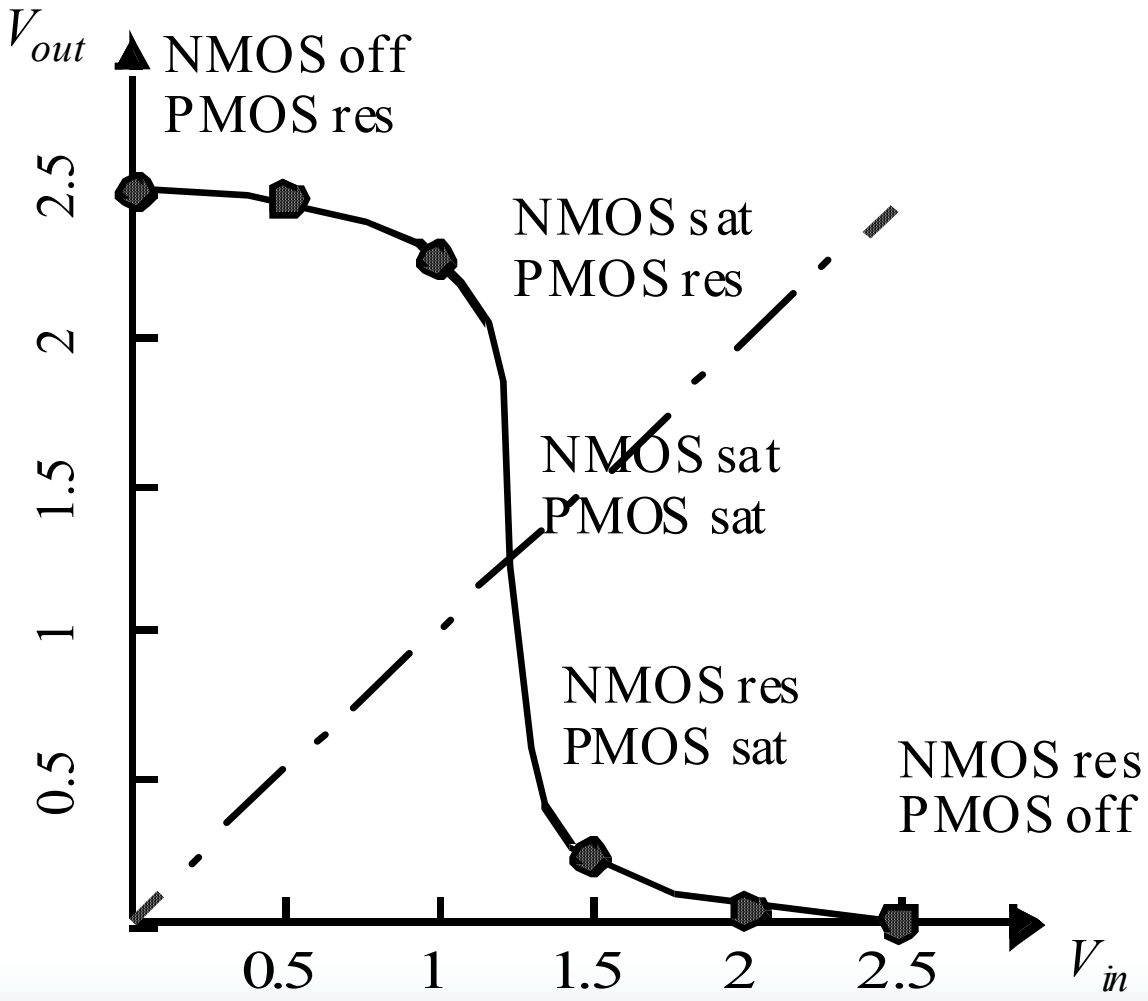
$V_{out} = V_{DD} + V_{DSp}$



CMOS Inverter Load Characteristics

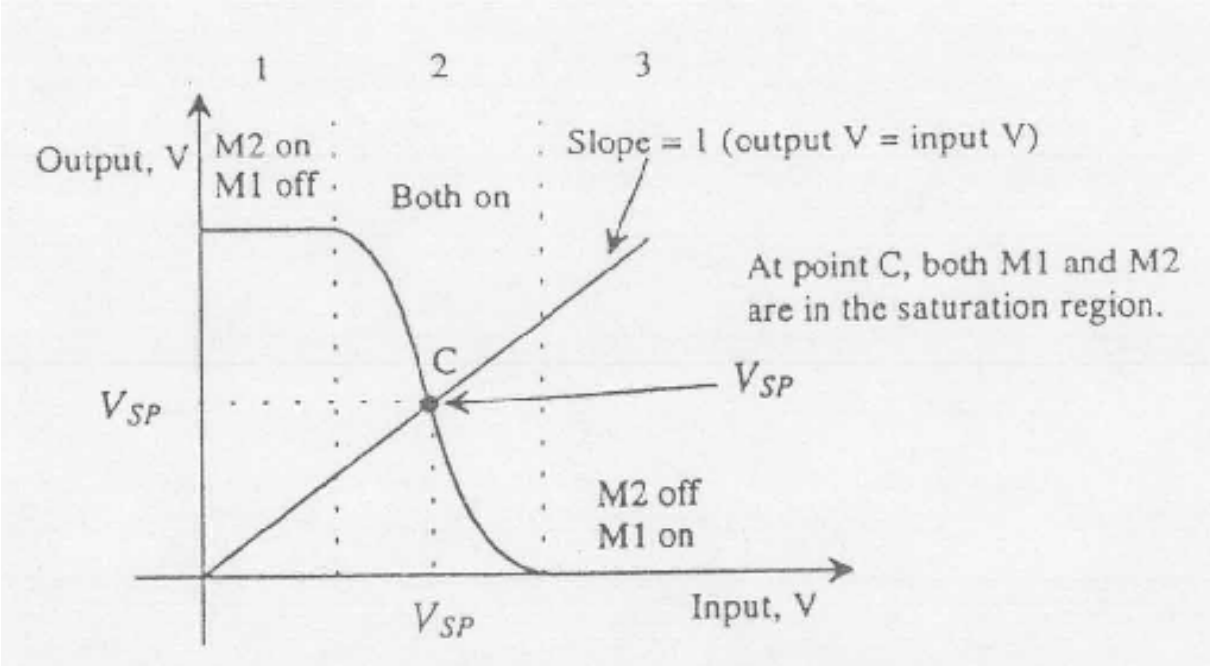


CMOS Inverter VTC



The Switching Threshold

- Switching threshold V_M is defined as the point where Vin = Vout



Switching Threshold as a function of Transistor Ratio

- Switching threshold V_M is defined as the point where Vin = Vout

$$K_n \frac{W_n}{L_n}\left(V_M - V_T\right)^2 = K_p \frac{W_p}{L_p}\left(Vdd - V_M - V_T\right)^2$$

- Yielding V_M as a function of transistor geometries, threshold voltages and Vdd

$$V_M = \frac{\sqrt{\beta_n / \beta_p}\, V_{Tn} + (Vdd - V_{Tp})}{1 + \sqrt{\beta_n / \beta_p}}$$

Transistor Ratio Setting

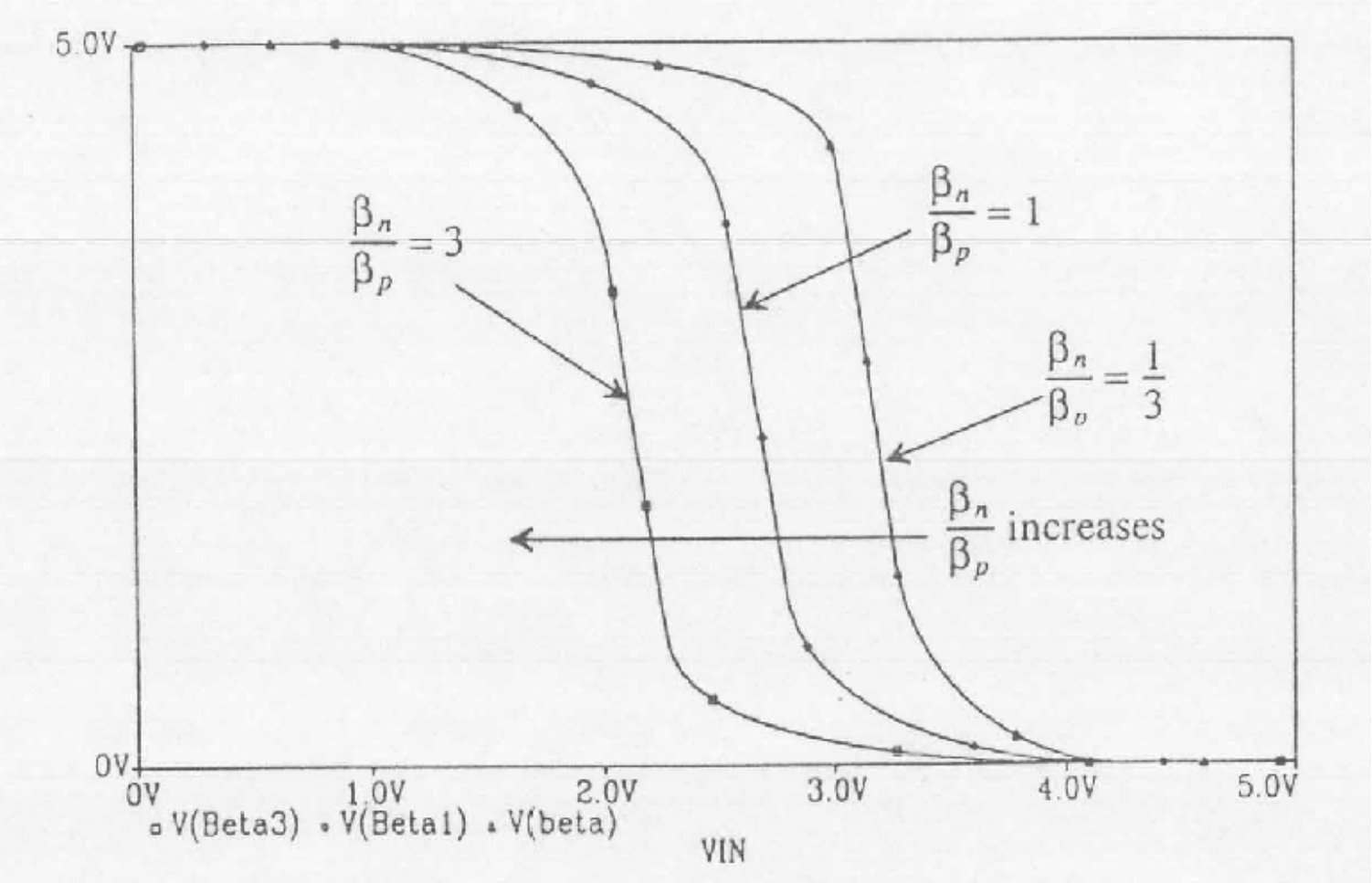
- With V_M = Vdd/2 the right hand side equals, in general to 1, so that

$$\frac{K_n S_n}{K_p S_p} = \frac{\left(Vdd - V_M - V_T\right)^2}{\left(V_M - V_T\right)^2}$$

$$\frac{S_n}{S_p} = \frac{K_p}{K_n}$$

- P transistor wider than N for equal margins

Switching Threshold



Power Dissipation

Where Does Power Go in CMOS?

- Dynamic Power Consumption

  Charging and Discharging Capacitors

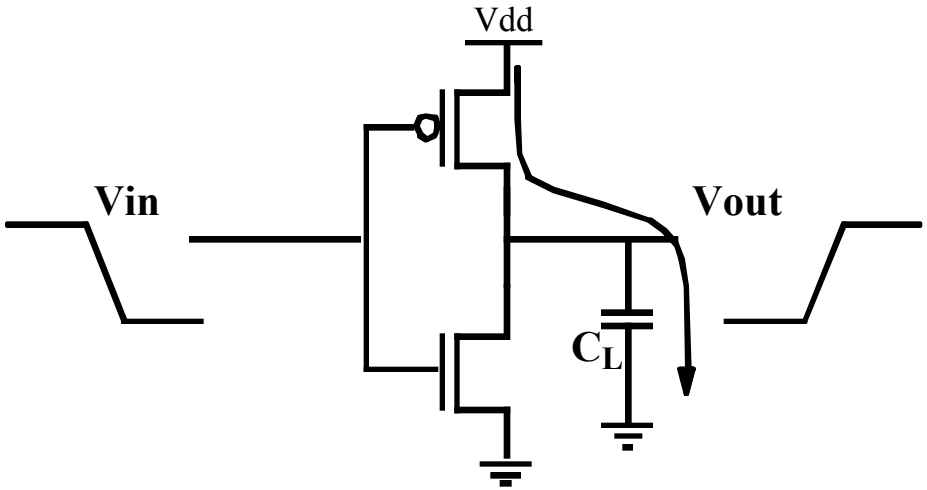
- Short Circuit Currents

  Short Circuit Path between Supply Rails during Switching

- Leakage

  Leaking diodes and transistors

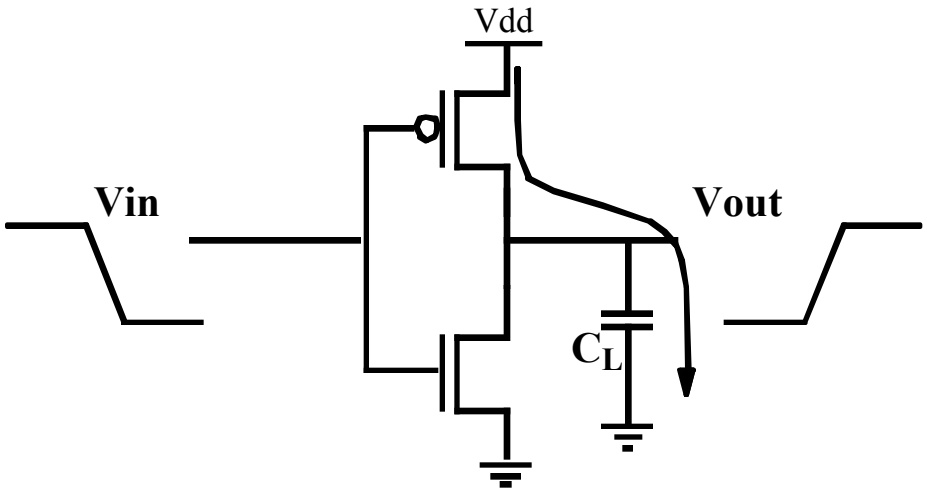
Dynamic Power Dissipation



$$E_{Vdd} = \int_0^\infty i_{Vdd}(t) Vdd \; dt = Vdd \int_0^\infty C_L \frac{dv_{out}}{dt} dt = C_L \int_0^{Vdd} dv_{out} = C_L Vdd^2$$

$$E_C = \int_0^\infty i_{Vdd}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{Vdd} v_{out} dv_{out} = \frac{C_L Vdd^2}{2}$$

Dynamic Power Dissipation



$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L, V_{dd}, and f to reduce power.
- Dependence with supply voltage is quadratic !!!

Node Transition Activity and Power

- Consider switching a CMOS gate for *N* clock cycles

$$E_N = C_L \bullet V_{dd}^2 \bullet n(N)$$

E_N : the energy consumed for *N* clock cycles

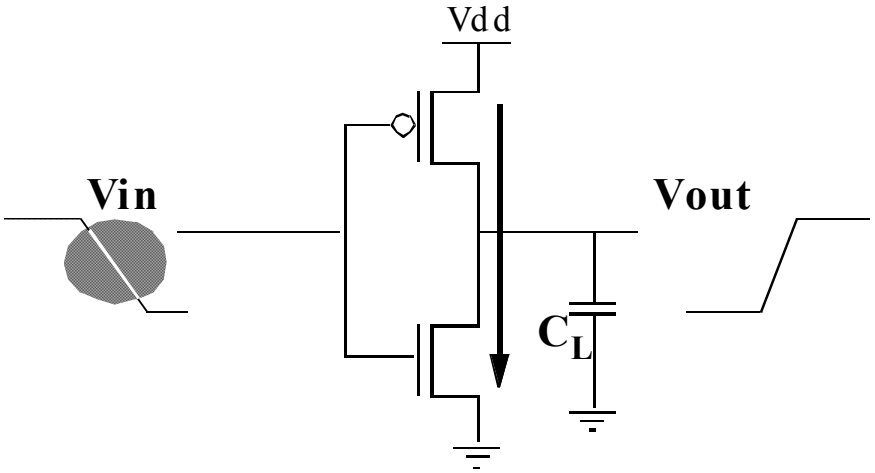
$n(N)$: the number of 0->1 transition in *N* clock cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \bullet f_{clk} = \left(\lim_{N \to \infty} \frac{n(N)}{N} \right) \bullet C_L \bullet V_{dd}^2 \bullet f_{clk}$$

$$\alpha_{0 \to 1} = \lim_{N \to \infty} \frac{n(N)}{N}$$

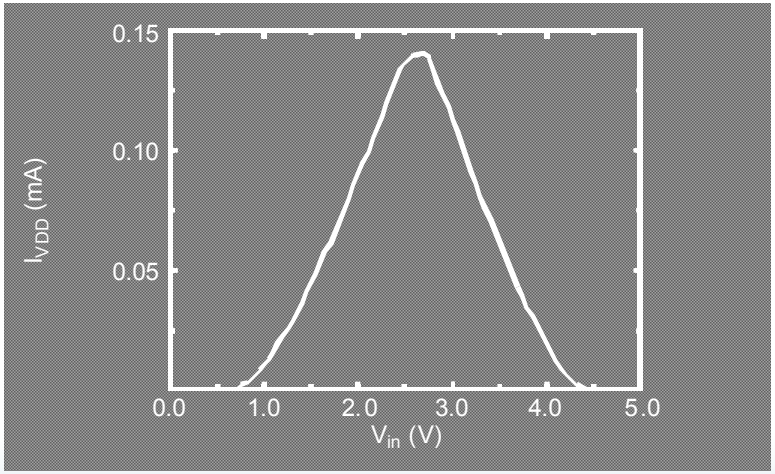
$$P_{avg} = \alpha_{0 \to 1} \bullet C_L \bullet V_{dd}^2 \bullet f_{clk}$$

Short Circuit Currents

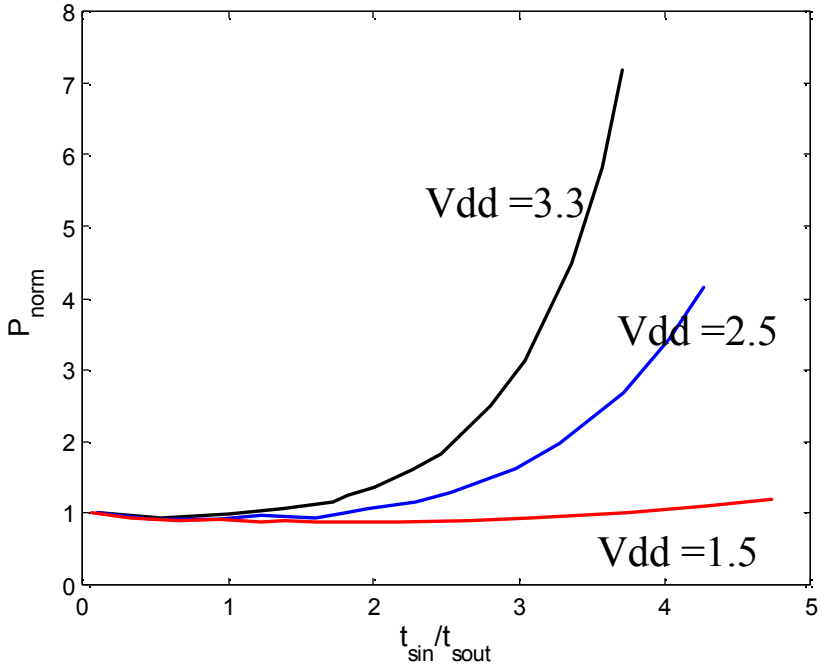


I peak is a function of transistor sizes.

It is also a strong function of the input and output slopes …

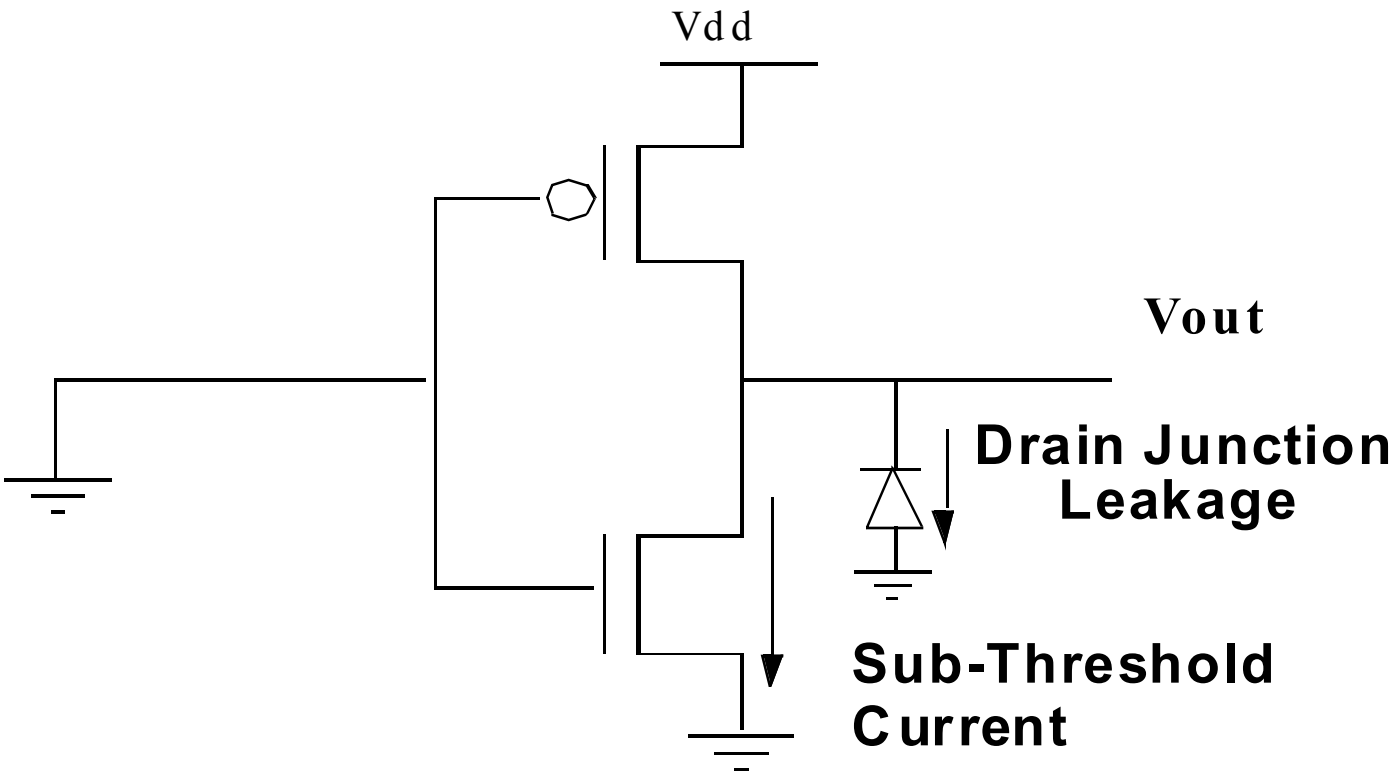


Minimizing Short-Circuit Power



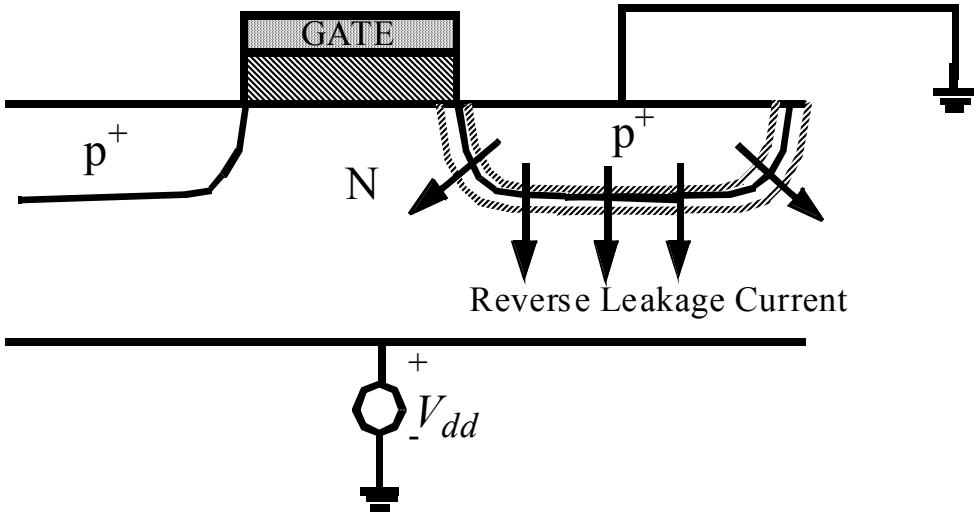
- Keep the input and output rise/fall times the same
  (< 10% of Total Consumption)
  from [Veendrick84]
  (***IEEE Journal of Solid-State Circuits*, August 1984**)
- If $V_{dd} < V_{tn} + |V_{tp}|$ then short-circuit power can be *eliminated*!

Leakage



Sub-threshold current one of most compelling issues in low-energy circuit design!

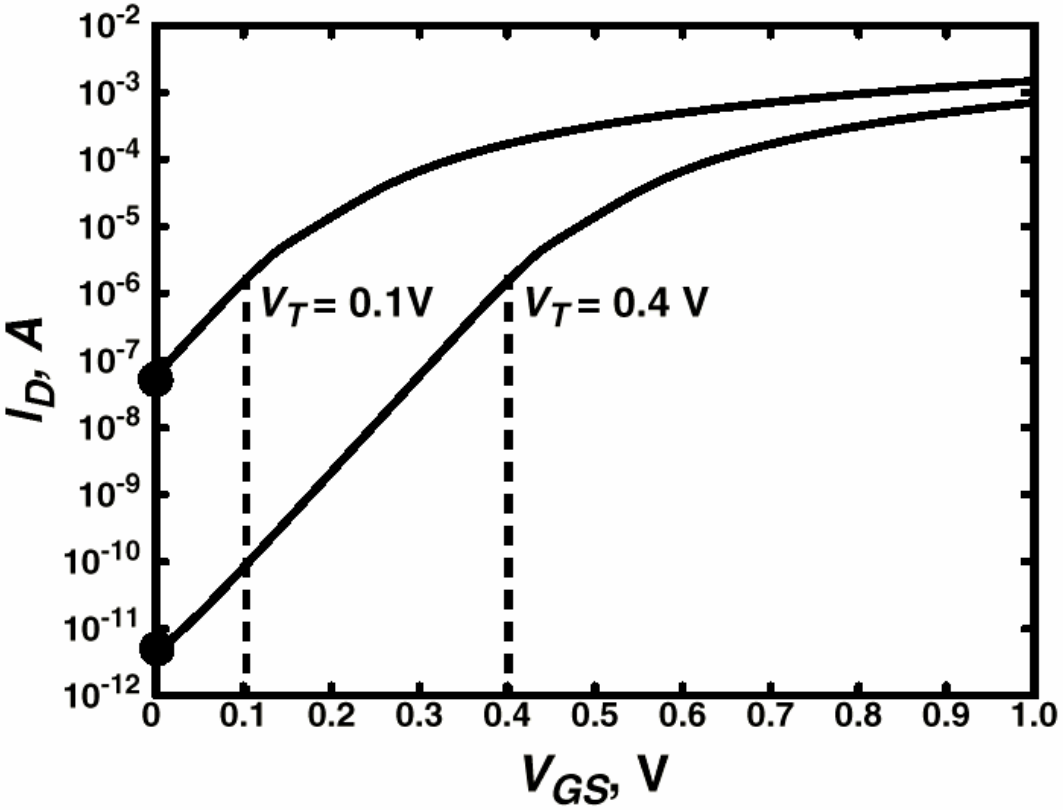
Reverse-Biased Diode Leakage

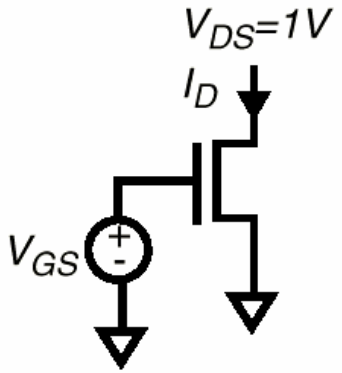


$$I_{DL} = J_S \times A$$

***JS* = 10-100 pA/μm2 at 25 deg C for 0.25μm CMOS**
***JS* doubles for every 9 deg C!**

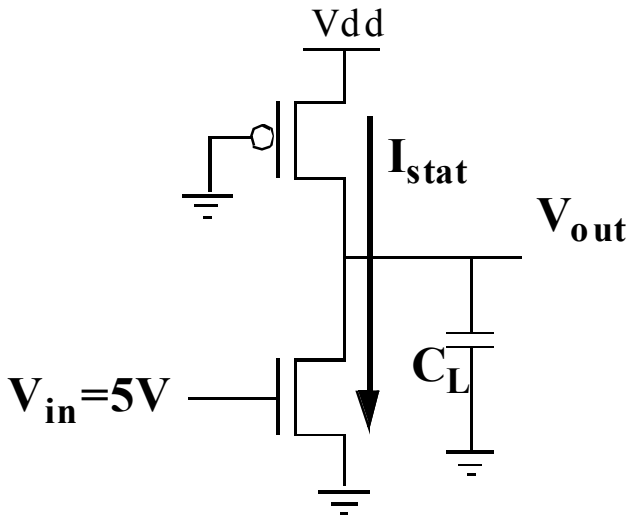
Subthreshold Leakage Component





- Leakage control is critical for low-voltage operation

Static Power Consumption



$$P_{stat} = P_{(In=1)}.V_{dd} \cdot I_{stat}$$

Wasted energy …
Should be avoided in almost all cases,
but could help reducing energy in others (e.g. sense amps)

Principles for Power Reduction

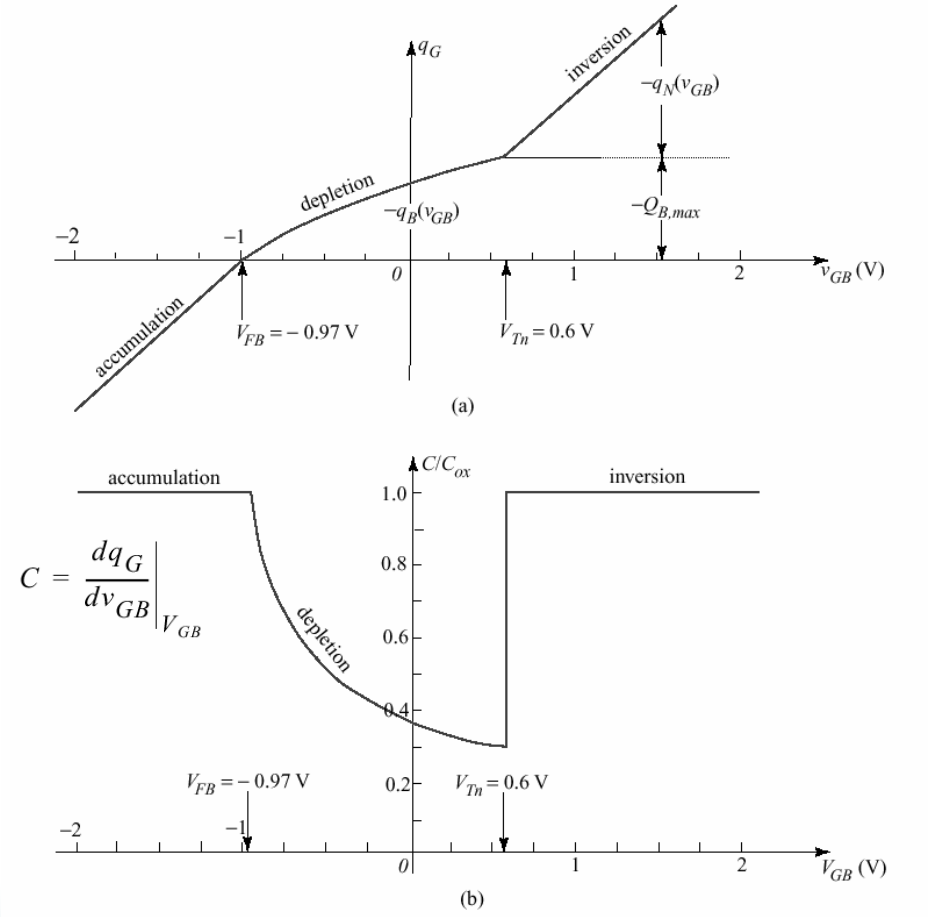
- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 … 0.9 V by 2010!)
- Reduce switching activity
- Reduce physical capacitance

Background Material

- Semiconductor Physics and carrier modelling: Chapter 2, 3, Howe Sodini; Chapter 2, Robert Pierret.
- MOS modelling: Chapter 4, Howe Sodini; Chapter 16-18, Robert Pierret.

Apéndice

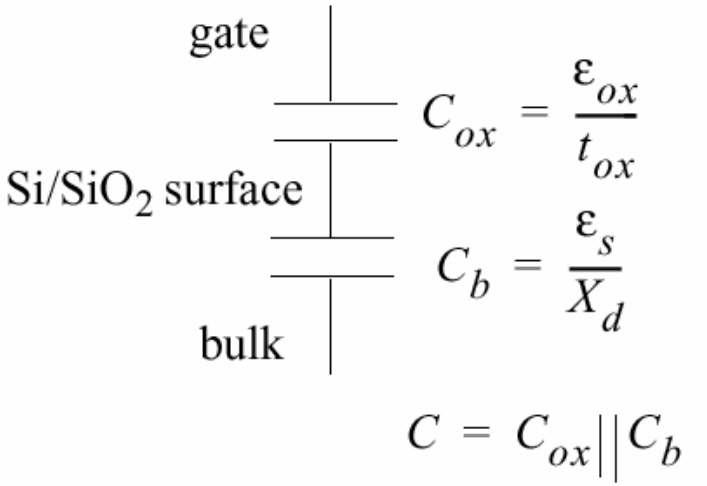
The capacitance



- Accumulation

$$C = C_{ox}$$

- Depletion



$$C = C_{ox} \,||\, C_b$$

- Inversion

$$C = C_{ox}$$

Como accedemos localmente ?

- MOSIS (www.mosis.org)
- Precios de descuento para miembros de LACIS (bajo volumen):
  - 2.2mm x 2.2mm (AMI 1.5µm) 980US$/4 = 246US$ 5 unidades
  - 1.5mm x 1.5mm (AMI 0.5µm) 5000US$/4 = 1250US$ 5 unidades
- Mayores volúmenes implican menores costos