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Del Lab a la Fab

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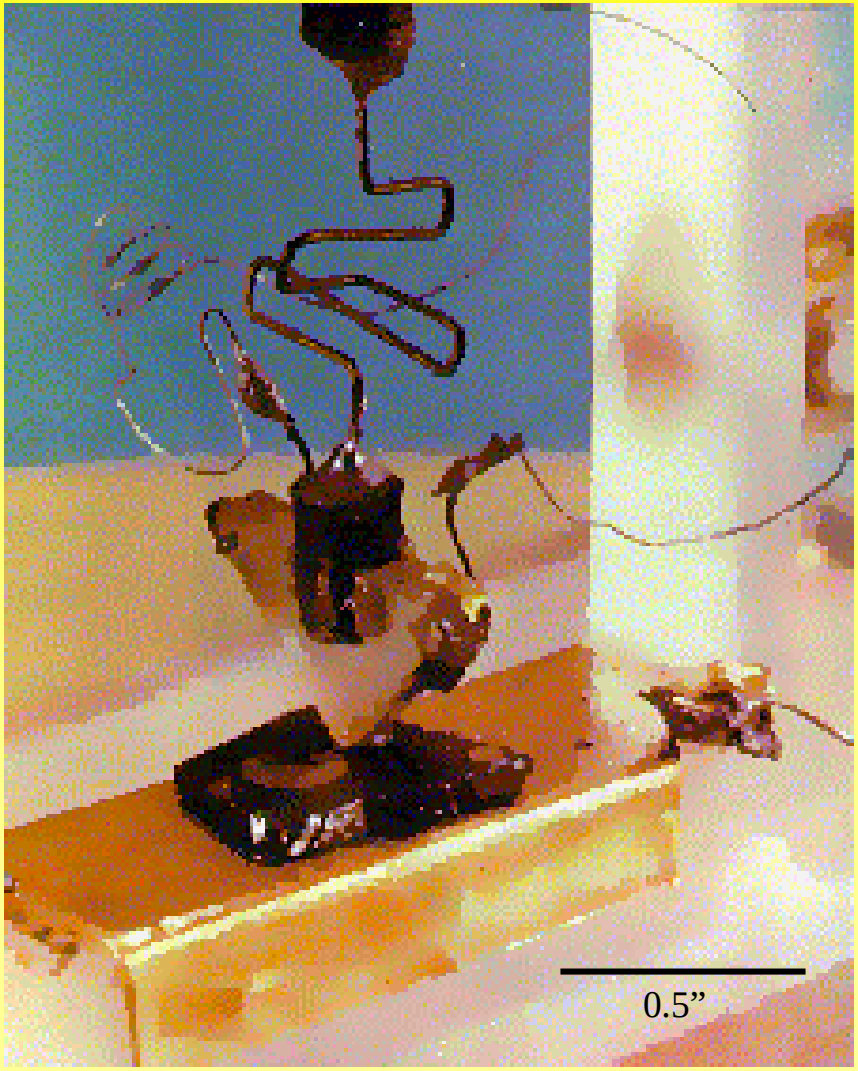
Primera época 1947-1960

- 1947 transistor (SBB, Bell Labs)
- 1947-50 Monocristales
- 1950-55 junturas grown, alloy, diffusion
- 1958 IC (Kilby, Texas)
- 1960 Hoerni aprovecha las prop de Si-SiO2 para diseñar prceso planar
- 1960 primer familia TTL (bip)
- 1960 MOS sobre Si (Atalla)

Birth of an Era – 1947, Bell Laboratories



The first transistor made of Germanium

INVENTORS Shockley (*seated*), Bardeen (*left*) and Brattain (*right*) were the first to demonstrate a solid-state amplifier (*opposite page*).

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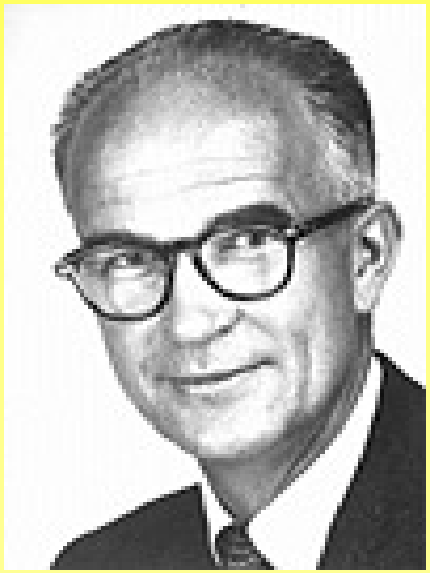
The Nobel Prize in Physics 1956

"for their researches on semiconductors and their discovery of the transistor effect"



William Bradford Shockley

John Bardeen

Walter Houser Brattain

Single crystals and junction transistor

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1947-Point contact Transistor

1947-1950 Single crystal work leading to the Teal-Little, or Czochralsky (1918) crystal growth technique

"Bill Shockley was opposed to the work on germanium single crystals when I suggested it, because, as he has publicly stated on several important occasions, he thought that transistor science could be elicited from small specimens of polycrystalline masses of material."

Teal

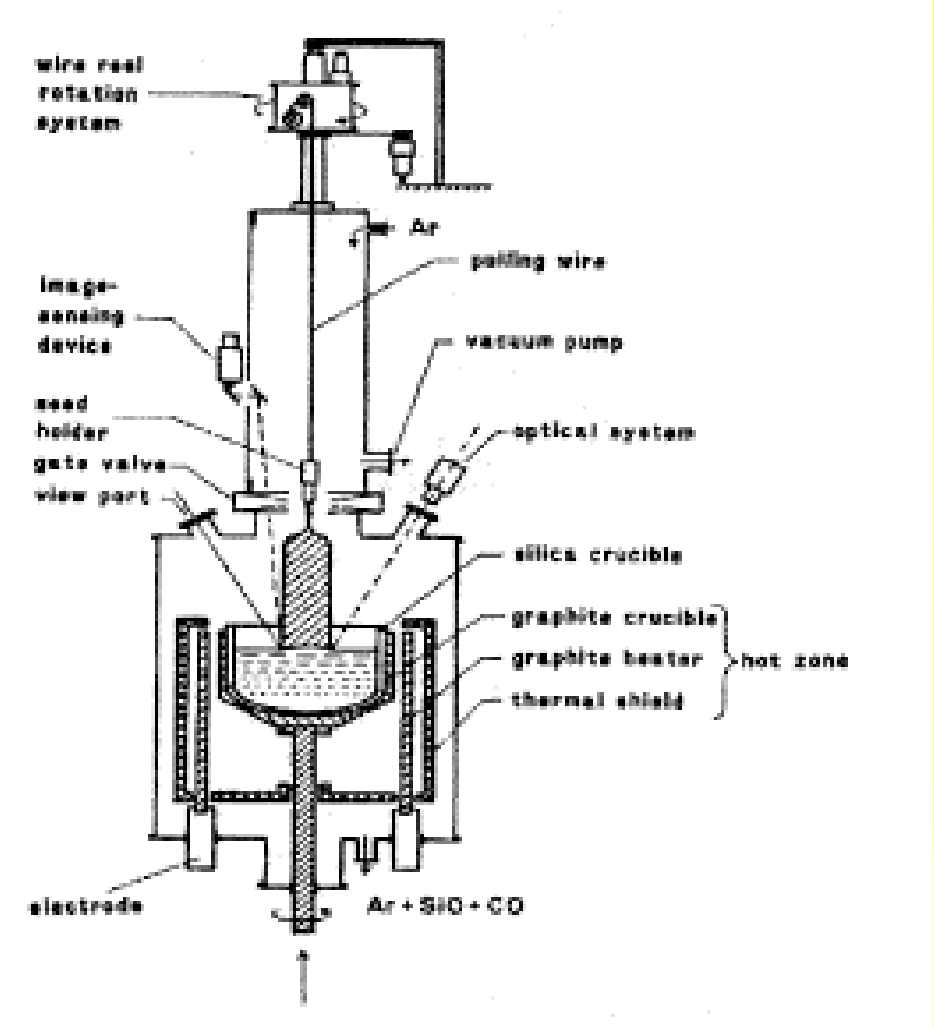
1950 – Junction Diode

G.K. Teal, U.S. Patent No. 2,727,840, Filed June 15, 1950, Issued Dec. 20, 1955

1951 – Junction Transistor

W. Shockley, M. Sparks and G.K. Teal, P-N Junction Transistors, Phys. Rev., **83**, 151-162 (1951)

Teal-Little or CZ crystal growth



single crystal material, however, facilitated experimental verification of a number of quantum theoretical concepts developed for electrons and holes in crystalline semiconductors such as effective mass, drift and conductivity mobility, carrier lifetime and tunneling [6,58] and clarification of a number of phenomena in p-n junctions [87] and, indeed, exhibited significantly improved characteristics compared to polycrystalline samples. For example, Haynes observed in early 1949 that the lifetime of minority carriers in single crystals of germanium was as much as 140 μs (20 to 300 times greater than observed in polycrystalline germanium) and mobilities three to four times higher, due to the greater perfection and purity (45 ohm-cm) of the single crystals [6,58,88-90]. Teal also reported injected carrier lifetimes greater than 200 μs in single crystal germanium as compared to significantly lower carrier lifetimes of 1-5 μs in polycrystalline

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Hacia el transistor de Si

- **Esfuerzos en Si CZ, melting point 1452 °C frente a 920 °C de Ge. Contaminación impurezas crucible. Gettering.**

- **1952 Primer dispositivo de Si: diodo p-n formado con alambre de Al aleado a sustrato n-Si.**
- **1954 Primer junction Si transistor comercial. Aumenta la potencia de salida y dobla el rango de temperatura respecto a Ge.**

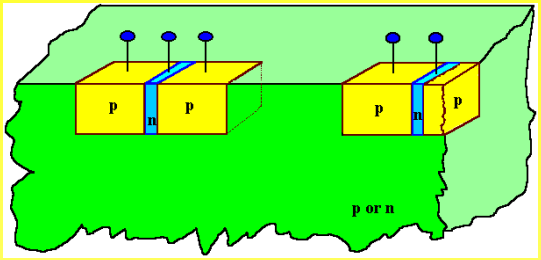
G.L. Pearson and B. Sawyer, Silicon P-N Junction Alloy Diode, Proc. IRE, 40, 1348-1351 (1952)

G.K. Teal, Some Recent Developments in Silicon and Germanium Materials and Devices, Nat'l IRE Conf., Dayton, May 10, 1954

Éste es el dispositivo que empujó la electrónica a múltiples aplicaciones y dominó los circuitos hasta el MOS

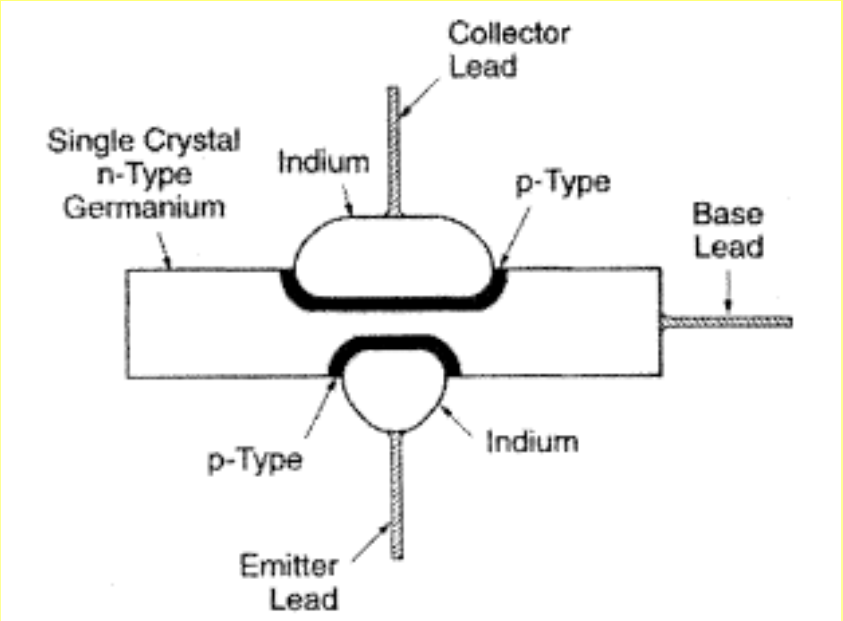
Hacia el transistor Si juntura difundida

- **El mayor problema del transistor de juntura fabricada durante el crecimiento del cristal: el control de ancho de base (cutoff freq 1-10 MHz contra 100 MHz de los point contact), y su conexionado.**



J.E. Saby, Fused Impurity p-n-p Transistors, Proc. IRE, **40**, 1358-1360 (1952)

- **1952 Transistor de aleación (Saby) resuelve el problema del contacto. Algunas ventajas pero no gana en frecuencia.**



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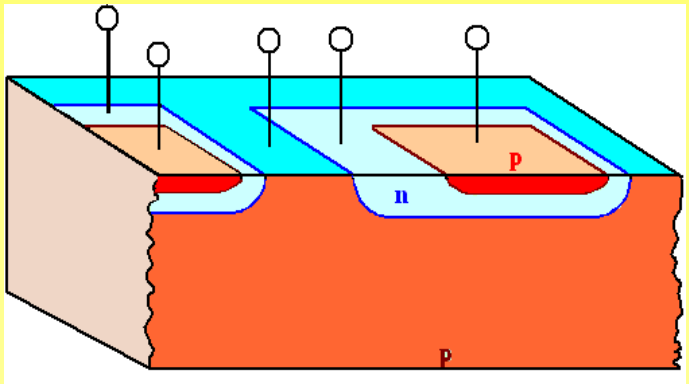
El transistor Si juntura difundida

- **1951-Patente de sistema de juntura por difusión en sólido.**
- **1955 –Primeras implementaciones en dispositivos. Diodo de 400 V reverse, 400 mA direct.**
- **1955 Transistor de 500 MHz (1 µm base).**

J.H. Scaff and H.C. Theurerer, Semiconductor Comprising Silicon and Method of Making It, U.S. Patent No. 2,567,970, filed Dec. 24, 1947, Issued Sept. 18, 1951

M.B. Prince, Diffused P-N Junction Silicon Rectifiers, Bell Syst. Tech. J., **35**, 661-684 (1955)
C.A. Lee, A High-Frequency Diffused Base Germanium Transistor, Bell Syst. Tech. J., **35**, 1401-1406 (1956)



La juntura difundida es uno de los elementos hacia el proceso planar

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La oxidación del Si

- **Accidentalmente Frosh y Derick descubren que el óxido formado sobre la sup del silicio por su exposicion al vapor de agua, lo protege de daños causados por procesos a alta temperatura.**
- **Inmediatamente se estudian las propiedades del SiO2 como mascara para procesos de difusión, como pasivación de las junturas p-n que intersectan la superficie, y como soporte dieléctrico (aislante) de líneas metálicas.**

C.J. Frosch and L. Derick, Surface Protection and Selective Masking During Diffusion in Silicon, J. Electrochem. Soc., **104**, 547-552 (1957)

The $Si-SiO_2$ diffusion technology had, in point of fact, been transferred from BTL to Shockley Semiconductor, to Fairchild Semiconductor Corporation and, from there led to the creation of Silicon Valley

El accidente de Frosh y Derick hizo lugar a la aparición del SiO2 en la tecnología de semiconductores, permitiendo: el proceso planar, el MOS, y, en definitiva a la revolucion IC

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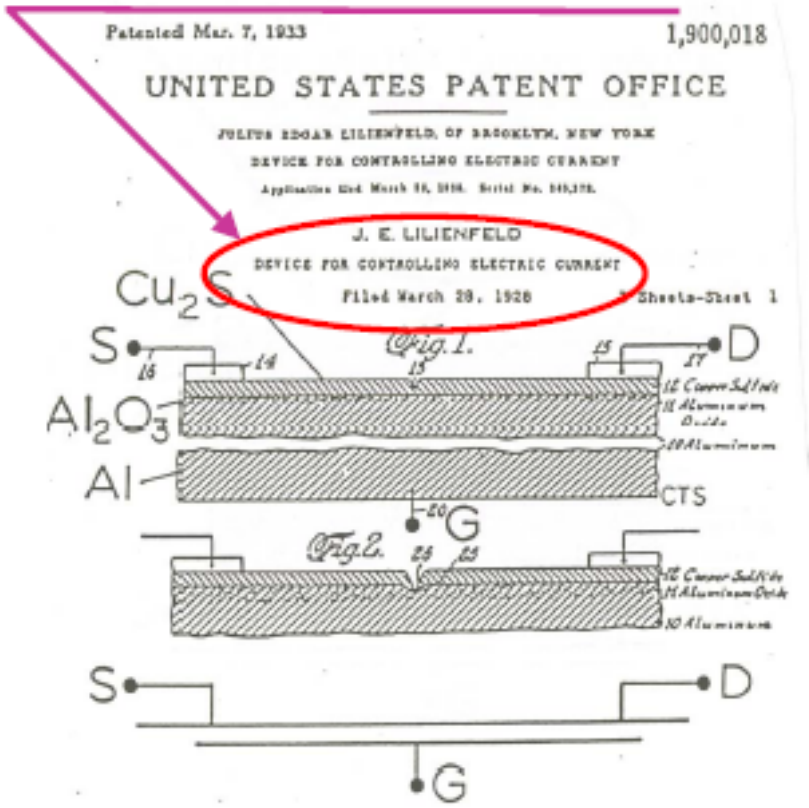
FET

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



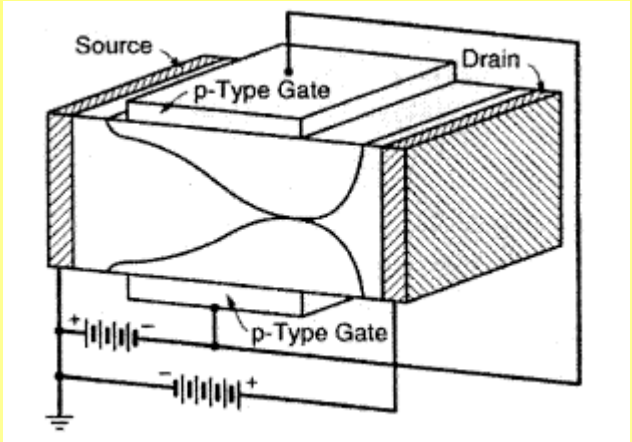
J.E.LILIENFELD

FET

- **Trabajos de Atalla y Kang sobre propiedades pasivantes del óxido y formación de inversión.**
- **MESFET, JFET majority carrier dev**

W.Shockley, A Unipolar "Field Effect" Transistor, Proc. IRE, **40**, 1365-1376 (1952)
W. Shockley, Semiconductor Translating Device, U.S. Patent No. 2,666,814, Filed April 27, 1949, Issued January 19, 1954

D. Kahng and M.M. Atalla, Silicon-Silicon Dioxide Field Induced Surface Devices, paper presented at the Solid State Research Conf., Carnegie Institute of Technology, Pittsburgh, PA, June, 1960
M.M. Attala, Semiconductor Triode, U.S. Patent No. 3,056,888, Filed Aug. 17, 1960, Issued Oct. 2, 1962
D. Kahng, Electric Field Controlled Semiconductor Device, U.S. Patent No. 3,102,230, Filed May 31, 1960, Issued Aug. 27, 1963



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Segunda época (1960-73)

- **IC**
- **Establecimiento tecn. MOS**
- **Memorias**

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Hacia el IC

Desde la invención del transistor los esfuerzos estuvieron puestos en reemplazar el triodo de vacío en sus múltiples aplicaciones. A comienzos de los ’50 comenzó otra idea.

“Gentlemen, you’ve got it all wrong! The advantage of the transistor is that it is inherently a small size and low power device. This means that you can pack a large number of them in a small space without excessive heat generation and achieve low propagation delays. And that’s what we need for logic applications. The significance of the transistor is not that it can replace the tube but that it can do things that the vacuum tube could never do!”

(R. Wallace 1952)

En contra

La tiranía de los números

La probabilidad de que un circuito funcione será $P=Y^N$ donde Y: yield de produccion de cada transistor N: nro componentes circuito… , o sea $P \rightarrow 0$.

Agravado por similar argumento para el gran número de interconexiones realizadas en tecnología de bajo yield.

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Hacia el IC. Antecedentes

Darlington y Oliver (1952), proponen integrar varios junction grown transistors en una pieza de Ge o Si. No incluyen componentes pasivos.

S. Darlington, Semiconductor Signal Translating Device, U.S. Patent No. 2,663,806, Filed May 9, 1952, Issued Dec. 22, 1953

Dummers (1952):

"… layers of insulating, conducting, rectifying and amplifying materials, the electrical functions being connected directly by cutting out areas of the various layers…

G.W.A. Dummer, Electronic Components in Great Britain, Symposium on Progress in Quality Electronic Components, IRE, Washington, D.C., May, 1952, 15-19 (1952)

Ninguno se realizó, y en ninguno se trató el tema de aislamiento entre componentes.

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IC: Las técnicas necesarias

- **Los elementos críticos para la fabricación de transistores (y IC's) están disponibles recién a fines de los '50: oxidación, fotolitografía, difusión, metalización, bonding por termocompresión**

- La tecnología Planar, desarrollada en Fairchild Semiconductor.

exodus of Bob Noyce, Gordon Moore, Jean Hoerni, Jay Last, Julius Blank, Victor Grinich, Eugene Kleiner and Sheldon Roberts 1957 from Shockley Semiconductor Laboratory, established in 1955

J. Andrus and W.L. Bond, Photograving in Transistor Fabrication, *Transistor Technology III*, (edited by F. J. Bondi), 151-162 (1958)

J. Andrus, Fabrication of Semiconductor Devices, U.S. Patent No. 3,122,817, Filed Aug. 15, 1957, Issued Mar. 3, 1964

Metalización

G.E. Moore and R.N. Noyce, Method for Fabricating Transistors, U.S. Patent No. 3,108,359, Issued Oct. 29, 1963

- **JA Hoerni, Planar Silicon Transistors and. Diodes, IRE Electron Dev. Mtg., Wash.,. DC, Oct, 1960**

J. A. Hoerni, Method of Manufacturing Semiconductor Devices, U.S. Patent No. 3,025,589, Filed May 1,1959, Issued March 20, 1962

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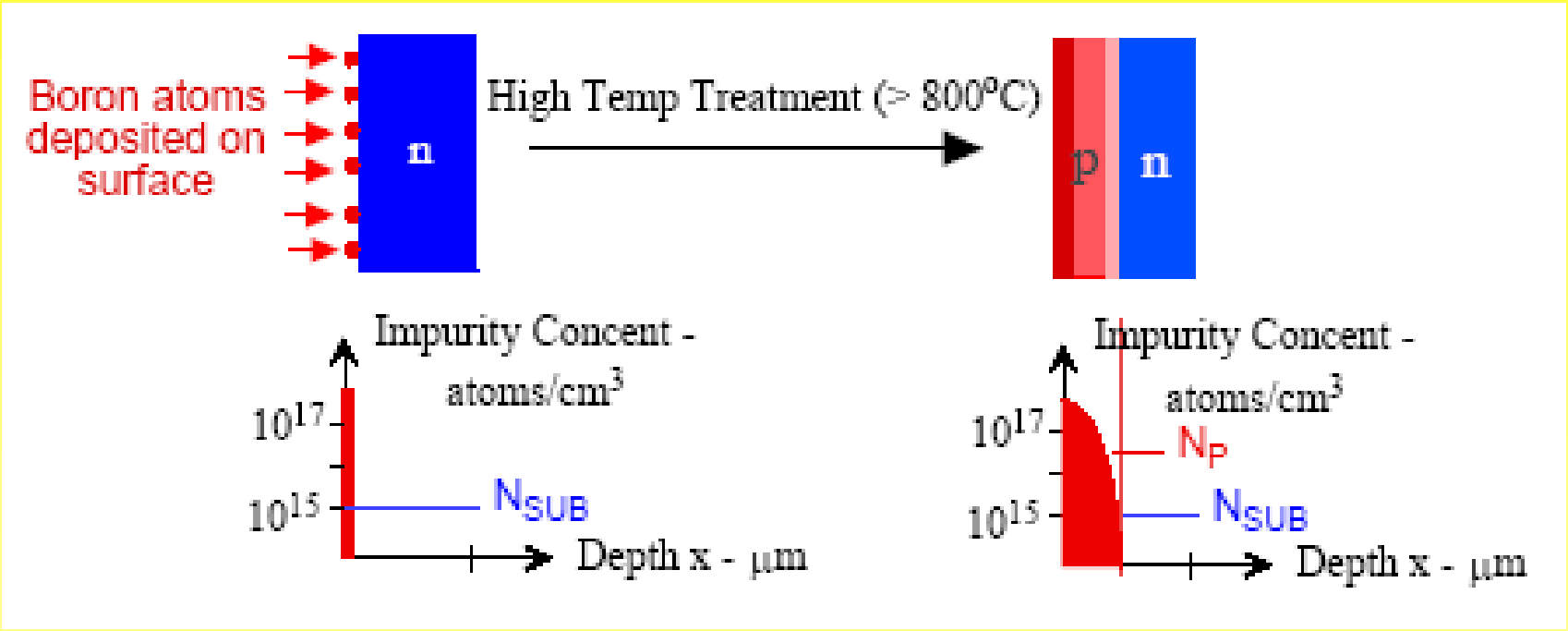
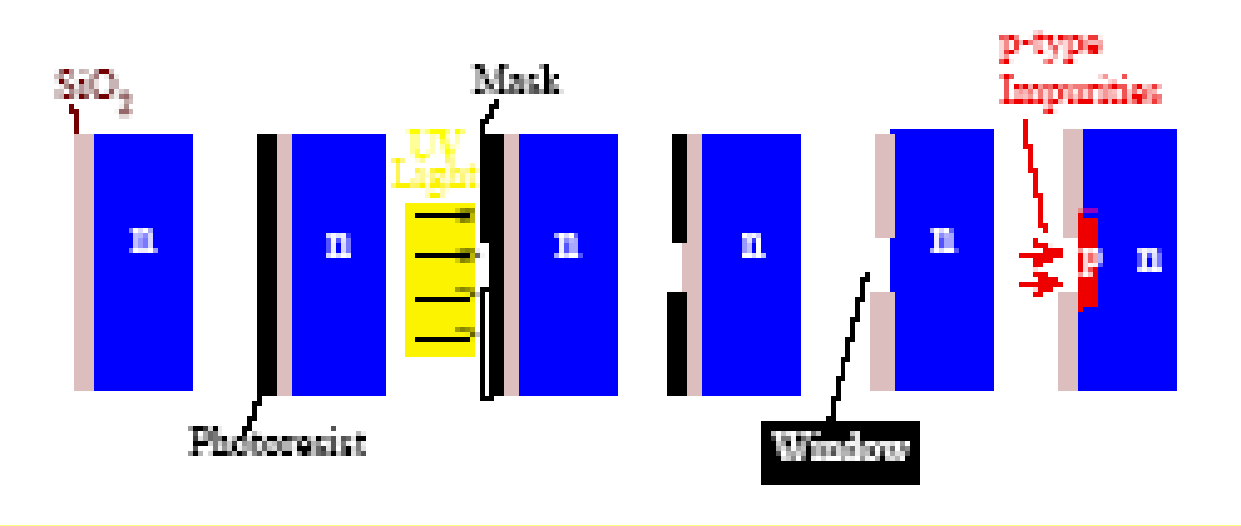
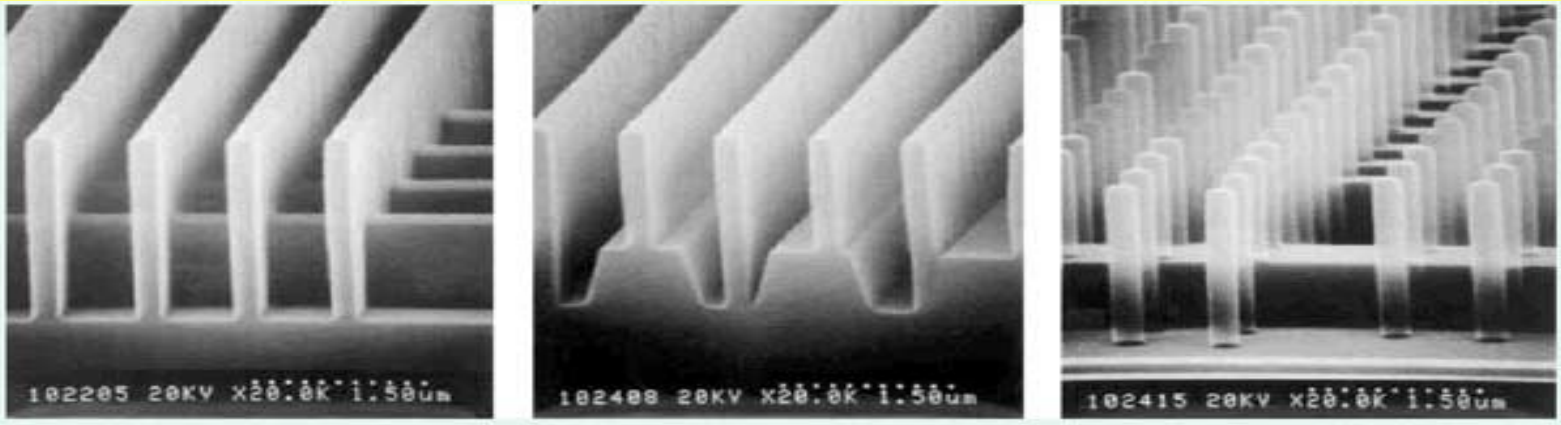
Procesos. Difusión en sólido.



Procesos. Fotolitografía y máscara SiO2



electronic structures



IC: El primero

J.S. Kilby, Miniaturized Electronic Circuits, U.S. Patent No. 3,138,743, Filed February 6, 1959, Issued June 23, 1964

El primer integrado, prueba de concepto de la patente. Un Phase shift oscillator, 10 componentes en Ge, tecnología Mesa.

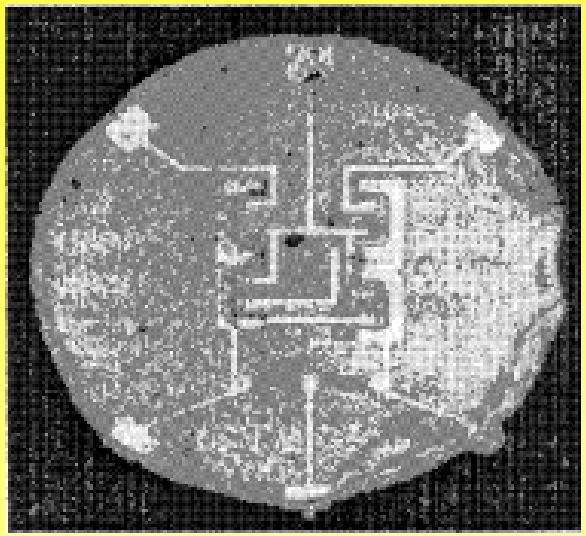
1958 - Jack Kilby – Texas Instr.

"… describing a concept that allowed, using relatively simple steps, the fabrication of all the necessary components of the desired circuit, both active and passive, in a single piece of semiconductor and their interconnection in situ"

Le siguieron un flip-flop y una patente cubriendo Ge y Si. El primer circuito comercial lo anuncio Texas en 1960: un shift register, o contador.

IC: El segundo

R.N. Noyce, Semiconductor Device-And-Lead Structure, U.S. Patent No. 2,981, 877, Filed July 30, 1959, Issued April 25, 1961



El primer integrado planar sobre silicio.
Un flip flop de 4 transistores

1959 – Robert Noyce – Fairchild.

Noyce v. Kilby; Kilby v. Noyce Board of Patents Interference

- **Kilby:**

"…ellectrically conducting material such as gold may then be *laid down* on the insulating material to make the electrical connections"

- **Noyce:**

"…an electrical connection to one of said contacts comprising a conductor *adherent to* said layer"

- **A la pregunta de si *laid down* era equivalente a *adherent to* la corte contestó que sí fallando a favor de Kilby**
- **En 1969 la Court of Customs and Patent Appeals revirtió el fallo confirmando la prioridad de Noyce. El punto, remarcó, es si leyendo la formulación de Kilby inevitablemente se entiende que la pista metálica debe ser adherente**
- **La Corte Suprema rechazó rever el caso**

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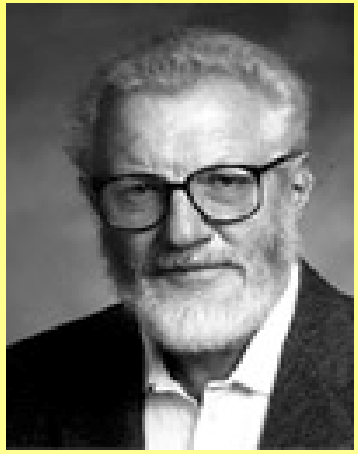
The Nobel Prize in Physics 2000

"for basic work on information and communication technology"

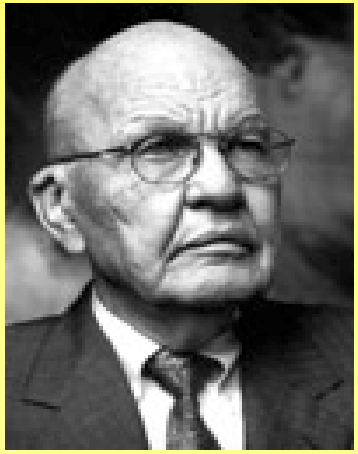
"for developing semiconductor heterostructures used in high-speed- and opto-electronics"

"for his part in the invention of the integrated circuit"

Zhores I Alferov



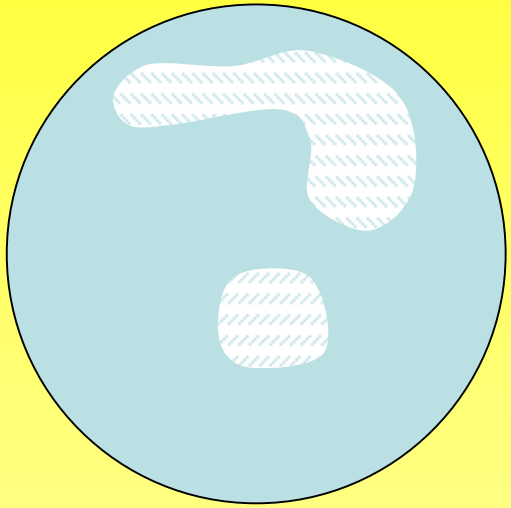
Herbert Kroemer



Jack S Kilby

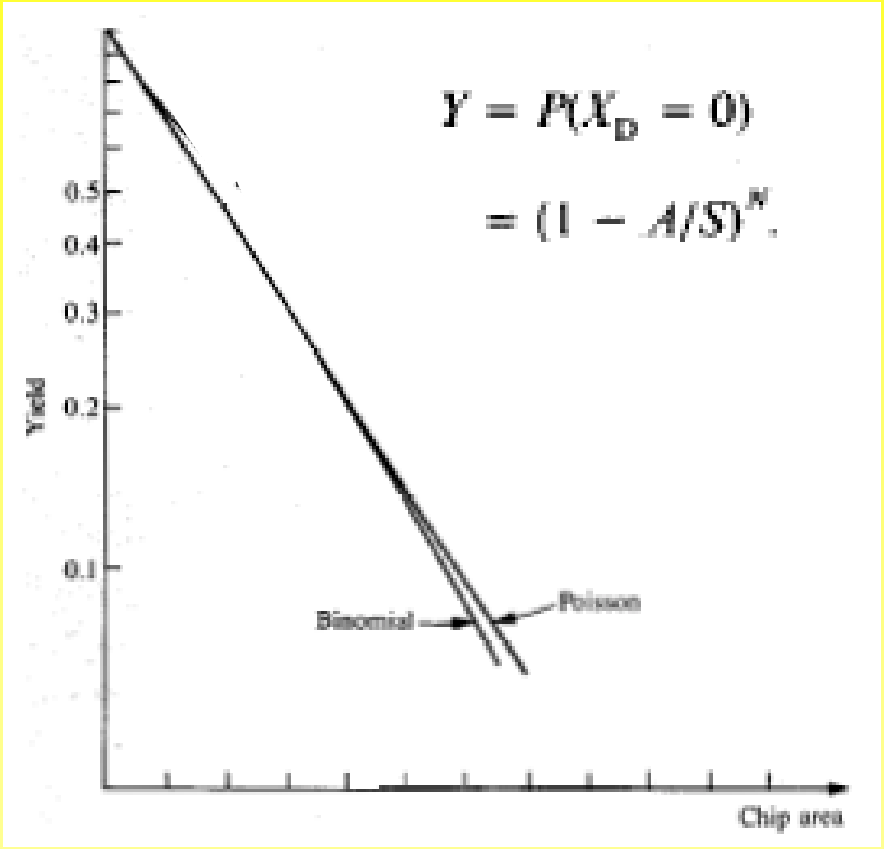
Porqué creció la integración

- **La ley $Y=Y_t^N$ no resultó cierta.**
- **Más bien pareció haber areas donde todo funcionaba y areas donde nada.**
- **Asi, para areas de chip suficientemente pequeñas, el yield sería independiente del area del chip.**



- **Bajo esta premisa explotó el desarrollo de IC's**
- ***Pronto se vio que eso no era cierto***

Yield



B.T. Murphy, “Cost size optima of monolithic integrated circuits”, Proceedings Inst. Electr. Eng. Vol 52, 1964, p.1537

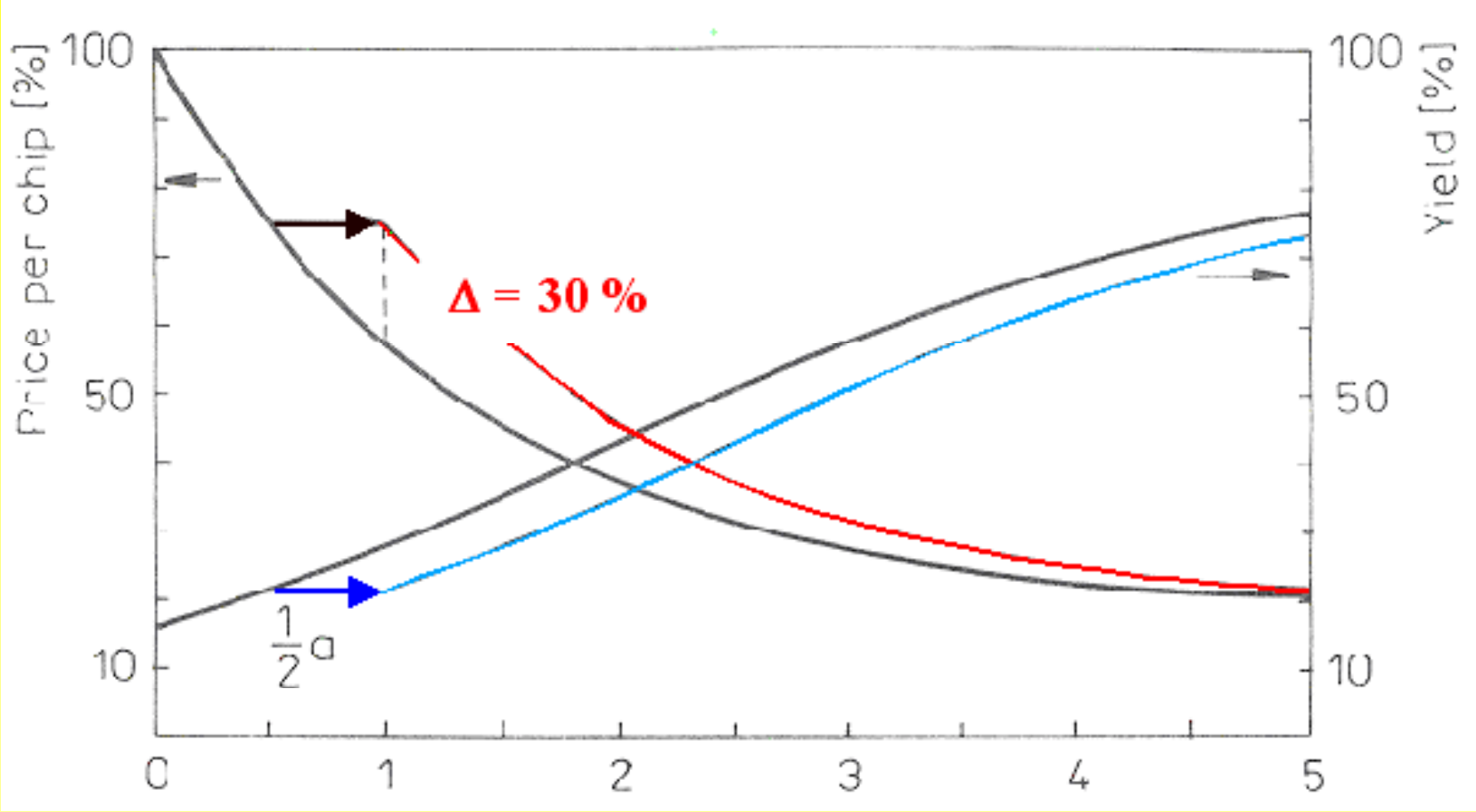
$$\text{Cost per chip} = \frac{\text{Cost per wafer}}{\text{Gross chips per wafer}} \cdot 1/Y$$

$$\text{Cost per chip} = \text{Cost per wafer} \quad \frac{A/S}{(1-A/S)^N}$$

S area wafer, A area chip, N nro defectos criticos por wafer, XD defectos por chip

La teoría del beneficio económico de la miniaturización estaba fundada

Yield and Learning curve



También la teoría del valor económico de aprender rápido

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Avances tecnología 2°

- **Estructuras**

- **Epitaxy en relacion a aislación de IC's bipolares**
- **Epitaxy para reducir resistencia de colector**
- **Estructuras autoalineadas**

- **La puerta de polysilicio dopado**

A. Mark, Growth of Single Crystal Overgrowth on Silicon Substrate, J. Electrochem. Soc., **107**, 568-569 (1960)

H.C. Theuerer, J.J. Kleimack, H.H. Loar and H. Christensen, Epitaxial Diffused Transistors, Proc. IRE, **48**, 1642-1643 (1960)

R.W. Bower and H.C. Dill, Insulated Gate Field Effect Transistors Fabricated Using the Gate as Source-Drain Mask, *IEDM*, 21-22 (1966)

R.E. Kerwin, D.L. Klein and J.C. Sarace, Method for Making MIS Structures, U.S. Patent No. 3,475,234, Filed Mar. 27, 1967, Issued Oct. 28, 1969

Avances tecnología 2°

- **Procesos**
- **Trabajos de Deal y Grove sobre cinética de oxidación, cargas en el óxido y estados en la interfaz Si-SiO2.**
- **Condiciones de fabricación de dispositivos comerciales:**
  - **Eliminación cargas móviles (K y Na)**
  - **Reducción cargas fijas (indispensables en n-channel)**
  - **Reducción de estados de interfaz**
- **Introducción de las etapas de post-oxidation annealing, y post-metalization annealing, según modelo Balk de saturación de dangling bonds con H.**

B.E. Deal and A.S. Grove, General Relationship For The Thermal Oxidation of Silicon, J. Appl. Phys., **36**, 3770-3778 (1965)

B.E. Deal, M. Sklar, A.S. Grove and E.H. Snow, Characteristics of The Surface-State Charge (Q_{ss}) of Thermally Oxidized Silicon, J. Electrochem. Soc, **114**, 266-274 (1967)

P. Balk, Effects of Hydrogen Annealing on Silicon Surfaces, Elecrochemical Society Extended Abstracts of Electronics Divison, **14**, No.1, Abst. 109, 237-240 (May, 1965), also abstracted in J. Electrochem. Soc., **112**, abst. 109, p.69C, (1965)

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Avances tecnología 2°

- **Procesos**
- **Deposición de polysilicio por CVD**

L.L. Vadasz, A.S. Grove, T.A. Rowe and G.E. Moore, Silicon Gate Technology, *IEEE Spectrum*, **6**, No. 10, 28-35 (1969)

- **El dopado por implantacion.**

R.W. Bower, H.G. Dill, K.G. Aubuchon and S.A. Thompson, MOS Field-Effect Transistors Formed by Gate Masked Ion Implantation, IEEE Trans Electron Dev., **ED-15**, 757-761 (1968)

Avances tecnología 2°

- **Procesos**
- **Desarrollo de capas pasivantes aislantes del entorno:**
  - **Si3N4 plasma o CVD.**
  - **Phospho-glass**

J.V. Dalton and J. Dorbeck, Structure and Sodium Migration in Silicon Nitride Films, **J.** Electrochem. Soc., **115**, 865-868 (1968)
D.R. Kerr, J.S. Logan, P.J. Burkhardt and W.A. Pliskin, Stabilization of SiO_2 Passivation Layers With P_2O_5, IBM J. Res. Develop., **8**, 376-384 (1964)

- **Técnicas de gettering**

R.J. Kriegler, Y.C. Chang and D.R. Colton, The Effect of HCl and Cl_2 on The Thermal Oxidation of Silicon, J. Electrochem. Soc., **119**, 388-392 (1971)

- **Polysilicon Gate**
- **LOCOS**

J.A. Appels, E. Kooi, M.M. Paffen, J.J.H. Schatorje and W.H.C.G. Verkuylen, Local Oxidation of Silicon and its Application in Semiconductor-Device Technology, Philips Repts., **25**, 118-132 (1970)

Avances tecnología 2°

- **Dispositivos**
- **Body effect technique (Heiman)**
- **Implantación para ajuste de VT**
- **CMOS (Wanlass)**

F.P. Heiman, Integrated Insulation-Gate Field-Effect Transistor Circuit on a Single Substrate Employing Substrate-Electrode Bias, U.S. Patent No. 3,233,123, Filed Feb. 14, 1963, Issued Feb. 1, 1966

F.M. Wanlass, Low Stand-By Power Complementary Field Effect Circuitry, U.S. Patent No. 3, 356,858, Filed June 18,1963, Issued Dec. 5, 1967

Caracterización

- **Caracterización del sistema Si-SiO2 por Capacidad-Voltaje**
- **Y vía Conductancia-frecuencia (Nicollian-Goetzberger)**

L.M. Terman, An Investigation of Surface States at a Silicon/Silicon Diode Interface Metal-Oxide-Silicon Diodes, Solid-State Electron., **5**, 285-299 (1962)

A.S. Grove, E.H. Snow, B.E. Deal and C.T. Sah, Simple Physical Model For The Space-Charge Capacitance of Metal-Oxide-Semiconductor Structures, J. Appl. Phys., **35**, 2458-2460 (1964)

K.H. Zaininger and F.P. Heiman, The C-V Technique as an Analytical Tool (Part 1 and 2), Solid State Tech., No. 5, 49-56 (Part 1), May and No. 6, 46-55 (Part 2), June, (1970)

E.H. Nicollian and A.Goetzberger, The Si-SiO_2 Interface-Electrical Properties as Determined by the MIS Conductance Technique, Bell System Tech. J., **46**, 1055-1133 (1967)

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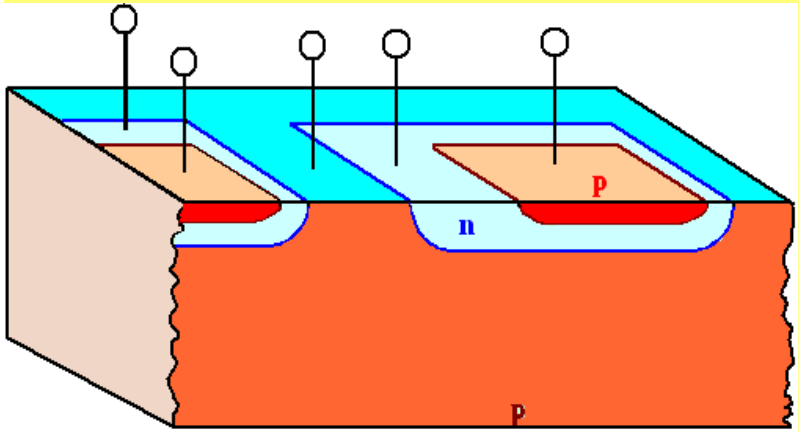
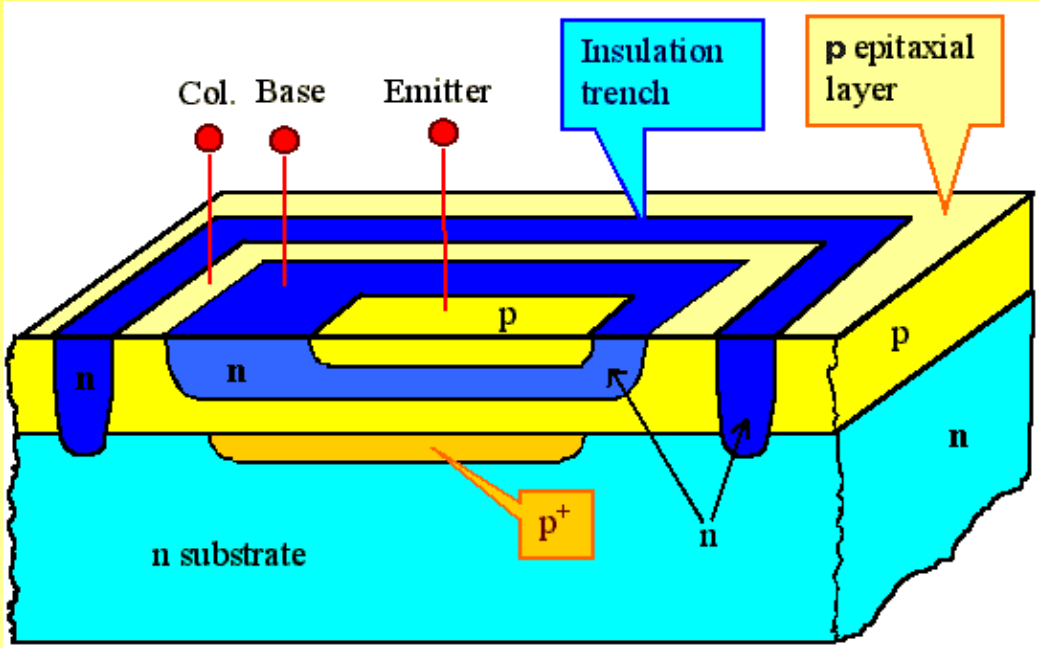
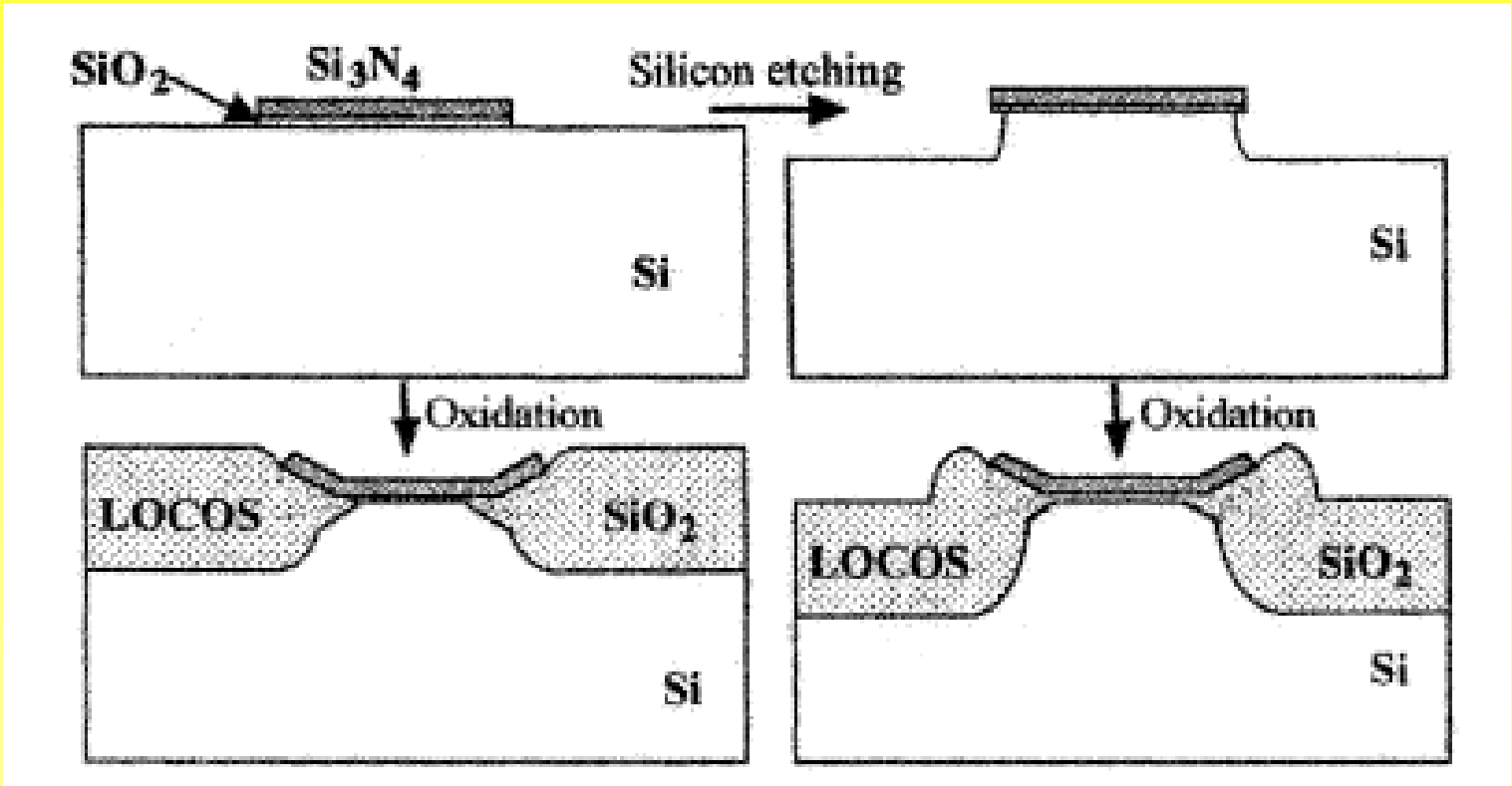




Avances Tecnología 2°
LOCOS (Local Oxidation of Si)



Avances Tecnología 2°

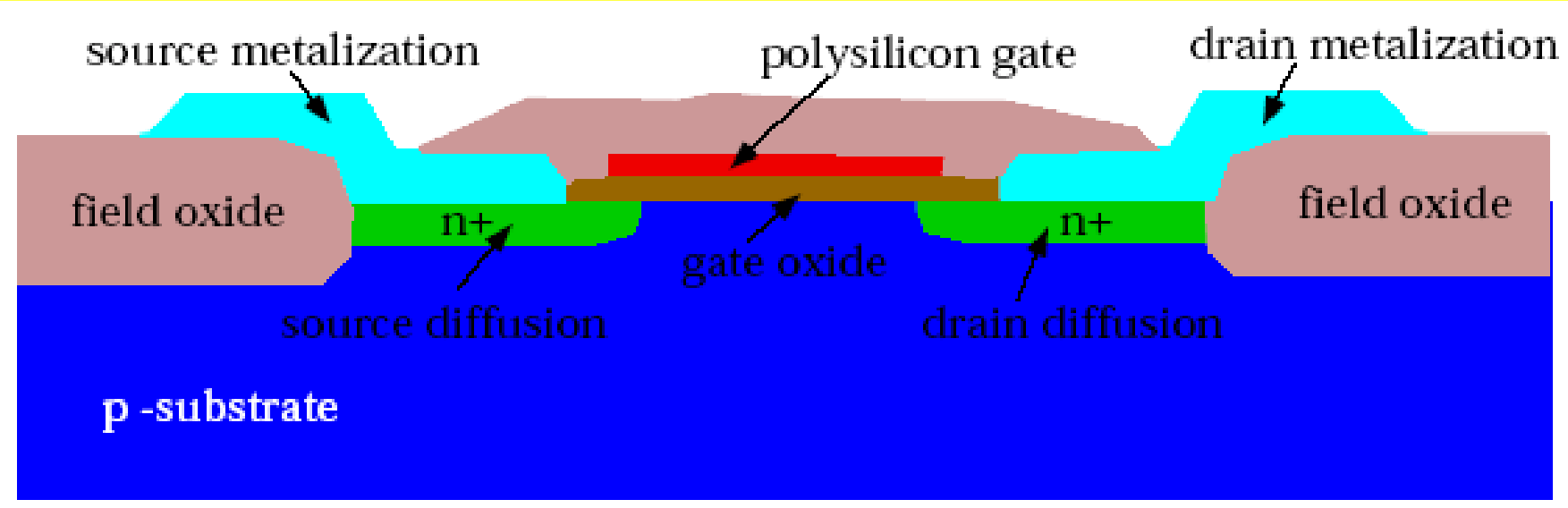
- **Dispositivos**

- **Body effect technique.**
- **Implantación para ajuste de VT**

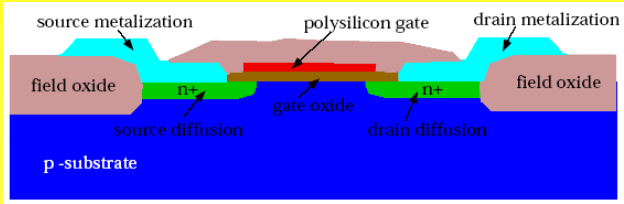
F.P. Heiman, Integrated Insulation-Gate Field-Effect Transistor Circuit on a Single Substrate Employing Substrate-Electrode Bias, U.S. Patent No. 3,233,123, Filed Feb. 14, 1963, Issued Feb. 1, 1966

$$V_T = \Phi_{ms} + 2\Phi_b - \frac{Qox}{Cox} + \frac{(2\varepsilon_s qNa)^{1/2}}{Cox}.(2\Phi_b + Vbb)^{1/2}$$

N-MOS simple


source metalization
polysilicon gate
drain metalization
field oxide
n+
gate oxide
n+
field oxide
source diffusion
drain diffusion
p -substrate

Proceso N-MOS simple (1/2)



Patterning SiO_2 Layer

SiO_2

Gate Oxidation

Thin Oxide

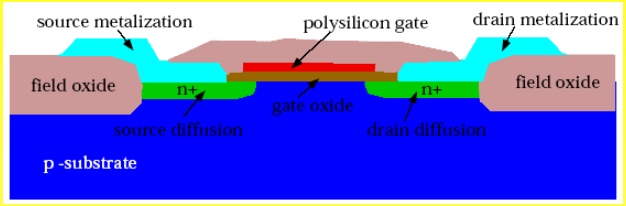
100A - 300A

Patterning Polysilicon

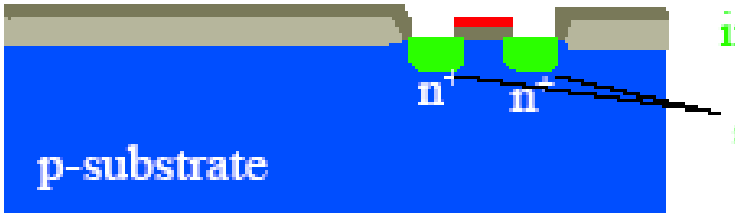
Polysilicon

0.5 µm - 2 µm

Proceso N-MOS simple (2/2)



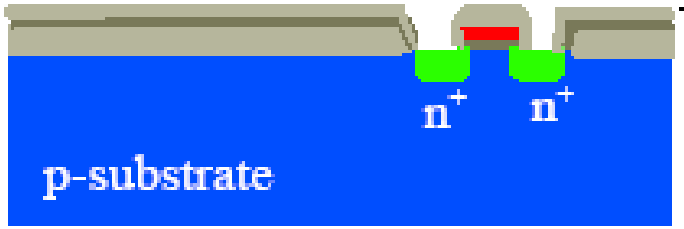
Source, Drain Inplants or Diffusions (self aligned)



implant of impurities

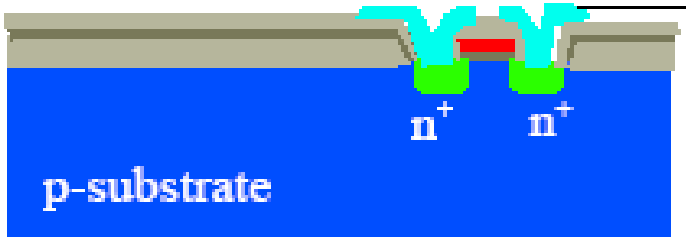
≈ 1 μm deep

Contact Cuts



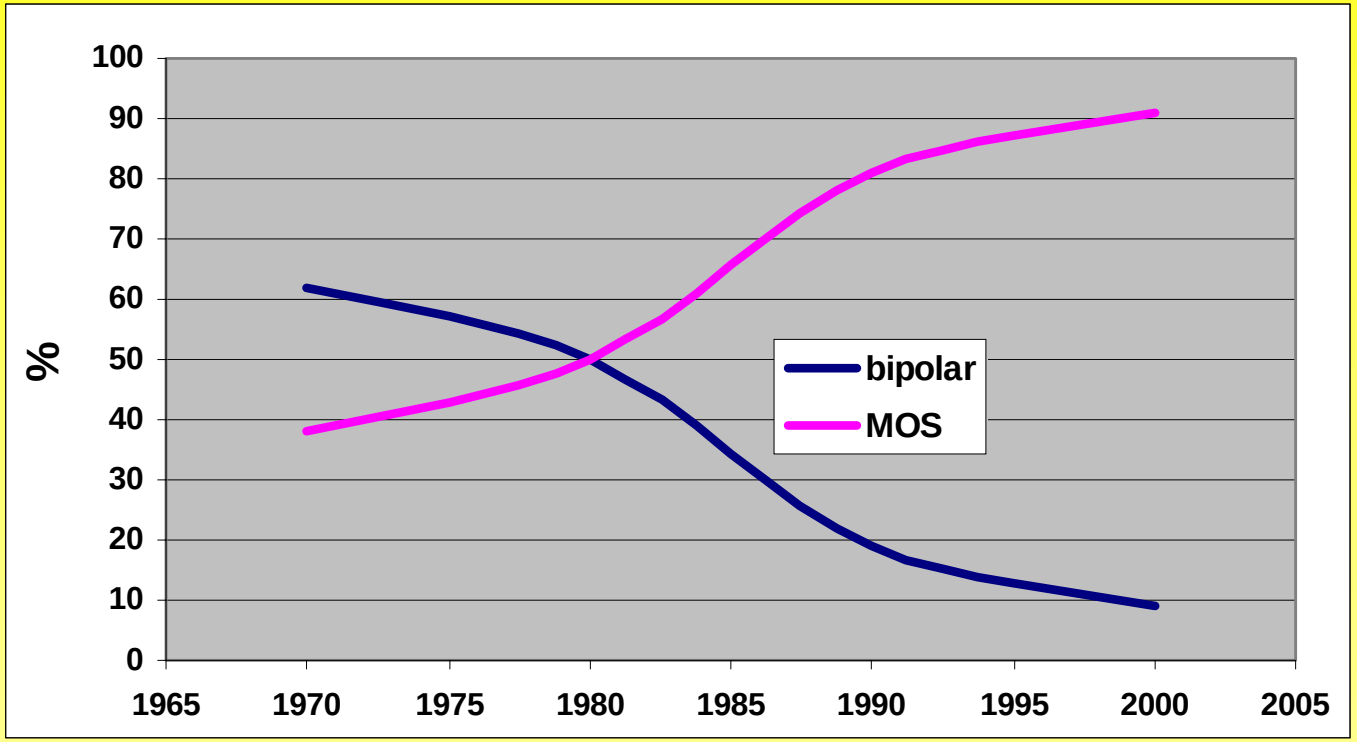
SiO_2 by deposition

Patterning Al Layer



Aluminum contacts

Market share by technology



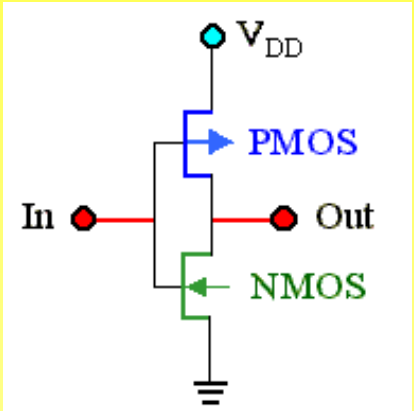
100% = sales for 200.000 millon u$,

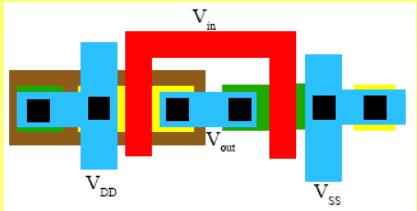
or 20% of total sales in electronic equipment.

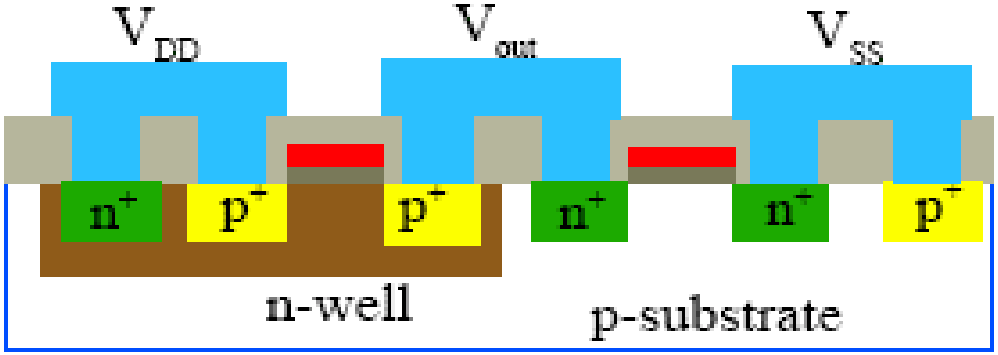
Avances Tecnología 2°

- **Dispositivos**
- **CMOS (Wanlass)**
  - **El circuito de demostración (inversora de 2 trans) mostró consumir pocos nW comparados con los mW de los equivalentes bipolares o pMOS.**
  - **Curiosamente tuvo que usar body effect para el n-channel. Indice del estado de la tecnologia.**

F.M. Wanlass, Low Stand-By Power Complementary Field Effect Circuitry, U.S. Patent No. 3, 356,858, Filed June 18,1963, Issued Dec. 5, 1967







Memorias

- **1964 64 bit SRAM – 6 trans/cell – enhancement p-ch MOS (Fairchild)**

- **1964 Similar de RCA pero en n-channel usando body effect (falta control sobre Qox)**

- **…**

- **1970 Texas 256 bit DRAM**

- **1970 Intel 1K 3 trans/cell p-ch DRAM**

Con esta última comienzan las memorias Si a reemplazar al ferrite en las computadoras. La innovación la hizo Honeywell, Inc.

Tercera época (1973-)

•IBM resuelve reemplazar ferrite (1 microsec access time) por memorias NMOS (1 nsec a.t.) para su mainframe IBM-370/158.

Intel y MOSTEK son los primeros proveedores.

1974 se suma Texas usando la estructura 1 trans/cell de Dennard

Ahí comienza verdaderamente el mercado a tirar de la tecnología.

Tercera época (1973-)

- **1976 16Kb DRAM con los siguientes cambios**
  - **Reglas de diseño de 7-8 micras a 5 micras**
  - **Remoción de la difusión de souce (merged transistor DRAM cell)**
  - **Doble silicon gate para gate y charge storage capacitor.**
  - **Diámetro de oblea de 2 a 3 pulgadas.**

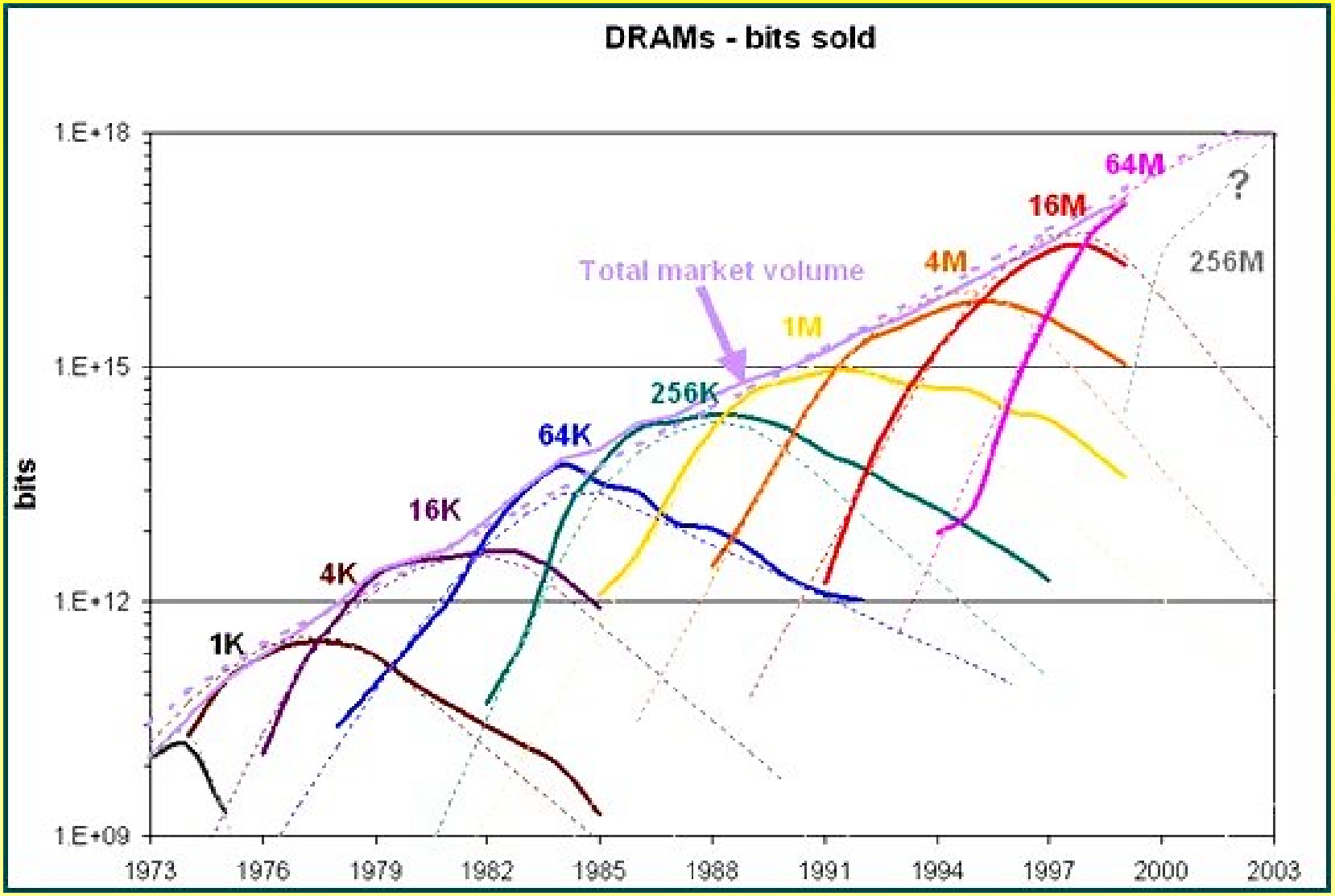
- **1979 64K DRAM**
  - **Reglas de diseño a 2-3 micras**
  - **Diámetro de oblea a 4 pulgadas**
  - **Cambios en estructuras y procesos**

….. 256 K (1982) …. 1M (1985)…

- **1988 4Mb DRAM**
  - **Reglas de diseño submicrón 0.8 micras**

LabFisDispμ

. . .



LabFisDispμ

Tecnologías 3°

- **Estructuras**

  -Capacitor de placas y no de inversión para almacenar 10^6 electrones a 5 V alimentación (C= 32 fF) p/reducción soft errors.

  -Dual dielectric (SiO2-Si3N4)para el Charge Storage Cap.

  3D trench Charge Storage Cap.

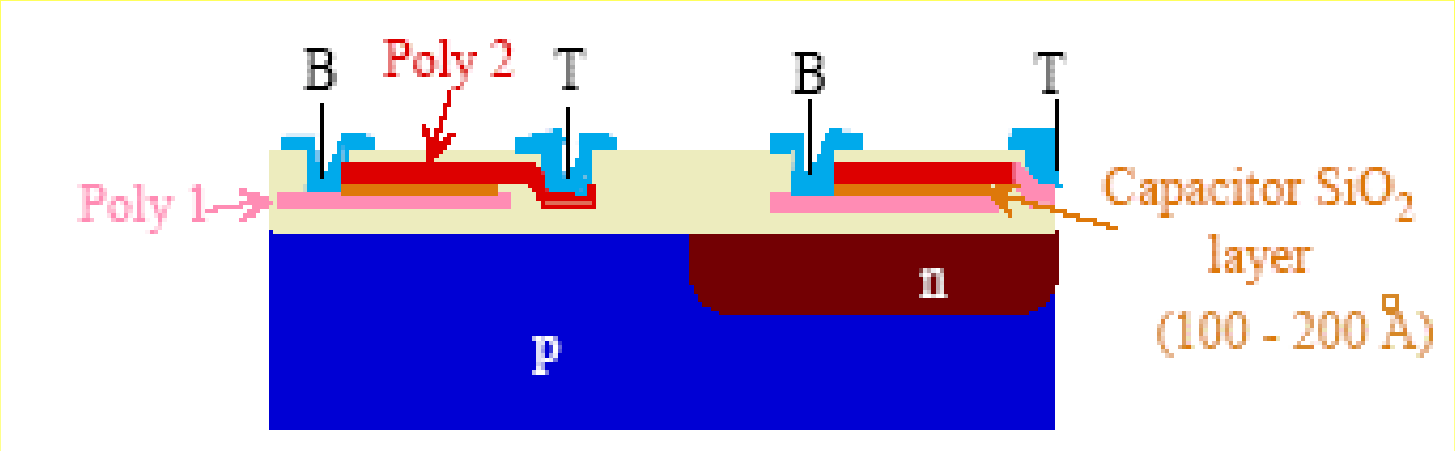
- **Procesos**

  Plasma etch para mejor definición vertical (economía de área)

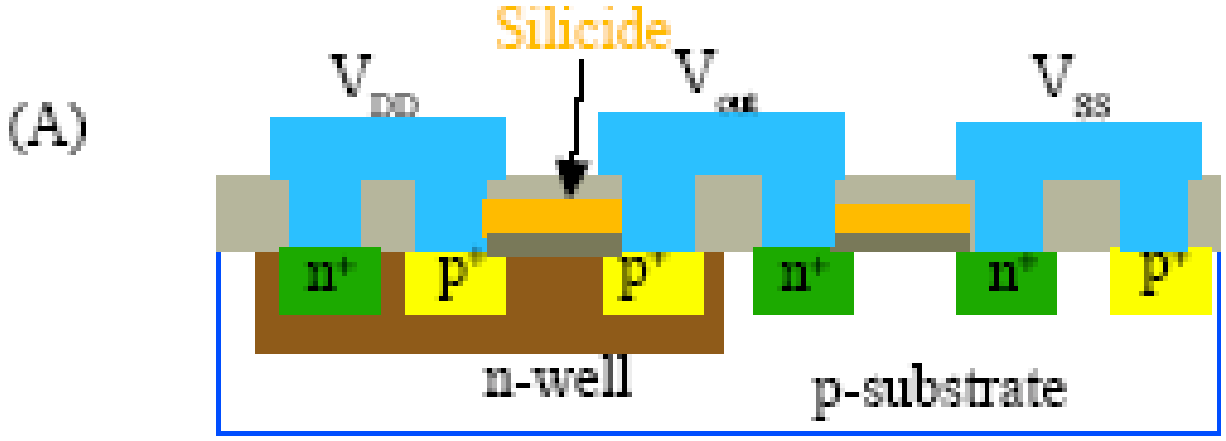
  Optical wafer stepper para bajar de las 2 micras ancho de linea

  Metalización con Silicides

Tecnologías 3°
Double poly gate



Tecnologías 3°
Refractory/poly interconect (1/3)

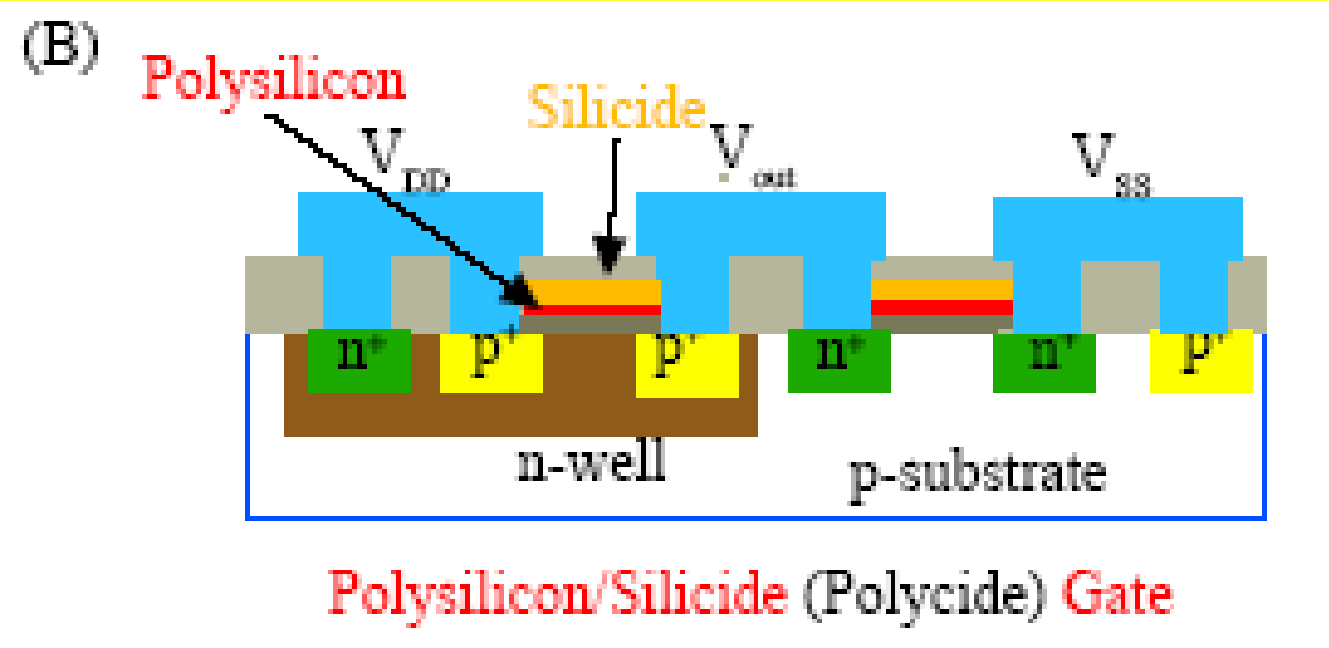


Silicide Gate (e.g. silicon and tantalum)

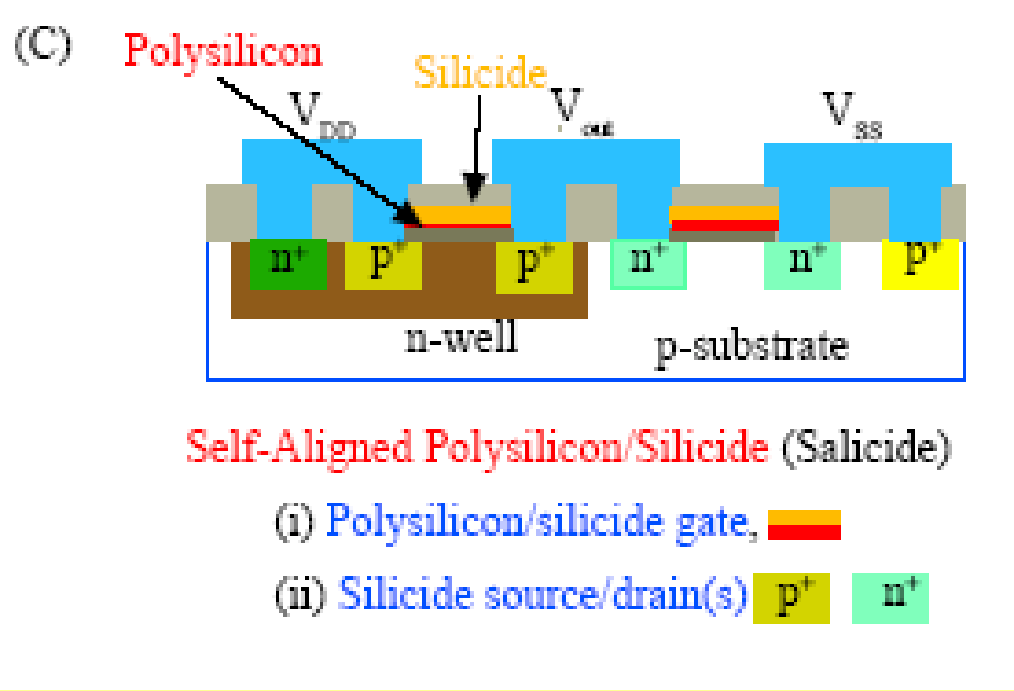
Doped Polysilicon: R_{sheet} = 20 to 40 Ω/Square

Silicide: R_{sheet} = 1 to 5 Ω/Square

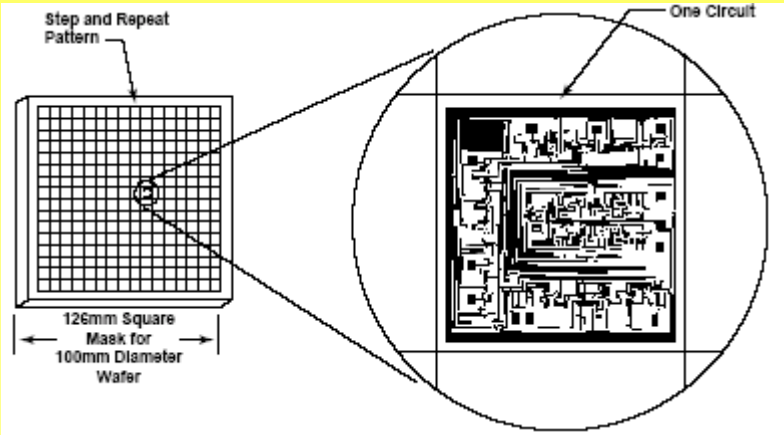
Tecnologías 3°
Refractory/poly interconect (2/3)



Tecnologías 3°
Refractory/poly interconect (3/3)

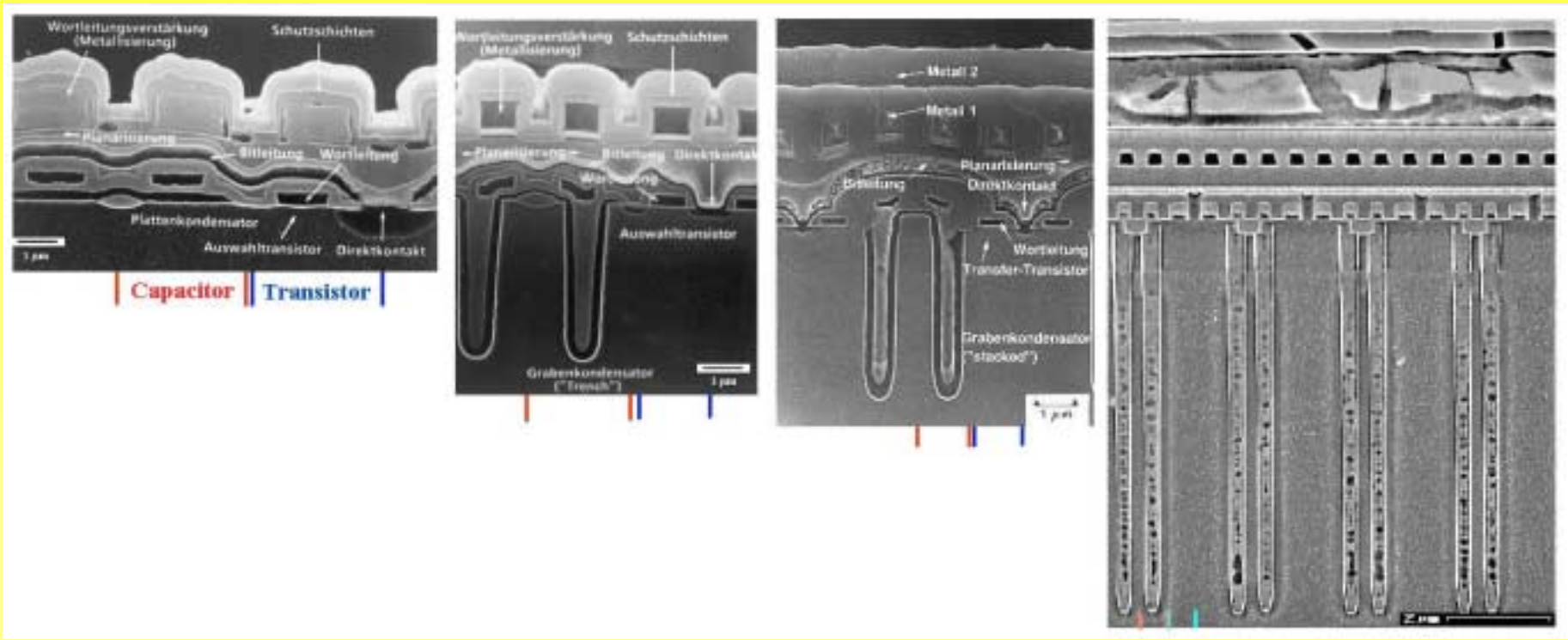


Tecnologías 3°
Step and Repeat

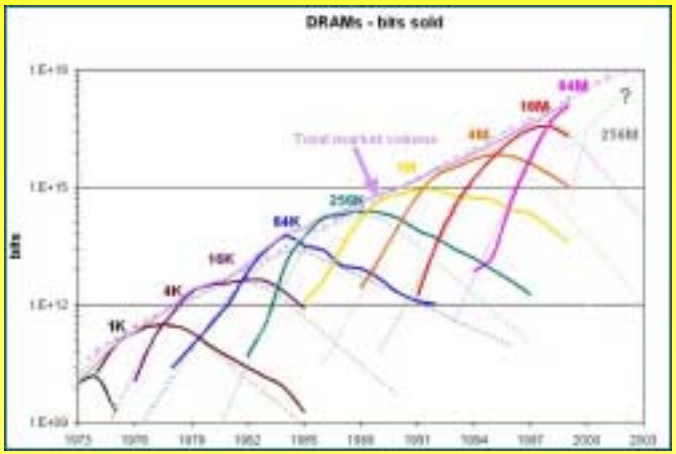


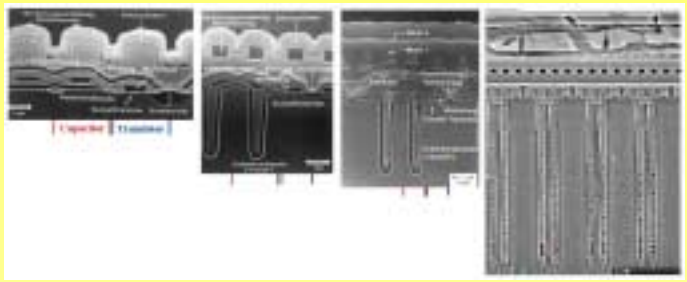
Tecnologías 3°

1M **4M** **16M** **64M DRAM's**



……hasta dónde continuará?





Las dificultades tecnológicas y límites físicos en la reducción de dimensiones

(próximamente)