

Chapter Outline

16.1	Introduction	16.11	Voltage-to-Frequency and Frequency-to-Voltage Converters
16.2	Comparators	16.12	Sample-and-Hold Circuits
16.3	Zero-Crossing Detectors	16.13	Digital-to-Analog Converters
16.4	Schmitt Triggers	16.14	Analog-to-Digital Converters
16.5	Square-Wave Generators	16.15	Circuit Design Using Analog ICs
16.6	Triangular-Wave Generators		
16.7	Sawtooth-Wave Generators		
16.8	Voltage-Controlled Oscillators		
16.9	The 555 Timer		
16.10	Phase-Lock Loops		

SUMMARY ► REFERENCES
REVIEW QUESTIONS ► PROBLEMS

16.1 ► Introduction

Electronic circuits are commonly employed in generating waveforms of various shapes for control and interfacing purposes. This chapter will examine the basic principles of operation of circuits used to generate waveforms and the applications of some commonly used ICs.

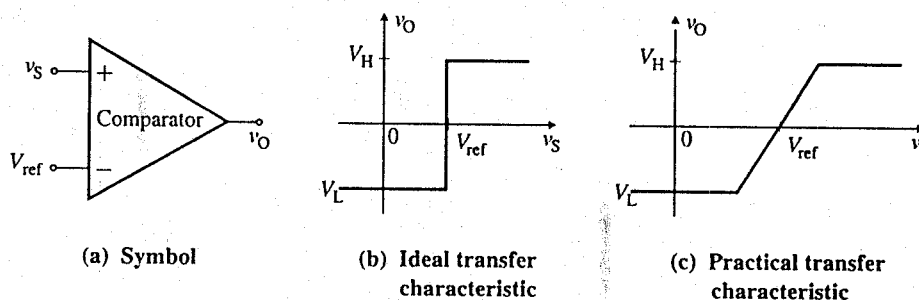
The learning objectives of this chapter are as follows:

- To understand the differences between comparators and op-amps
- To study the applications of comparators and op-amps as zero-crossing detectors, Schmitt triggers, and square-wave, triangular-wave, and sawtooth-wave generators
- To examine the internal structure and the principles of operation of commonly used analog integrated circuits
- To become familiar with the applications of some ICs and to design circuits for waveform generation, conversion, detection, and signal processing

16.2 ► Comparators

A comparator compares a signal voltage v_S on one input terminal with a known voltage, called the *reference voltage* V_{ref} , on the other input terminal. The symbol of a comparator, which is similar to that of an op-amp, is shown in Fig. 16.1(a). A comparator gives a digital output voltage v_O . Thus, it can be considered a simple one-bit analog-to-digital (A/D)

FIGURE 16.1
Symbol and transfer
characteristics of a
comparator



converter, which produces a digital 1 output ($v_O = V_H$) if the input voltage v_S is above the reference level V_{ref} and a digital 0 output ($v_O = V_L$) if the input voltage v_S falls below the reference level V_{ref} . The output levels V_L and V_H may be of opposite polarity (that is, V_H positive and V_L negative, or vice versa), or both V_L and V_H may be either positive or negative. The transfer characteristic of an ideal comparator is shown in Fig. 16.1(b). The output may be symmetrical or asymmetrical.

A practical comparator has a finite voltage gain in the range from 3000 to 200 000 and takes a finite amount of time (in the range from 10 ns to 1 μ s) to make a transition from one level to another (e.g., V_L to V_H). The transfer characteristic of a practical comparator is shown in Fig. 16.1(c). The input voltage swing required to produce the output voltage transition is in the range of about 0.1 mV to 4 mV. The output of a comparator must switch rapidly between the levels. The bandwidth must be wide, because the wider the bandwidth, the faster the switching speed. Some typical parameters (listed here for the LM111 comparator) are as follows:

- Operates from a single 5-V power supply
- Input current: 150 nA (maximum)
- Offset current: 20 nA (maximum)
- Differential input voltage: ± 30 V
- Voltage gain: 200 V/mV (typical)

Comparators versus Op-Amps

A comparator is designed to operate under open-loop conditions, usually as a switching device, whereas an op-amp is generally operated under closed-loop conditions as a linear amplifier. Otherwise, comparators are very similar to op-amps. Like an op-amp, a comparator has an offset voltage (typically 4 mV), a biasing current (typically 150 nA), and an offset current (typically 20 nA). The characteristics of comparators and op-amps are listed in Table 16.1.

Output-Side Connection

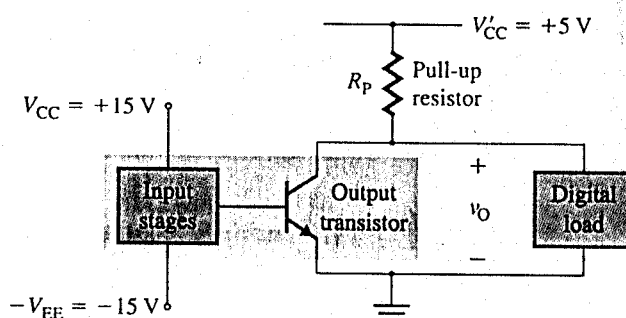
Comparators are often used as an interface between digital and analog signals. The power supply at the analog side (V_{CC} and V_{EE} , typically ± 15 V) is different from that at the digital side (V'_{CC} , typically 0 to 5 V). Comparators generally have an open-collector output

TABLE 16.1
Comparators versus op-amps

Op-Amps	Comparators
Operation is in closed-loop mode. In order to avoid an unstable oscillatory response, a sacrifice is usually made in bandwidth, rise time, and slew rate.	Operation is in open-loop mode. No sacrifice is needed in frequency characteristics, and a very fast response time can be obtained.
The output voltage is designed to be zero when the differential input voltage is zero.	The output voltage operates between two fixed output levels: V_L (low) and V_H (high).
The output voltage saturates about 1 or 2 V away from the positive and negative supply voltages (V_{CC} and V_{EE}).	The low- and high-output levels can be changed for ease in interfacing with digital logic circuits.

stage, which allows separate power supplies for the analog and digital parts. A block diagram of the LM111 comparator is shown in Fig. 16.2. The output terminals are the collector and emitter of an *npn* transistor. If the input voltage to the transistor is low, the transistor is off and the output logic level is 1—that is, the output is high (5 V) and the current flows through the pull-up resistor R_P to the digital load. On the other hand, if the input voltage to the transistor is high, the transistor is driven into saturation and the output logic level is 0—that is, the output is low at the saturation voltage of the transistor (typically 0.2 V) and no current flows through the pull-up resistor R_P to the digital load.

FIGURE 16.2
Output connection of
LM111 comparator



Threshold Comparators

The voltage at which a comparator changes from one level to another is called the *crossover* (or *threshold*) voltage. Its value can be adjusted by adding resistors, as shown in the noninverting comparator in Fig. 16.3(a). From the superposition theorem, the voltage V_+ at the noninverting terminal is given by

$$V_+ = \frac{R_1}{R_1 + R_F} V_{\text{ref}} + \frac{R_F}{R_1 + R_F} v_S \quad (16.1)$$

Ideally, the crossover will occur when $V_+ = 0$. That is,

$$R_1 V_{\text{ref}} + R_F v_S = 0$$

which gives the low threshold voltage of the comparator $V_{L_t} = v_S$ (for changing from low to high) as

$$V_{L_t} = -\frac{R_1}{R_F} V_{\text{ref}} \quad (16.2)$$

Thus, the output voltage becomes high (V_H) at the positive saturation voltage ($+V_{\text{sat}}$) when $V_+ > 0$ (that is, $v_S > V_{L_t}$). The transfer characteristic is shown in Fig. 16.3(b).

If the input signal v_S is connected to the inverting terminal, as shown in Fig. 16.4(a), the output will change from high (V_H) to low (V_L). This situation is shown in Fig. 16.4(b).

FIGURE 16.3
Noninverting threshold
comparator

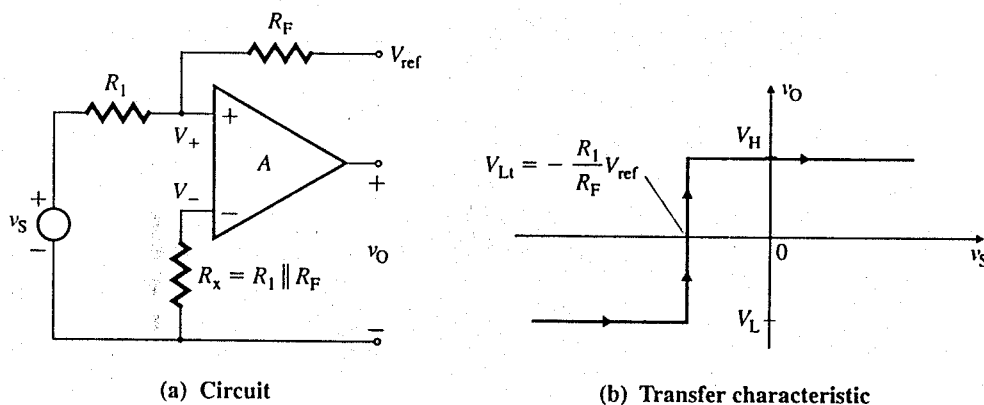
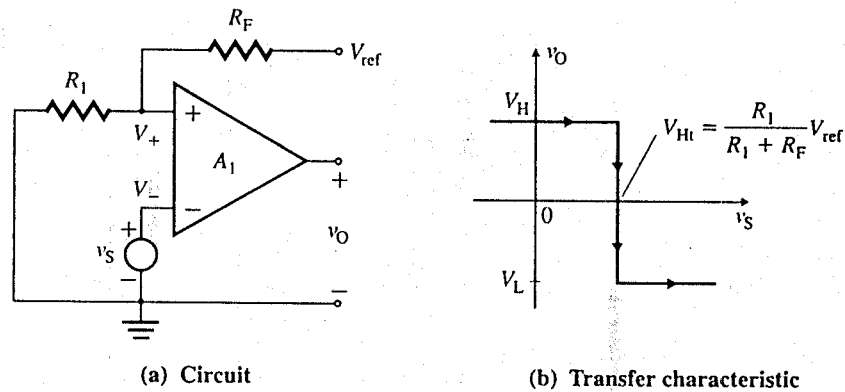


FIGURE 16.4

Inverting configuration for noninverting threshold comparator

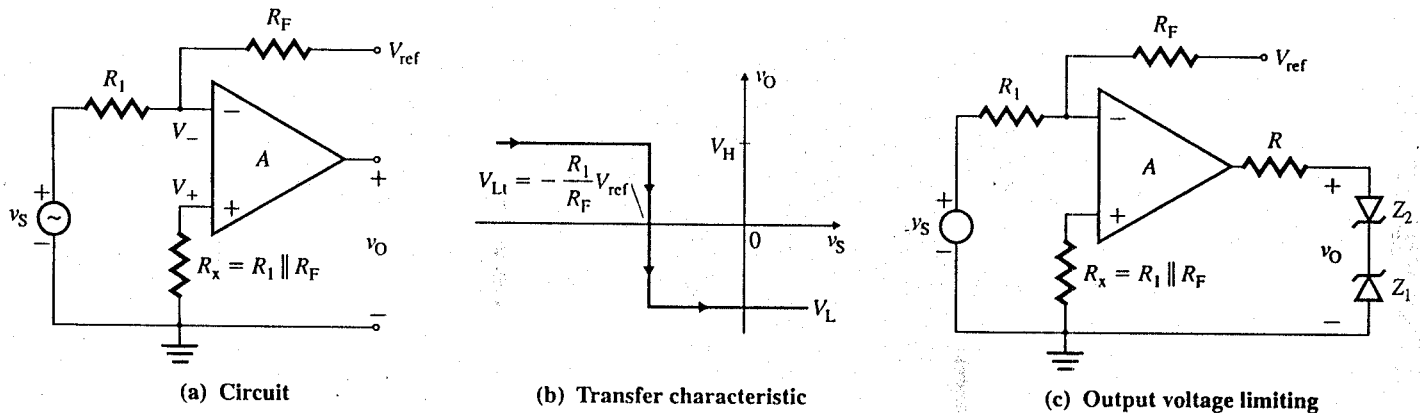


The high threshold voltage of the comparator $V_{Ht} = v_S$ (for changing from high to low) is given by

$$V_{Ht} = \frac{R_1}{R_1 + R_F} V_{ref} \quad (16.3)$$

Thus, the output voltage becomes low (V_L) at the negative saturation voltage ($-V_{sat}$) when $v_S > V_+$ (that is, $v_S > V_{Ht}$). The transfer characteristic is shown in Fig. 16.4(b).

If both the input signal v_S and the reference signal V_{ref} are connected to the inverting terminal, as shown in Fig. 16.5(a), the output will be the inversion of the output in Fig. 16.3(b). That is, the output will change from high (V_H) to low (V_L) when the input is $v_S = V_{Lt}$. This situation is shown in Fig. 16.5(b).

FIGURE 16.5 Inverting threshold comparator

In both inverting and noninverting configurations, the output voltage is limited to the saturation voltage of the comparator. The output voltage can, however, be set to specified limits by external limiters such as zener diodes connected across the output terminals of Figs. 16.3(a), 16.4(a), and 16.5(a). This approach is illustrated in Fig. 16.5(c), in which resistance R is connected to limit the current through the zener diodes.

KEY POINTS OF SECTION 16.2

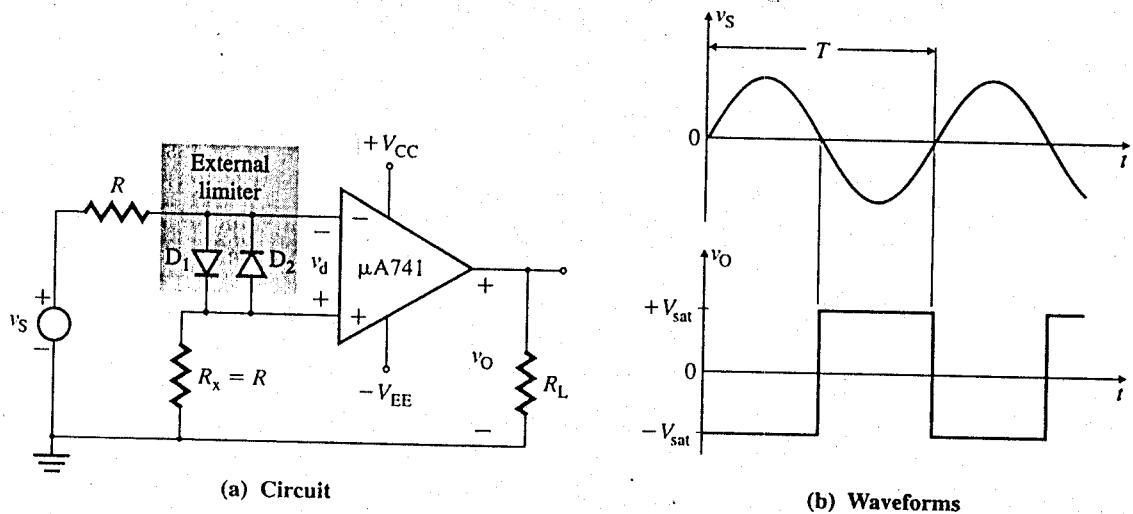
- A comparator compares a signal voltage on one input terminal with a known voltage, called the *reference voltage*, on the other input terminal. It is designed to operate under open-loop conditions, usually as a switching device. Comparators are often used as an interface between digital and analog signals.

- A comparator can be used as a *threshold comparator* in either inverting or noninverting mode. The voltage at which the comparator changes from one level to another is called the *crossover* (or *threshold*) voltage.

16.3 Zero-Crossing Detectors

A comparator can be used as a zero-crossing detector, as shown in Fig. 16.6(a). Input signal v_S is compared with a reference signal of 0 V. When v_S passes through zero in the positive direction, the output v_O is driven into negative saturation ($-V_{sat}$) as a result of the very high gain of the comparator. Conversely, when v_S passes through zero in the negative direction, the output is driven into positive saturation ($+V_{sat}$). The input and output waveforms are shown in Fig. 16.6(b).

FIGURE 16.6 Zero-crossing detector



Diodes D_1 and D_2 in Fig. 16.6(a) protect the comparator from damage due to excessive input voltage v_S . Because of these diodes, the differential input voltage v_d of the comparator is clamped to approximately 0.7 V or -0.7 V. These diodes, called *clamp diodes*, are external to the comparator. It is up to the designer to determine if the diodes are needed to protect the circuit. Resistance R is connected in series with input signal v_S to limit the current through D_1 and D_2 . Resistance R_x is used to reduce the effect of comparator offset problems.

If v_S is such that it crosses zero very slowly, then v_O may not switch quickly from one saturation voltage to the other. Instead, v_O may fluctuate between two saturation voltages $+V_{sat}$ and $-V_{sat}$ as a result of input offset voltage or noise signals at the comparator input terminals. Therefore, a zero-crossing detector will not be suitable for a low-frequency signal or a signal with noise superimposed on it.

KEY POINT OF SECTION 16.3

- A zero-crossing detector is a special application of a comparator in which the input signal is compared with a reference signal of 0 V.

16.4 ► Schmitt Triggers

Inverting Schmitt Trigger

A *Schmitt trigger* compares a regular or irregular waveform with a reference signal and converts the waveform to a square or pulse wave. A Schmitt trigger is often known as a *squaring circuit*. It is also known as a *bistable multivibrator*, because it has two stable states, low and high. It can remain in one state indefinitely; it moves to the other stable state only when a triggering signal is applied. Schmitt triggers can be classified into two types depending on the type of op-amp configuration used: inverting or noninverting.

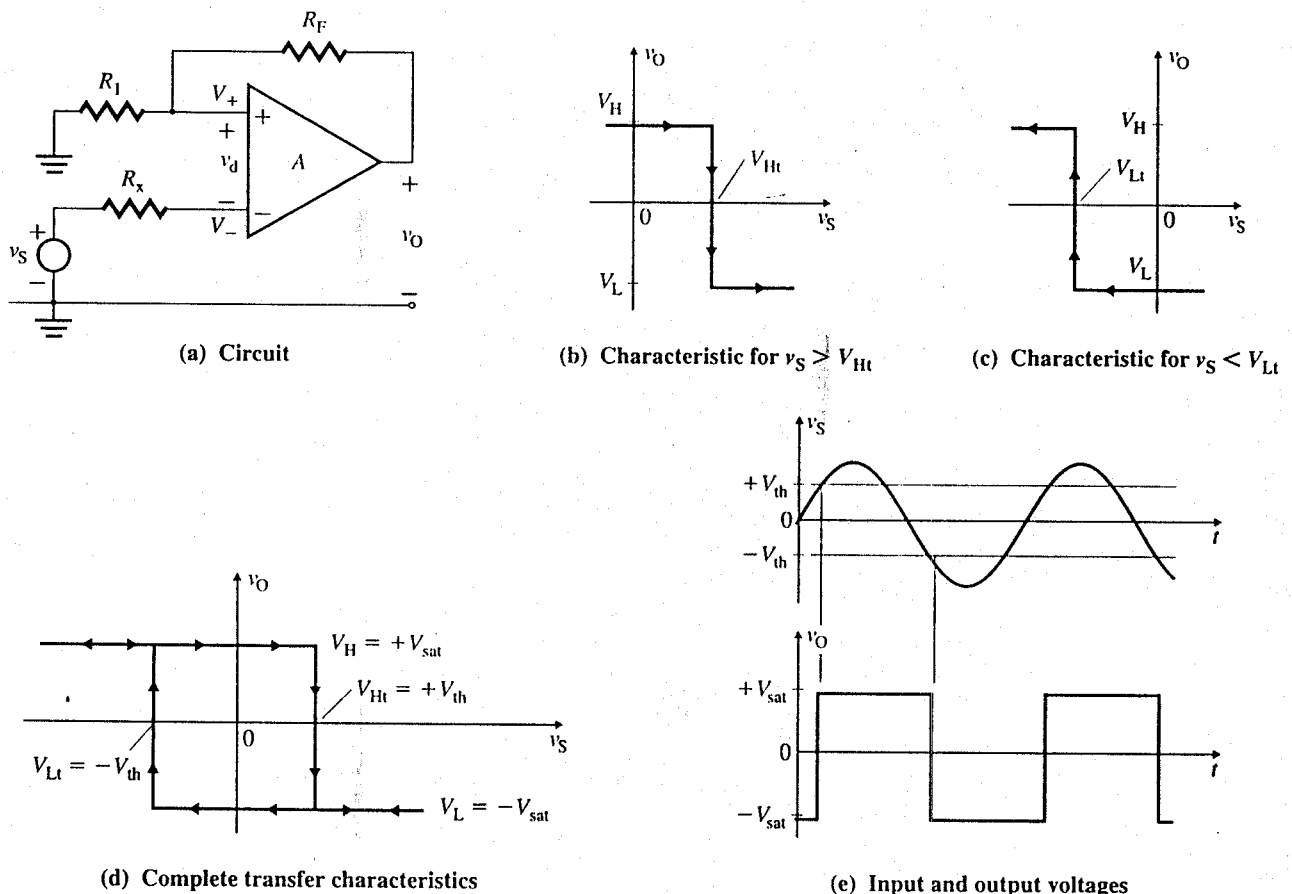
In an inverting Schmitt trigger, the input signal is applied to the inverting terminal of the comparator. The inverting threshold comparator in Fig. 16.4(a) can operate as an inverting Schmitt trigger if the resistance R_F is connected to the output side. This arrangement is shown in Fig. 16.7(a). The voltage divider consisting of R_1 and R_F will feed a fraction $\beta = R_1/(R_1 + R_F)$ of the output voltage back to the positive terminal of the comparator. If A is the open-loop gain of the comparator, the closed-loop voltage gain A_f is given by

$$A_f = \frac{v_O}{v_S} = \frac{-A}{1 - \beta A} \quad (16.4)$$

If $\beta A > 1$, which is usually the case, the feedback signal $V_+ = \beta v_O = \beta A_f v_S$ will be greater than its original value. For any change in v_S , the output v_O will continue to build up toward the saturation limit.

Transfer Characteristics To start with, let us assume that v_S is negative and the output is at the positive saturation voltage, $V_H = +V_{sat}$. If v_S is increased from 0, there will be no change in the output until v_S reaches a value of $v_S = V_+ = \beta V_{sat}$. If v_S begins to exceed $V_{Ht} = \beta V_{sat}$, the differential voltage v_d , which will be negative, will be amplified by the

FIGURE 16.7 Schmitt trigger



voltage gain A of the comparator. That is, v_O will be negative, thereby making V_+ negative also. The result will be an increase in the magnitude of the differential voltage v_d , and v_O will become more negative. This regenerative process will continue until eventually the comparator saturates, with its output voltage equal to the negative saturation voltage, $v_O = V_L = -V_{sat}$, and $V_+ = -\beta V_{sat}$. Increasing v_S beyond $v_S = \beta V_{sat}$ will have no effect on the state of the output voltage. The transfer characteristic for increasing v_S is shown in Fig. 16.7(b).

If v_S is decreased further while the output is low, there will be no change in the output until v_S goes negative, with a value of $v_S = V_+ = -\beta V_{sat}$. If v_S begins to exceed $V_{Lt} = -\beta V_{sat}$, the differential voltage v_d , which will be positive, will be amplified by the gain of the comparator. That is, V_+ will be positive. The result will be an increase in the differential voltage v_d , and v_O will become more positive. This regenerative process will continue until eventually the comparator saturates, with its output voltage equal to the positive saturation voltage, $v_O = V_H = +V_{sat}$, and $V_+ = \beta V_{sat}$. Decreasing v_S further ($v_S \leq -\beta V_{sat}$) will have no effect on the state of the output voltage. The transfer characteristic for decreasing v_S is shown in Fig. 16.7(c).

The complete transfer characteristics are shown in Fig. 16.7(d). A Schmitt trigger exhibits a *hysteresis*, or *deadband*, condition. That is, when the input of the Schmitt trigger exceeds $V_{Ht} = +V_{th}$, its output switches from $+V_{sat}$ to $-V_{sat}$, and when the input goes below $V_{Lt} = -V_{th}$, the output reverts to its original state, $+V_{sat}$.

Every time input voltage v_S exceeds certain levels, called the *upper threshold voltage* $+V_{th}$ and the *lower threshold voltage* $-V_{th}$, it changes the state of output voltage v_O . If the input signal is a sine wave, the output will be a square wave, as shown in Fig. 16.7(e). $+V_{th}$ and $-V_{th}$ are given by

$$+V_{th} = V_{Ht} = \frac{R_1}{R_1 + R_F} (+V_{sat}) \quad (16.5)$$

$$-V_{th} = V_{Lt} = \frac{R_1}{R_1 + R_F} (-V_{sat}) \quad (16.6)$$

where $V_{sat} = |+V_{sat}| = |-V_{sat}|$ and $V_{th} = |+V_{th}| = |-V_{th}|$.

Effect of Positive Feedback R_F provides positive feedback. As soon as the output voltage begins to change, positive feedback increases the differential voltage v_d , which, in turn, further changes the output voltage. Once a transition is initiated by a change in the input signal v_S , the positive feedback forces the comparator to complete the transition from one state to another rapidly and to operate in saturation, either positive or negative. Positive feedback leads to rapid transition of the output. Oscillations, which normally occur in the active region and hence prevail for a short time, are avoided.

EXAMPLE 16.1

D

Designing a Schmitt trigger with a hysteresis band

- (a) Design a Schmitt trigger as in Fig. 16.7(a) so that $V_{th} = +V_{th} = -V_{th} = 5$ V. Assume $V_{sat} = |-V_{sat}| = 14$ V.
 (b) Use PSpice/SPICE to plot the hysteresis characteristic for $v_S = 10 \sin(800\pi t)$.

SOLUTION

(a) The steps required to design the Schmitt trigger are as follows.

Step 1. Find the values of R_1 and R_F . From Eq. (16.5),

$$\begin{aligned} 1 + \frac{R_F}{R_1} &= \frac{V_{sat}}{V_{th}} \\ &= 14/5 = 2.8 \end{aligned} \quad (16.7)$$

so $R_F/R_1 = 2.8 - 1 = 1.8$. Let $R_1 = 10 \text{ k}\Omega$; then

$$R_F = 1.8 \times R_1 = 18 \text{ k}\Omega \quad (\text{use a } 20\text{-k}\Omega \text{ potentiometer})$$

Step 2. Choose the value of offset minimizing resistance R_x :

$$R_x = R_1 \parallel R_F = 10 \text{ k}\Omega \parallel 18 \text{ k}\Omega = 6.43 \text{ k}\Omega$$

(b) The circuit for PSpice simulation is shown in Fig. 16.8. The comparator is simulated by the PSpice macromodel of the LM111. In order to obtain the negative output voltage swing, terminal 1 is connected to the negative power supply instead of to the ground. The list of the circuit file is as follows.

Example 16.1 Schmitt Trigger

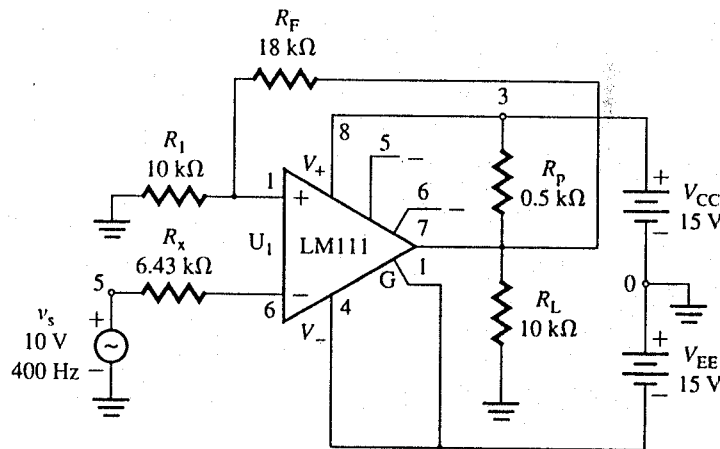
```

R1 0 1 10k
RF 1 2 18k
VCC 3 0 15V
VEE 0 4 15V
RL 2 0 10k
Vs 5 0 SIN (0 10V 400Hz)
Rx 5 6 8.43k
Rp 2 3 0.5k

.LIB NOM.LIB ; Call library file NOM.LIB for the LM111 comparator macromodel
* Connections:
*
* Noninverting input
*
* Inverting input
*
* Positive power supply
*
* Negative power supply
*
* Open-collector output
*
* Output ground (or negative)
*
XU1 1 6 3 4 2 4 LM111 ; Call LM111 comparator macromodel
*
* vi+ vi- vp+ vp -vo ground model name
*
.TRAN 1US 4MS
.PROBE
.END

```

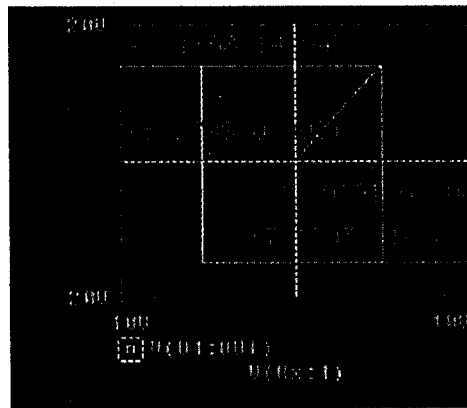
FIGURE 16.8 Schmitt trigger circuit for PSpice simulation



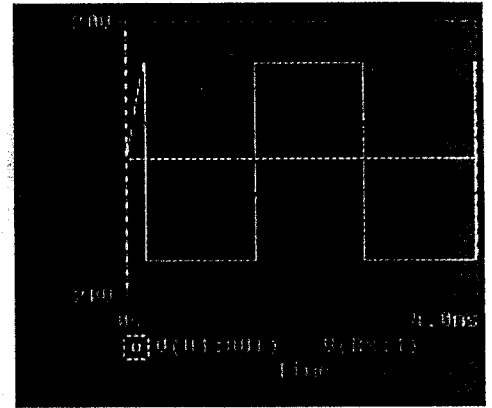
The transfer characteristic and the output voltage $v_O \equiv V(U1:OUT)$ (using EX16-1.SCH) are shown in Fig. 16.9(a) and (b), respectively. The simulated values are $V_{Ht} = 5.02 \text{ V}$ (expected value is 5 V), $V_{Lt} = -5.28 \text{ V}$ (expected value is -5 V), $V_{Ht} = 14.05 \text{ V}$ (expected value is 14 V), and

$V_L = -14.83$ V (expected value is -14 V). At the beginning, the output voltage varies linearly with the input voltage until the input reaches the threshold level, after which the transfer characteristic follows the normal hysteresis band. As a result, the transfer characteristic starts from the origin ($v_O = 0$ and $v_S = 0$). When the output transistor is off, the pull-up resistor R_P forms a potential divider with the load resistor R_L . As a result, the positive output voltage will depend on R_P , whose value should be made small compared to that of R_L . Notice that the transition from low to high and vice versa is very sharp because of the high slew rate of the comparator.

FIGURE 16.9 Transfer characteristic and output voltage for Example 16.1



(a) Transfer characteristic



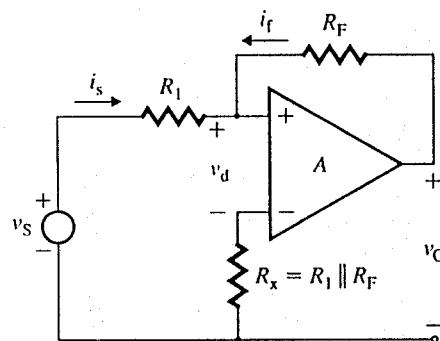
(b) Input and output voltages

Noninverting Schmitt Trigger

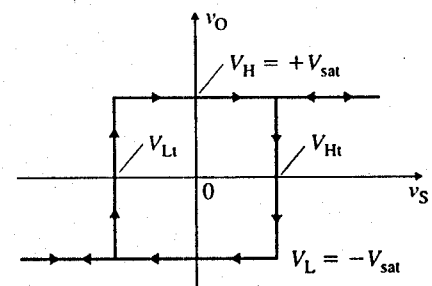
In a noninverting Schmitt trigger, the input signal is applied to the noninverting terminal of the comparator and the transfer characteristics are inverted. The noninverting threshold comparator in Fig. 16.3(a) can be operated as a noninverting Schmitt trigger if the resistance R_F is connected to the output side. This arrangement is shown in Fig. 16.10(a). Resistance R_F will feed a current signal, a fraction $\beta = 1/R_F$ of the output voltage, back to the positive terminal of the comparator, providing positive shunt-shunt feedback. As soon as the output voltage begins to change, the positive shunt-shunt feedback increases the feedback current i_F , which, in turn, increases the differential voltage v_d and hence further changes the output voltage. Once a transition is initiated by a change in the input signal v_S , positive feedback forces the comparator to complete the transition from one state to another rapidly and to operate in saturation, either positive or negative.

Transfer Characteristics To start with, let us assume that v_S is negative and the output is at the negative saturation voltage, $V_L = -V_{sat}$. If v_S is increased from a relatively large negative value, there will be no change in the output until v_S reaches a value of

FIGURE 16.10
Noninverting Schmitt trigger



(a) Circuit



(b) Transfer characteristics

$v_S = V_{Lt} = -V_{sat}R_1/R_F$. If v_S begins to exceed V_{Lt} , the differential voltage v_d , which will be positive, will be amplified by the voltage gain A of the comparator. That is, v_O will be positive, thereby making v_+ positive also. The result will be an increase in the magnitude of the differential voltage v_d , and v_O will become more positive. This regenerative process will continue until eventually the comparator saturates, with its output voltage equal to the positive saturation voltage, $V_H = +V_{sat}$. Increasing v_S further ($v_S \geq V_{Lt}$) will have no effect on the state of the output voltage.

If v_S is decreased while the output is high, there will be no change in the output until v_S decreases to a value of $v_S = V_{Ht} = +V_{sat}R_1/R_F$. If v_S begins to decrease beyond V_{Ht} , the differential voltage v_d will be negative and will be amplified by the gain of the comparator. As a result, v_O will become more negative. This regenerative process will continue until eventually the comparator saturates, with its output voltage equal to the negative saturation voltage $-V_{sat}$. Decreasing v_S further ($v_S \leq V_{Ht}$) will have no effect on the state of the output voltage. The complete transfer characteristics are shown in Fig. 16.10(b).

Schmitt Trigger with Reference Voltage

The *switching voltage* of a Schmitt trigger circuit is defined as the average of V_{Lt} and V_{Ht} . For the circuits in Figs. 16.7(a) and 16.10(a), $V_{Lt} = -V_{Ht}$, and hence the switching voltage V_{st} , which is the width of the hysteresis band, is zero—that is, $V_{st} = (V_{Lt} + V_{Ht})/2 = 0$. However, some applications require shifting the crossover voltage in either the positive or the negative direction along the v_S -axis. This can be accomplished by adding a reference voltage V_{ref} to the circuit in Fig. 16.7(a), as shown in Fig. 16.11(a) for a noninverting Schmitt trigger. The complete transfer characteristics are shown in Fig. 16.11(b). Assuming V_{Lt} and V_{Ht} are symmetrical about the zero-axis, the switching voltage is given by

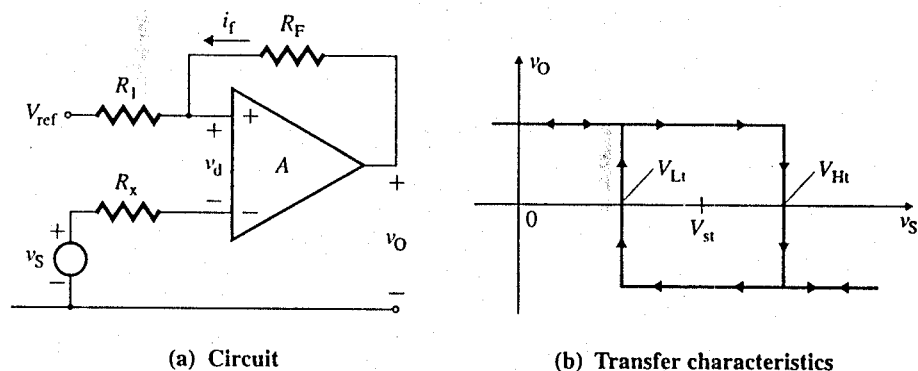
$$V_{st} = \frac{R_F}{R_1 + R_F} V_{ref} \quad (16.8)$$

Thus, the upper and lower crossover voltages become

$$V_{Ht} = V_{st} + \frac{R_1}{R_1 + R_F} (+V_{sat}) \quad (16.9)$$

$$V_{Lt} = V_{st} + \frac{R_1}{R_1 + R_F} (-V_{sat}) \quad (16.10)$$

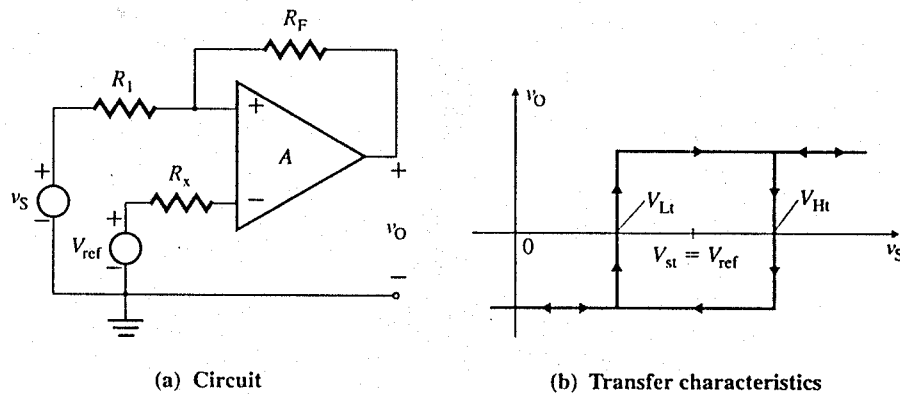
FIGURE 16.11
Noninverting Schmitt trigger with reference voltage



The direction of the hysteresis loop in Fig. 16.11(b) can be reversed by applying a reference voltage V_{ref} to the circuit in Fig. 16.10(a). This arrangement is shown in Fig. 16.12(a), and the corresponding transfer characteristics are shown in Fig. 16.12(b).

FIGURE 16.12

Noninverting Schmitt trigger with reference voltage

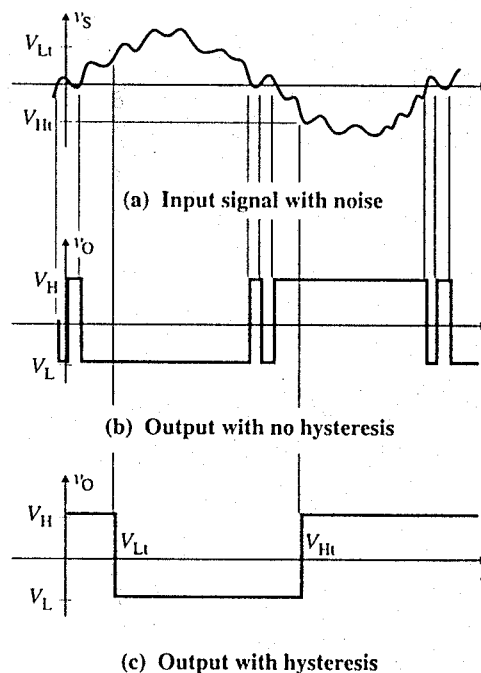


Effects of Hysteresis on the Output Voltage

In order to understand the effect of the *hysteresis*, or *deadband*, condition, consider a sinusoidal signal with a noise signal superimposed on it, as shown in Fig. 16.13(a). If there is no hysteresis, the output voltage will change to its saturation limit when the input signal v_s crosses zero, as shown in Fig. 16.13(b). However, if the output is made to change when the input signal exceeds specified voltage limits V_{Ht} and V_{Lt} , there will be less switching of the output voltage, as shown in Fig. 16.13(c). As a result, any unwanted signal (e.g., noise) will not make the output change. Also, a deadband can be used to reduce the number of contact-bounces in a system such as a temperature-control system, in which the heating element turns on or off when the temperature falls below or rises above the set value.

FIGURE 16.13

Effects of hysteresis on the output voltage



EXAMPLE 16.2

D

Designing a Schmitt trigger with a shifted hysteresis band

- Design a Schmitt trigger as in Fig. 16.11(a) so that $V_{Ht} = 7\text{ V}$ and $V_{Lt} = 3\text{ V}$. Assume $V_{sat} = -V_{sat} = 14\text{ V}$ and an input frequency of $f = 400\text{ Hz}$. Determine the values of R_1 , R_F , and V_{ref} .
- Use PSpice/SPICE to plot the hysteresis characteristic for $v_s = 10 \sin(800\pi t)$. Use the macro-model of the $\mu A741$ op-amp.

SOLUTION

- The Schmitt trigger can be designed using the following steps.

Step 1. Find the values of R_1 and R_F . From Eqs. (16.9) and (16.10), we can find the input width of the hysteresis band (HB) as follows:

$$HB = V_{Ht} - V_{Lt} = \frac{2R_1}{R_1 + R_F} V_{sat}$$

which gives

$$1 + \frac{R_F}{R_1} = \frac{2V_{sat}}{V_{Ht} - V_{Lt}} = \frac{2 \times 14}{7 - 3} = 7$$

Let $R_1 = 10 \text{ k}\Omega$; then $R_F = (7 - 1) \times R_1 = 60 \text{ k}\Omega$.

Step 2. Determine the value of reference voltage V_{ref} .

$$V_{st} = \frac{R_F}{R_1 + R_F} V_{ref} = \frac{V_{Ht} + V_{Lt}}{2} = \frac{7 + 3}{2} = 5 \text{ V}$$

which gives $V_{ref} = 5.83 \text{ V}$.

(b) We will use op-amp $\mu A741$ rather than comparator LM111 to illustrate the advantage of a comparator in a Schmitt trigger. The circuit for PSpice simulation is shown in Fig. 16.14. The list of the circuit file is as follows.

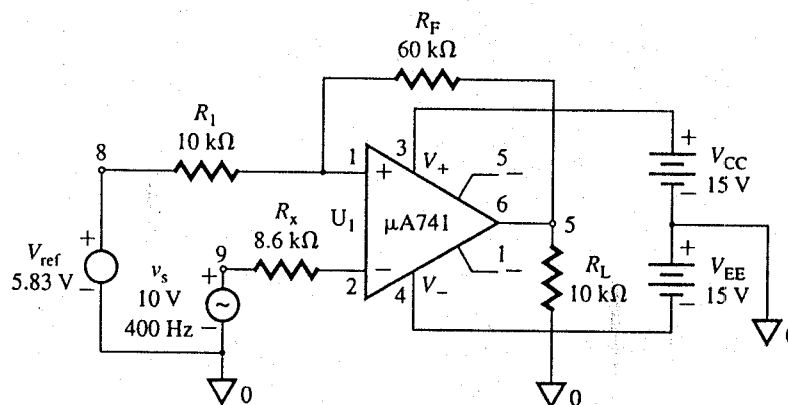
Example 16.2 Schmitt Trigger with a Shifted Hysteresis Band

```

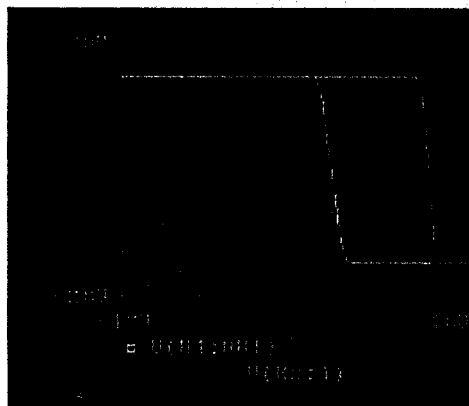
R1      8  1  10k
RF      1  5  60k
Vref    8  0  DC   5.83V
VCC     3  0  15V
VEE     0  4  15V
RL      0  5  10k
Vs      9  0  SIN (0 10V 400Hz)
Rx      9  2  8.6k
.LIB NOM.LIB ; Call library file EVAL.LIB for the UA741 op-amp macromodel
XU1     1  2  3  4  5  ua741 ; Call UA741 op-amp macromodel
*      vi+ vi- vp+ vp- vo
.TRAN   1US 4MS ; Transient analysis
.PROBE ; Graphics post-processor
.END

```

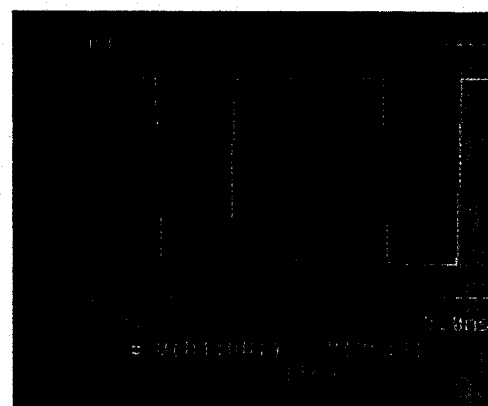
FIGURE 16.14 Schmitt trigger circuit for PSpice simulation



The transfer characteristic and the output voltage (using EX16-2.SCH) are shown in Fig. 16.15(a), which gives $V_{Ht} = 7.03 \text{ V}$ (expected value is 7 V), $V_{Lt} = 3.03 \text{ V}$ (expected value is 3 V), and $V_{sat} = 14.6 \text{ V}$ (expected value is 14 V). The transition from low to high and vice versa is not very sharp, as a result of the low slew rate of the op-amp (compared to that of a comparator, shown in Fig. 16.9).

FIGURE 16.15 Transfer characteristic and output voltage for Example 16.2

(a) Transfer characteristic



(b) Input and output voltages

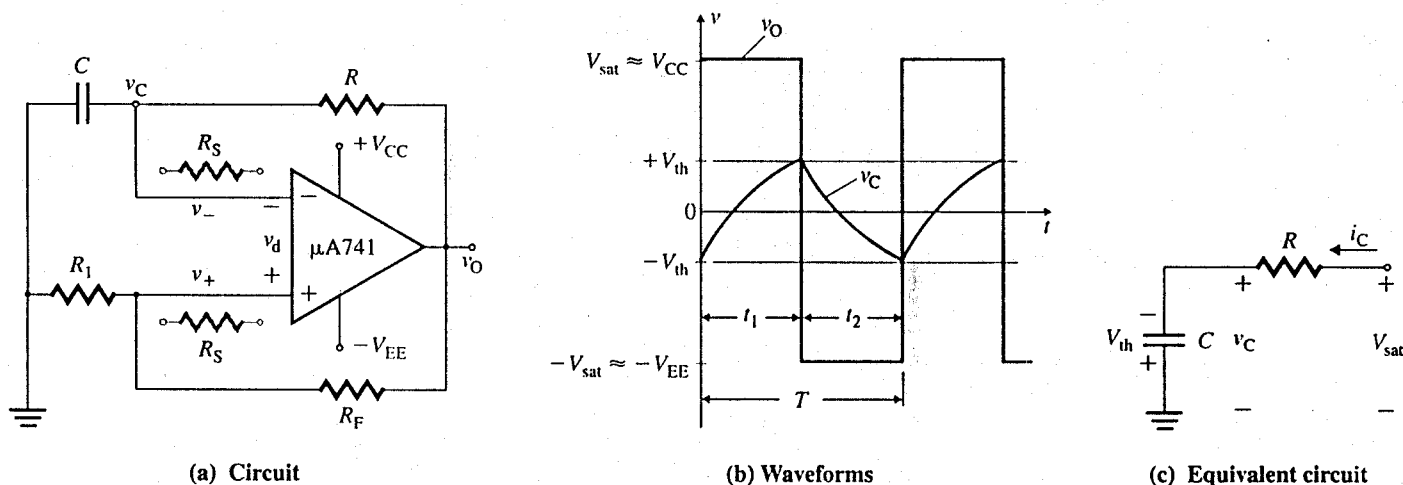
KEY POINTS OF SECTION 16.4

- A *Schmitt trigger* compares a regular or irregular waveform with a reference signal and converts the waveform to a square or pulse wave. A Schmitt trigger is often known as a *squaring circuit*. It is also known as a *bistable multivibrator*, because it has two stable states, low and high. Schmitt triggers can be classified into two types depending on the type of op-amp configuration used: inverting or noninverting.
- A Schmitt trigger exhibits a *hysteresis*, or *deadband*, condition. That is, when the input of the Schmitt trigger exceeds $+V_{th}$, its output switches from $+V_{sat}$ to $-V_{sat}$, and when the input goes below $-V_{th}$, the output reverts to its original state, $+V_{sat}$.
- When a general-purpose op-amp (e.g., $\mu A741$) is used to generate the characteristic of a hysteresis loop, the transition from low to high and vice versa is not as sharp as it is with a comparator.

16.5

Square-Wave Generators

A square wave can be generated if the output of an op-amp is forced to swing repetitively between positive saturation $+V_{sat}$ and negative saturation $-V_{sat}$. This can be accomplished by connecting a bistable multivibrator (or Schmitt trigger) with an RC circuit in the feedback loop. The circuit implementation is shown in Fig. 16.16(a). This square-wave

FIGURE 16.16 Square-wave generator

generator is also called a *free-running* or *astable multivibrator*, because the output does not have any stable state. The output of the op-amp will be in either positive saturation or negative saturation, depending on whether the differential input voltage v_d is positive or negative.

Assuming the voltage across capacitor C is zero, the voltage at the inverting terminal is zero initially—that is, $v_- = 0$ at the instant the dc supply voltages V_{CC} and V_{EE} are turned on. However, at the same instant, the voltage v_+ at the noninverting terminal will have a very small value that will depend on the output offset voltage V_{OO} . That is,

$$v_d = v_+ - v_- = v_+ = V_{OO}$$

which has a positive value. But v_d will be amplified as a result of the very large gain of the op-amp (typically 2×10^5) and will drive the output of the op-amp to positive saturation $+V_{sat}$. Capacitor C will start charging toward $+V_{sat}$ through R . However, as soon as the voltage across C , which is equal to v_- , is slightly more than v_+ , then $v_d = v_+ - v_-$ will become negative and the output of the op-amp will switch to negative saturation $-V_{sat}$. The operation of the circuit can be divided into two modes: mode 1 for $v_d > 0$ V and mode 2 for $v_d < 0$ V.

During mode 1, $v_d > 0$ V and the output voltage of the op-amp is at positive saturation $+V_{sat}$. The voltage v_+ becomes

$$v_+ = \frac{R_1}{R_1 + R_F} (+V_{sat}) \quad (16.11)$$

Capacitor C will again start charging toward $+V_{sat}$ through R . As soon as the voltage across C is slightly more than v_+ , then $v_d = v_+ - v_-$ will become negative and the output of the op-amp will be forced to switch to negative saturation $-V_{sat}$.

During mode 2, $v_d < 0$ V and the op-amp's output voltage is at negative saturation $-V_{sat}$. The voltage v_+ follows the voltage divider rule and can be found from

$$v_+ = \frac{R_1}{R_1 + R_F} (-V_{sat}) \quad (16.12)$$

As long as v_d is negative, the output will remain in negative saturation. The capacitor will discharge and then recharge toward $-V_{sat}$ through R . When the voltage across C is slightly more negative than v_+ , then $v_d = v_+ - v_-$ will become positive and the output of the op-amp will be forced to switch to positive saturation $+V_{sat}$. Then mode 1 begins again, and the cycle is repeated.

Voltage v_+ acts as the reference. The capacitor voltage v_- tries to follow v_+ . However, as soon as the magnitude of v_- becomes slightly greater than that of v_+ , v_+ switches its polarity. As a result, the output swings from positive to negative and vice versa. The waveforms of the output voltage and capacitor voltage are shown in Fig. 16.16(b).

Assuming $+V_{sat}$ is the output voltage and the capacitor has an initial voltage of $-V_{th}$ during mode 1, the equivalent circuit during the charging period is as shown in Fig. 16.16(c). Using Kirchhoff's voltage law, we can write

$$V_{sat} = Ri_C + \frac{1}{C} \int i_C dt - V_{th}$$

which gives the charging current $i_C(t)$ as

$$i_C(t) = \frac{V_{sat} + V_{th}}{R} e^{-t/RC} \quad (16.13)$$

$$\text{where} \quad V_{th} = \frac{R_1}{R_1 + R_F} V_{sat} \quad (16.14)$$

The capacitor voltage $v_C(t)$ can be found from

$$v_C(t) = V_{\text{sat}} - (V_{\text{sat}} + V_{\text{th}})e^{-t/RC} \quad (16.15)$$

At $t = t_1$, the capacitor is recharged to V_{th} . That is, $v_C(t = t_1) = V_{\text{th}}$. From Eq. (16.15), we get

$$V_{\text{th}} = V_{\text{sat}} - (V_{\text{sat}} + V_{\text{th}})e^{-t_1/RC} \quad (16.16)$$

which gives

$$\begin{aligned} t_1 &= -RC \ln \frac{V_{\text{sat}} - V_{\text{th}}}{V_{\text{sat}} + V_{\text{th}}} = -RC \ln \frac{V_{\text{sat}} - R_1 V_{\text{sat}}/(R_1 + R_F)}{V_{\text{sat}} + R_1 V_{\text{sat}}/(R_1 + R_F)} \\ &= -RC \ln \frac{R_F}{2R_1 + R_F} = RC \ln \frac{2R_1 + R_F}{R_F} \end{aligned} \quad (16.17)$$

The period T of the output voltage is given by

$$T = t_1 + t_2 = 2t_1 = 2RC \ln \frac{2R_1 + R_F}{R_F} = 2RC \ln \left(1 + \frac{2R_1}{R_F} \right) \quad (16.18)$$

Thus, the frequency of the output voltage f_o is given by

$$f_o = \frac{1}{T} = \frac{1}{2RC \ln (1 + 2R_1/R_F)} \quad (16.19)$$

Equation (16.19) shows that the output frequency depends not only on the time constant $\tau = RC$, but also on the relationship between R_1 and R_F . If $R_F \approx 1.164R_1$, Eq. (16.19) is reduced to

$$f_o = \frac{1}{2RC} \quad (16.20)$$

► **NOTES:**

1. The inputs of the op-amp are subjected to large differential voltages. To prevent excessive differential current flow to the op-amp, a series resistance R_S , typically on the order of 100 k Ω , can be connected to each of the inverting and noninverting terminals of the op-amp.
2. The peak-to-peak output voltage can be reduced by connecting a pair of zener diodes back to back at the output terminal.

EXAMPLE 16.3

D

Designing a square-wave generator

- (a) Design the square-wave generator shown in Fig. 16.16(a) so that $f_o = 5$ kHz. Assume $+V_{\text{sat}} = +14$ V, $-V_{\text{sat}} = -14$ V.
- (b) Use PSpice/SPICE to check your design. Use the macromodel of the LM111 for sharper transition.

SOLUTION

(a) The steps used to design the square-wave generator are as follows.

Step 1. Choose the value of R_1 : Let $R_1 = 10$ k Ω .

Step 2. To simplify the design, choose $R_F = 1.164R_1$ and find R_F :

$$R_F = 1.164R_1 = 1.164 \times 10 \text{ k}\Omega = 11.64 \text{ k}\Omega \quad (\text{use a 20-k}\Omega \text{ potentiometer})$$

Step 3. Choose a value of C : Let $C = 0.01$ μ F.

Step 4. Find the value of R from Eq. (16.20):

$$R = \frac{1}{2Cf_o} = \frac{1}{2 \times 0.01 \mu\text{F} \times 5 \text{ kHz}} = 10 \text{ k}\Omega$$

(b) The circuit for PSpice simulation is shown in Fig. 16.17. The list of the circuit file is as follows.

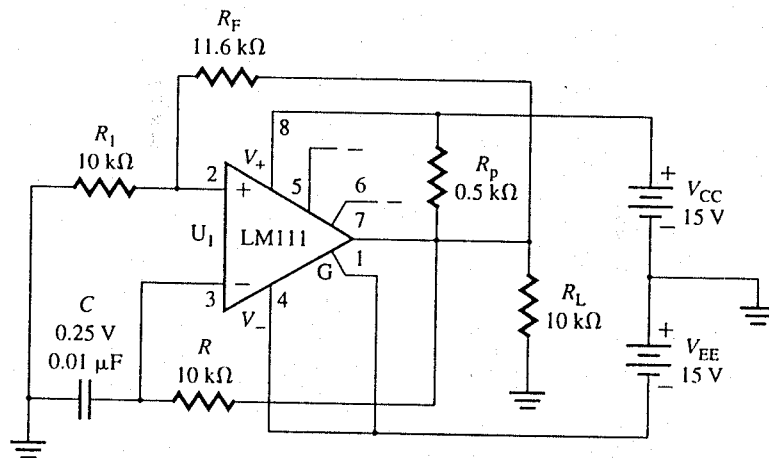
Example 16.3 Square-Wave Generator

```

R1  0  1  10k
RF  1  2  11.6k
VCC 3  0  15V
VEE 0  4  15V
RL  0  2  10k
R  5  2  10k
C  0  5  0.01μF IC=0.25V ; Assign an initial condition
Rp  2  3  0.5k

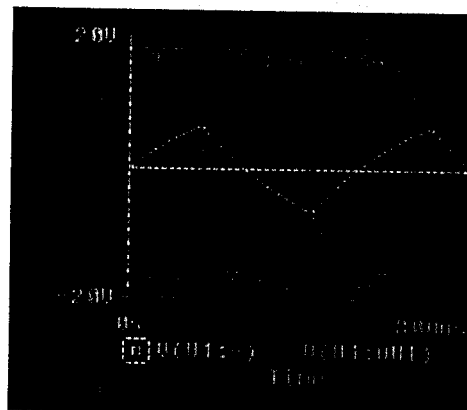
.LIB NOM.LIB ; Call library file NOM.LIB for the LM111 comparator macromodel
XU1 1  5  3  4  2  4 LM111 ; Call LM111
* vi+ vi- vp+ vp -vo ground model name
.TRAN 1US 300US UIC ; Transient analysis using initial condition
.PROBE
.END
  
```

FIGURE 16.17 Square-wave generator for PSpice simulation



The output waveforms (using EX16-3.SCH) are shown in Fig. 16.18. The results are $V_{sat} = 13.53$ V (expected value is 14 V), $-V_{sat} = -14.83$ V (expected value is -14 V), $V_{th} = 6.3$ V, $-V_{th} = -6.8$ V, and $T = 2 \times (267.5 - 162.5) = 210$ μ s (expected value is 200 μ s). The output voltage does not change sharply from one state to another. It is not a full square wave because of the slew rate and bandwidth limits of the op-amp.

FIGURE 16.18 Output voltage waveforms for Example 16.3



KEY POINT OF SECTION 16.5

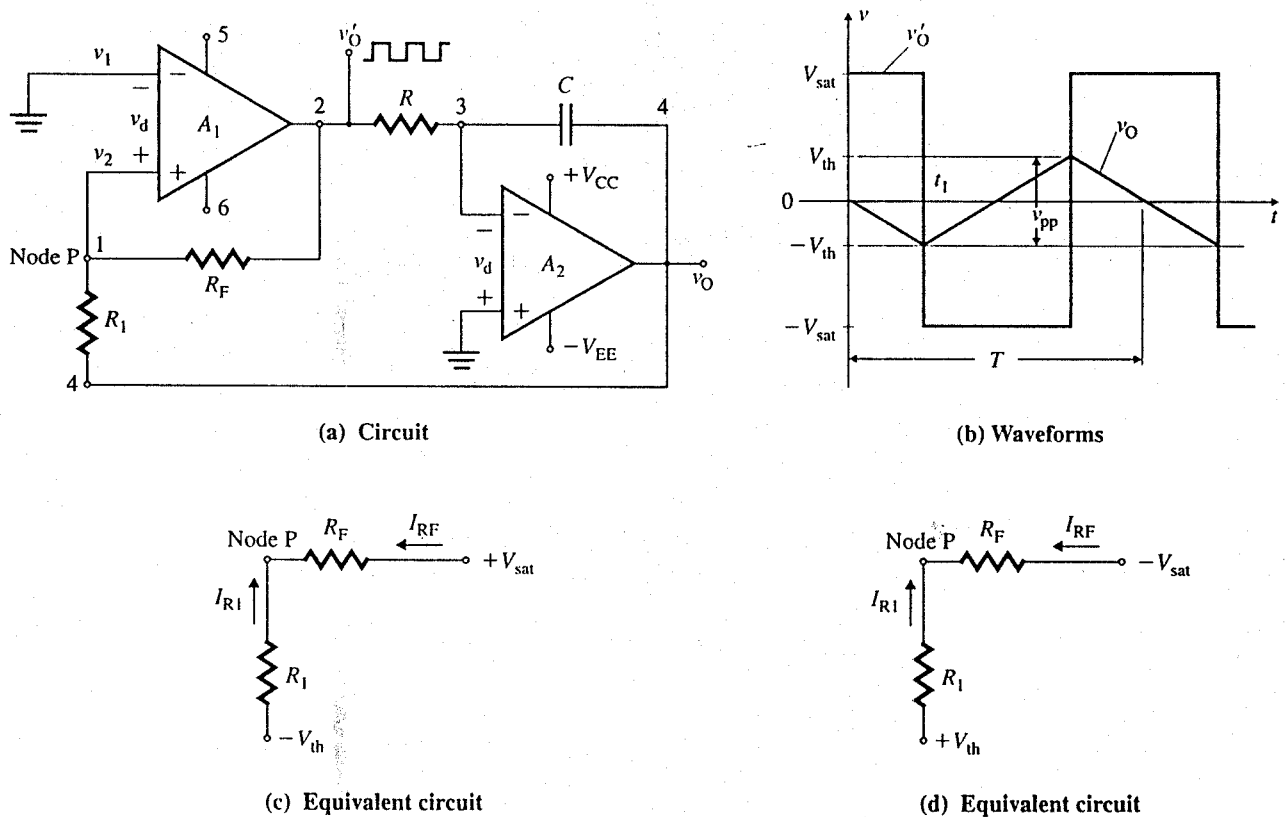
- A square wave can be generated by forcing the output of an op-amp to swing repetitively between positive saturation $+V_{\text{sat}}$ and negative saturation $-V_{\text{sat}}$. This is accomplished by connecting a bistable multivibrator (or Schmitt trigger) in the feedback loop. This square-wave generator is also called a *free-running* or *astable multivibrator*.

16.6 Triangular-Wave Generators

A triangular-wave generator can be produced by integrating the square-wave output of a Schmitt trigger circuit. This can be accomplished by cascading an integrator with a bistable multivibrator (or Schmitt trigger), as shown in Fig. 16.19(a), which consists of a comparator A_1 and an integrator A_2 . Comparator A_1 continuously compares the noninverting input v_+ at point P with the inverting input v_- (that is, 0 V). Thus, the differential voltage is $v_d = v_+ - v_- = v_+$. Because of the very large gain of the op-amp, the output of A_1 will be at negative saturation $-V_{\text{sat}}$ or positive saturation $+V_{\text{sat}}$ when v_+ goes slightly below or above 0 V, respectively.

To examine the principle of operation of the triangular-wave generator, let us assume that when the supply voltages V_{CC} and $-V_{\text{EE}}$ are switched on, the voltage at the noninverting terminal begins slightly above 0 V as a result of the input offset voltage of the op-amp. Because of the high gain of the op-amp, the output of A_1 will be switched to positive saturation $+V_{\text{sat}}$. Therefore, the output of the op-amp is forced to swing repetitively between positive saturation $+V_{\text{sat}}$ and negative saturation $-V_{\text{sat}}$. The output voltages of A_1 and A_2 are shown in Fig. 16.19(b). The operation of the circuit can be divided into two modes.

FIGURE 16.19 Triangular-wave generator



During mode 1, $v_+ > 0$ V and the output of A_1 is at positive saturation $+V_{\text{sat}}$, which is the input to the inverting integrator A_2 . The output of A_2 will be a negative-going ramp. Thus, one side of R_F will be at $+V_{\text{sat}}$, and one side of R_1 will be at the negative-going ramp of A_2 . When the negative-going ramp exceeds a certain value $-V_{\text{th}}$, the voltage at point P will be slightly below 0 V, and the output of A_1 will switch from positive saturation $+V_{\text{sat}}$ to negative saturation $-V_{\text{sat}}$.

The equivalent circuit for determining the condition under which the circuit switches over to negative saturation is shown in Fig. 16.19(c). Since the current flowing into the op-amp is negligible, $I_{R1} = -I_{RF}$. That is,

$$\frac{-V_{\text{th}}}{R_1} = \frac{-V_{\text{sat}}}{R_F}$$

which gives the condition for $v_+ < 0$ V as

$$-V_{\text{th}} = \frac{R_1}{R_F} (-V_{\text{sat}}) \quad (16.21)$$

During mode 2, $v_+ < 0$ V and the output of A_1 is at negative saturation $-V_{\text{sat}}$, which is the input to the integrator A_2 . The output of A_2 will be a positive-going ramp. When the positive-going ramp exceeds a certain value $+V_{\text{th}}$, the voltage at point P will be slightly above 0 V, and the output of A_1 will switch from negative saturation $-V_{\text{sat}}$ to positive saturation $+V_{\text{sat}}$. When this occurs, mode 1 starts again, and the cycle is repeated.

The equivalent circuit for determining the condition under which the circuit switches over to positive saturation is shown in Fig. 16.19(d). Neglecting the current flowing into the op-amp, we have $I_{R1} = -I_{RF}$. That is,

$$\frac{V_{\text{th}}}{R_1} = \frac{V_{\text{sat}}}{R_F}$$

which gives the condition for $v_+ > 0$ V as

$$V_{\text{th}} = \frac{R_1}{R_F} (+V_{\text{sat}}) \quad (16.22)$$

where $V_{\text{sat}} = |+V_{\text{sat}}| = |-V_{\text{sat}}|$. The peak-to-peak output amplitude of the triangular wave is given by

$$v_{\text{pp}} = V_{\text{th}} - (-V_{\text{th}}) = \frac{2R_1}{R_F} V_{\text{sat}} \quad (16.23)$$

The period and the frequency of the output voltage can be determined from the time that is required to charge the capacitor from $-V_{\text{th}}$ to V_{th} or from V_{th} to $-V_{\text{th}}$. Let us consider the capacitor voltage during mode 2, when the input voltage to the integrator is $-V_{\text{sat}}$. That is,

$$\begin{aligned} v_C(t) &= -\frac{1}{RC} \int v_O' dt - V_{\text{th}} = -\frac{1}{RC} \int (-V_{\text{sat}}) dt - V_{\text{th}} \\ &= \frac{V_{\text{sat}}}{RC} t - V_{\text{th}} \end{aligned} \quad (16.24)$$

At half period, $t = t_1 = T/2$ and $v_C(t = T/2) = V_{\text{th}}$, and Eq. (16.24) yields

$$V_{\text{th}} = \frac{V_{\text{sat}}}{RC} \left(\frac{T}{2} \right) - V_{\text{th}}$$

which gives the period as

$$T = \frac{4RCV_{th}}{V_{sat}} \quad (16.25)$$

Substituting the value of V_{th} from Eq. (16.22), we have for the period of the triangular wave

$$T = \frac{4RC}{V_{sat}} \times \frac{R_1 V_{sat}}{R_F} = \frac{4RCR_1}{R_F} \quad (16.26)$$

which gives the frequency of oscillation as

$$f_o = \frac{R_F}{4RCR_1} \quad (16.27)$$

EXAMPLE 16.4

D

Designing a triangular-wave generator

- (a) Design the triangular-wave generator shown in Fig. 16.19(a) so that $f_o = 4$ kHz and $V_{th} = | -V_{th} | = 5$ V. Assume $+V_{sat} = | -V_{sat} | = 14$ V.
 (b) Use PSpice/SPICE to check your design.

SOLUTION

- (a) The steps used to design the triangular-wave generator are as follows.

Step 1. Find the values of R_1 and R_F . Equation (16.22) gives

$$\frac{R_1}{R_F} = \frac{V_{th}}{V_{sat}} = \frac{5}{14} = 0.36$$

Let $R_1 = 10$ k Ω ; then

$$R_F = R_1 / 0.36 = 10 \text{ k}\Omega / 0.36 = 28 \text{ k}\Omega \quad (\text{use a 30-k}\Omega \text{ potentiometer})$$

Step 2. Choose a suitable value of C : Let $C = 0.01$ μ F.

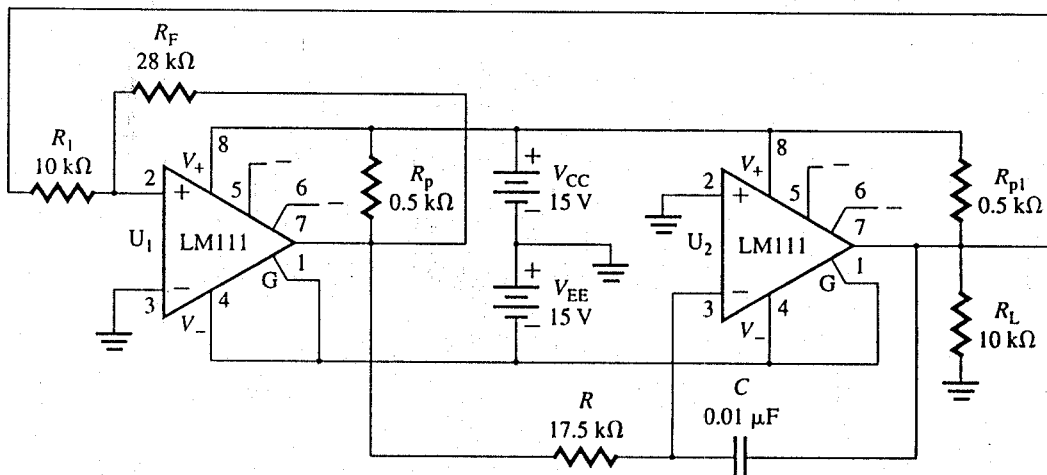
Step 3. Find the value of R . Equation (16.27) gives

$$R = \frac{R_F}{4f_o C R_1} \quad (16.28)$$

$$= \frac{28 \text{ k}\Omega}{4 \times 4 \text{ kHz} \times 0.01 \text{ }\mu\text{F} \times 10 \text{ k}\Omega} = 17.5 \text{ k}\Omega \quad (\text{use a 20-k}\Omega \text{ potentiometer})$$

- (b) The circuit for PSpice simulation is shown in Fig. 16.20. The op-amp is simulated by PSpice macromodel LM111. The list of the circuit file is as follows.

FIGURE 16.20 Triangular-wave generator for PSpice simulation



Example 16.4 Triangular-Wave Generator

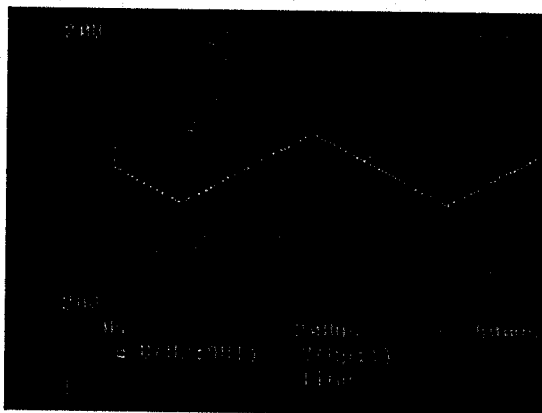
```

R1  2  1  10k
RF  1  3  28k
VCC 4  0  15V
VEE 0  5  15V
RL  2  0  10k           ; Load resistance
R   3  6  17.5k
C   6  2  0.01uF
Rp  3  4  0.5k
Rpl 2  4  0.5k
.LIB NOM.LIB           ; Call library file NOM.LIB for the LM111 macromodel
XU1 1  0  4  5  3  5  LM111
XU2 0  6  4  5  2  5  LM111
* vi+ vi- vp+ vp -vo ground model name
.TRAN 1US 400US UIC    ; Transient analysis using initial condition
.PROBE
.END

```

The PSpice plots of the voltages at the output of amplifiers A_1 and A_2 (using EX16-4.SCH) are shown in Fig. 16.21. The results are $V_{\text{sat}} = 14.4 \text{ V}$ (expected value is 14 V), $-V_{\text{sat}} = -14.8 \text{ V}$ (expected value is -14 V), $V_{\text{th}} = 5.3 \text{ V}$ (expected value is 5 V), $-V_{\text{th}} = -5.2 \text{ V}$ (expected value is -5 V), and $T = 312.1 - 62.6 = 249.5 \mu\text{s}$ (expected value is $250 \mu\text{s}$). If the integrator time constant $\tau = RC$ is made much smaller than the period of the output waveform, the triangular wave can be made very close to a sine wave.

FIGURE 16.21 Output waveforms for Example 16.4



KEY POINTS OF SECTION 16.6

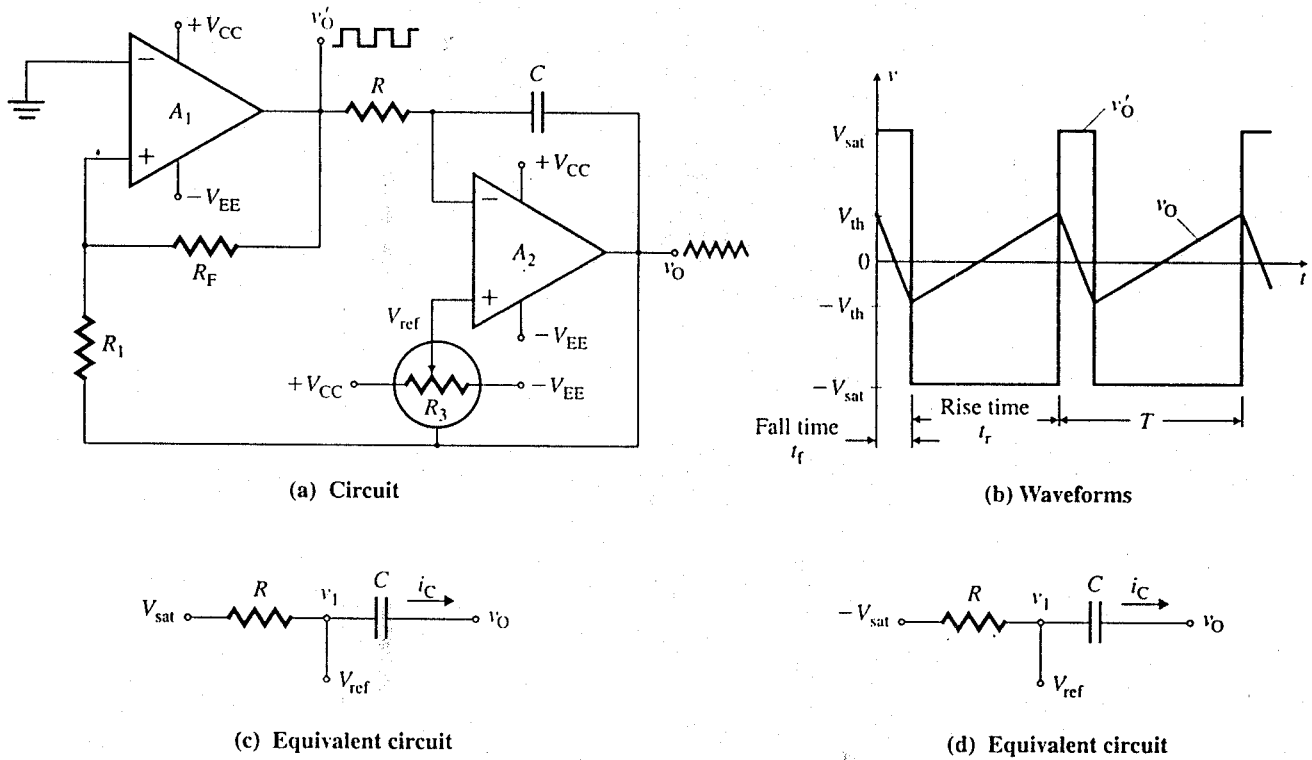
- A triangular-wave generator can be produced by integrating the square-wave output of a Schmitt trigger. This can be accomplished by cascading an integrator with a bistable multivibrator (or Schmitt trigger).
- If the integrator time constant $\tau = RC$ is made much smaller than the period of the output waveform, the triangular wave can be made very close to a sine wave.

16.7 Sawtooth-Wave Generators

In a triangular waveform, the rise time is always equal to the fall time. That is, the same amount of time is required for a triangular wave to swing from $-V_{\text{th}}$ to $+V_{\text{th}}$ as from $+V_{\text{th}}$ to $-V_{\text{th}}$. On the other hand, a sawtooth waveform has unequal rise and fall times. The rise time may be faster than the fall time or vice versa. The triangular-wave generator in

Fig. 16.19(a) may be converted to a sawtooth generator by adding a variable dc voltage V_{ref} to the noninverting terminal of the op-amp. The addition of V_{ref} , which acts as a reference signal for the integrator A_2 , can be accomplished by using a potentiometer, as shown in Fig. 16.22(a). The voltage waveforms are shown in Fig. 16.22(b). As with the triangular-wave generator, the operation of the circuit can be divided into two modes.

FIGURE 16.22 Sawtooth-wave generator



During mode 1, $v_+ > 0$ V and the output of A_1 is at positive saturation $+V_{\text{sat}}$, which is the input signal to the integrator A_2 . The equivalent circuit for the operation of the integrator is shown in Fig. 16.22(c). At the beginning of this mode, the output voltage is V_{th} and the voltage at the inverting terminal is $v_1 \approx V_{\text{ref}}$. Thus, the initial voltage on the capacitor is

$$v_C(t = 0) = v_1 - v_O = V_{\text{ref}} - V_{\text{th}}$$

The instantaneous voltage across the capacitor $v_C(t)$ is given by

$$V_{\text{ref}} - v_O(t) = \frac{1}{C} \int i_C dt + v_C(t = 0) = \frac{1}{C} \int \frac{V_{\text{sat}} - V_{\text{ref}}}{R} dt + V_{\text{ref}} - V_{\text{th}}$$

which gives the instantaneous output voltage as

$$v_O(t) = V_{\text{th}} - \frac{V_{\text{sat}} - V_{\text{ref}}}{RC} t \quad (16.29)$$

At the end of this mode (at $t = t_1$), the output voltage has changed to $-V_{\text{th}}$, whose value can be found from Eq. (16.21). That is, $v_O(t = t_1) = -V_{\text{th}}$. From Eq. (16.29),

$$-V_{\text{th}} = V_{\text{th}} - \frac{V_{\text{sat}} - V_{\text{ref}}}{RC} t_1$$

which gives the duration of mode 1 as

$$t_1 = \frac{2RCV_{th}}{V_{sat} - V_{ref}} \quad (16.30)$$

During mode 2, $v_+ < 0$ V and the output of A_1 is at negative saturation $-V_{sat}$, which is the input to the integrator A_2 . The equivalent circuit for the operation of the integrator is shown in Fig. 16.22(d). At the beginning of this mode, the output voltage is $-V_{th}$ and the initial voltage on the capacitor is

$$v_C(t=0) = v_1 - v_O = V_{ref} + V_{th}$$

If we redefine the time origin $t = 0$ as the beginning of this mode, the instantaneous voltage across the capacitor is given by

$$V_{ref} - v_O(t) = \frac{1}{C} \int i_C dt + v_C(t=0) = \frac{1}{C} \int \frac{-V_{sat} - V_{ref}}{R} dt + V_{ref} + V_{th}$$

which gives the instantaneous output voltage as

$$v_O(t) = -V_{th} + \frac{V_{sat} + V_{ref}}{RC} t \quad (16.31)$$

At the end of this mode (at $t = t_2$), the output voltage has changed to V_{th} , whose value can be found from Eq. (16.22). That is, $v_O(t = t_2) = V_{th}$. From Eq. (16.31),

$$V_{th} = -V_{th} + \frac{V_{sat} + V_{ref}}{RC} t_2$$

which gives the duration for mode 2 as

$$t_2 = \frac{2RCV_{th}}{V_{sat} + V_{ref}} \quad (16.32)$$

The period of the sawtooth wave can be found from Eqs. (16.30) and (16.32):

$$T = t_1 + t_2 = \frac{2RCV_{th}}{V_{sat} - V_{ref}} + \frac{2RCV_{th}}{V_{sat} + V_{ref}} = \frac{4RCV_{th}V_{sat}}{V_{sat}^2 - V_{ref}^2} \quad (16.33)$$

which gives the frequency of oscillation as

$$f_o = \frac{V_{sat}^2 - V_{ref}^2}{4RCV_{th}V_{sat}} \quad (16.34)$$

Duty cycle k , which is defined as the ratio of t_1 to T , can be determined from Eqs. (16.30) and (16.33) as follows:

$$\begin{aligned} k = \frac{t_1}{T} &= \frac{2RCV_{th}}{V_{sat} - V_{ref}} \times \frac{V_{sat}^2 - V_{ref}^2}{4RCV_{th}V_{sat}} = \frac{V_{sat} + V_{ref}}{2V_{sat}} \\ &= \frac{1}{2} \left[1 + \frac{V_{ref}}{V_{sat}} \right] \end{aligned} \quad (16.35)$$

► **NOTE:** This circuit allows a designer more control over the shape of the output waveform because k , T , and V_{th} can be varied.

EXAMPLE 16.5

D

Designing a sawtooth-wave generator Design the sawtooth-wave generator shown in Fig. 16.22(a) so that $f_o = 4$ kHz, $V_{th} = 4$ V, and the circuit has a duty cycle of $k = 0.25$. Assume $V_{sat} = |-V_{sat}| = 14$ V.

SOLUTION

The steps used to design the sawtooth-wave generator are as follows.

trigger is the capacitor voltage; the output of the Schmitt trigger has two threshold voltage switching levels V_L and V_H , which control the closing and opening of the current switch. Thus, depending on the capacitor voltage $v_C(t)$, the current switch connects the capacitor either to the top current source for charging or to the bottom current source for discharging. The waveform of the capacitor voltage is shown in Fig. 16.23(b); it has two modes, charging and discharging.

Charging Mode

During charging mode, the capacitor is charged by the top current source I_Q from the lower threshold voltage V_L to the upper trigger level V_H . The time required to charge the capacitor from V_L to V_H is given by

$$\Delta t_1 = \frac{C_1}{I_Q} \Delta v_C = \frac{C_1}{I_Q} (V_H - V_L) \quad (16.38)$$

Discharging Mode

The discharging mode begins when the capacitor is charged to the upper trigger level V_H . At this point the current switch disconnects the top current source from C_1 and connects the bottom current source to C_1 . The capacitor is then discharged by the bottom current source down to the lower trigger level V_L . The time required to discharge the capacitor from V_H to V_L is given by

$$\Delta t_2 = -\frac{C_1}{I_Q} \Delta v_C = -\frac{C_1}{I_Q} (V_L - V_H) = \frac{C_1}{I_Q} (V_H - V_L) \quad (16.39)$$

As long as the charging and discharging currents are maintained at the same magnitude of I_Q , $\Delta t_1 = \Delta t_2$. The period of oscillation T is given by

$$T = \Delta t_1 + \Delta t_2 = \frac{2C_1(V_H - V_L)}{I_Q} \quad (16.40)$$

which gives the frequency of oscillation f_o as

$$f_o = \frac{1}{T} = \frac{I_Q}{2C_1(V_H - V_L)} \quad (16.41)$$

Let us assume that the voltage-controlled current sources have a linear voltage-to-current transfer relationship. That is,

$$I_Q = G_m(v_{CN} + V_{CO}) \quad (16.42)$$

where G_m = transconductance of the current source, in A/V

v_{CN} = applied control voltage, in V

V_{CO} = constant voltage

Therefore, the oscillation frequency will be a linear function of the control voltage v_{CN} . That is,

$$f_o = \frac{I_Q}{2C_1(V_H - V_L)} = \frac{G_m(v_{CN} + V_{CO})}{2C_1(V_H - V_L)} \quad (16.43)$$

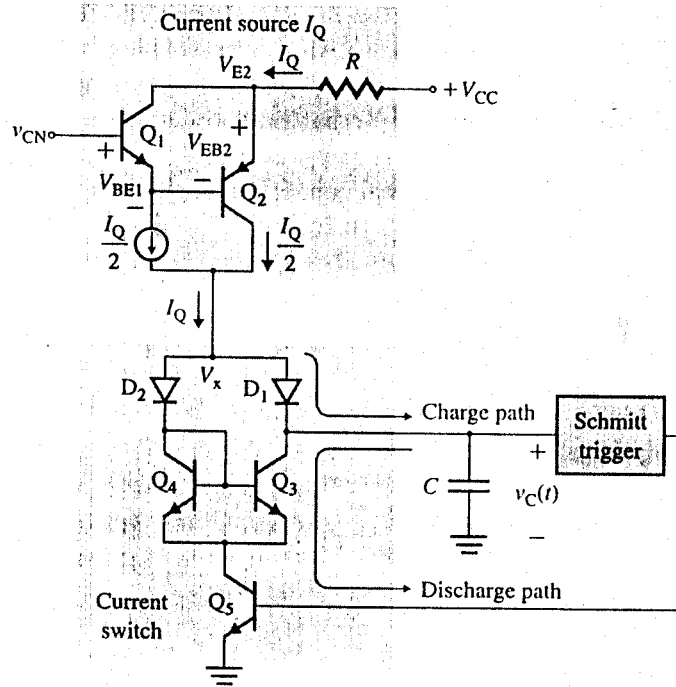
which gives the voltage-to-frequency transfer coefficient K_{vf} as

$$K_{vf} = \frac{df_o}{dv_{CN}} = \frac{G_m}{2C_1(V_H - V_L)} \quad (16.44)$$

Circuit Implementation

A circuit implementation for the charging and discharging of the capacitor is shown in Fig. 16.24. It can be divided into two parts: a voltage-controlled current source and a current switch.

FIGURE 16.24
Circuit implementation



Voltage-Controlled Current Source The voltage-controlled current source consists of an *nnp* transistor Q_1 and a *pnnp* transistor Q_2 . The voltage at the emitter of Q_2 is given by

$$V_{E2} = v_{CN} - V_{BE1} + V_{EB2}$$

which gives the current source I_Q flowing through R as

$$I_Q = \frac{V_{CC} - V_{E2}}{R} = \frac{V_{CC} - v_{CN} + V_{BE1} - V_{EB2}}{R} \quad (16.45)$$

Since V_{BE1} (for an *nnp* transistor) $\approx V_{EB2}$ (for a *pnnp* transistor) within the range from 10 to 50 mV, I_Q in Eq. (16.45) can be approximated by

$$I_Q \approx \frac{V_{CC} - v_{CN}}{R} \quad (16.46)$$

which gives a linear relationship between the current source I_Q and the control voltage v_{CN} .

Current Switch The current switch consists of diodes D_1 and D_2 and transistors Q_3 , Q_4 , and Q_5 . Transistor Q_5 is controlled by the Schmitt trigger and is operated as an on or off switch. When Q_5 is off, capacitor C is charged by the current source I_Q via diode D_1 . Diode D_2 and transistors Q_3 and Q_4 are off. When Q_5 is turned on (in saturation) by the Schmitt trigger, D_2 , Q_3 , and Q_4 are also turned on. As a result, the current source I_Q flows through D_2 and Q_4 instead of via diode D_1 . The voltage at the anode of diode D_2 becomes

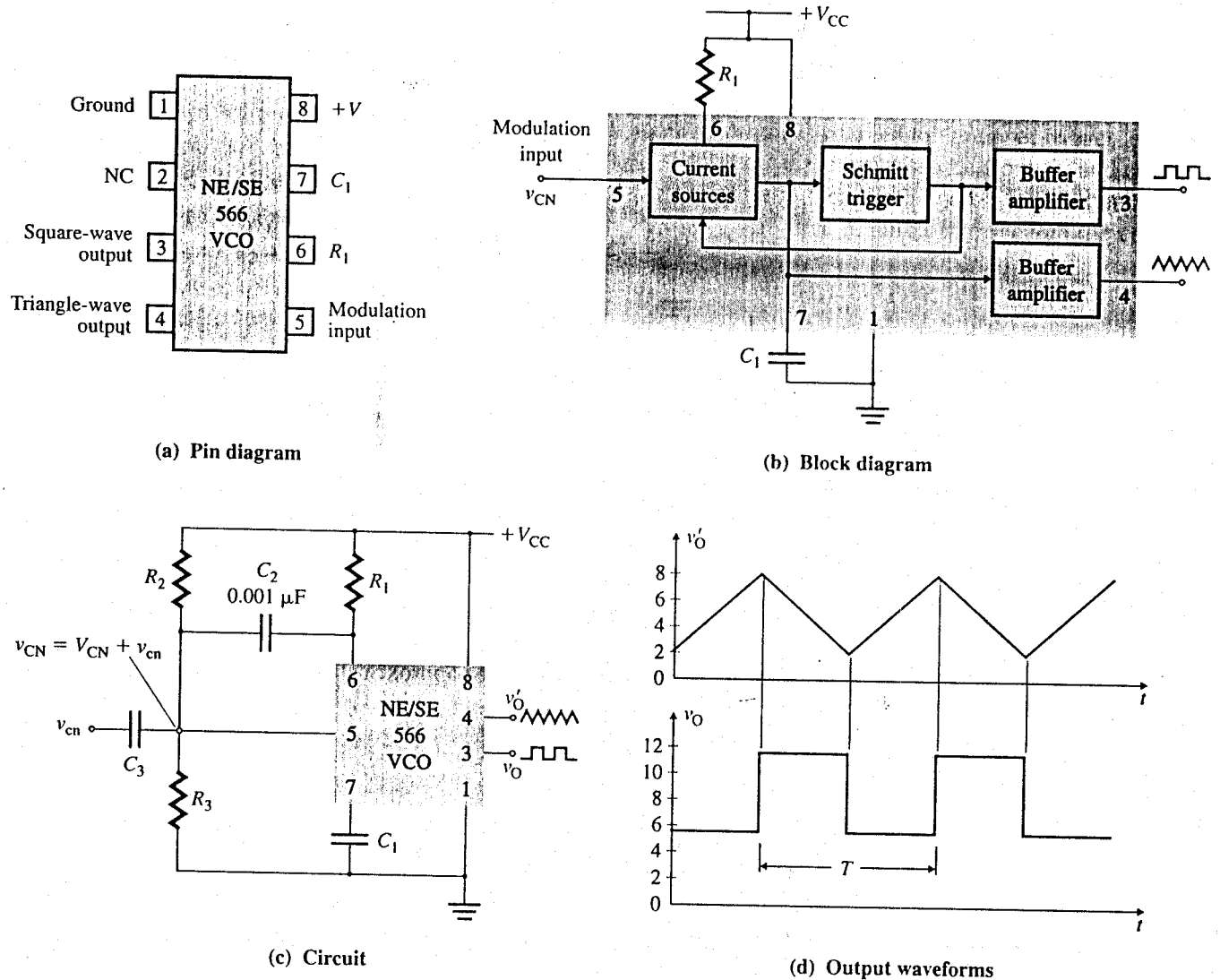
$$V_x = V_{D2(\text{anode})} = V_{D2} + V_{BE4} + V_{CE5(\text{sat})} = 0.6 + 0.6 + 0.2 = 1.4 \text{ V}$$

However, the voltage at the cathode of diode D_1 is the capacitor voltage $v_C(t)$, which will be larger than 1.4 V. Thus, diode D_1 will be reverse-biased (that is, off). Capacitor C will discharge through Q_3 at a rate of I_Q . The current through Q_3 is equal to the current through Q_4 . Thus, transistor Q_5 will carry a current of $2I_Q$.

The NE/SE-566 VCO

A typical example of a VCO integrated circuit is the NE/SE-566 VCO, whose pin diagram is shown in Fig. 16.25(a) and whose internal block diagram is shown in Fig. 16.25(b). This VCO produces simultaneous square-wave and triangular-wave outputs at frequencies of up to 1 MHz. Both outputs are buffered so that the output impedance of each is $50\ \Omega$. The typical amplitude of the square wave is 5.4 V pp (peak to peak), and that of the triangular wave is 2.4 V pp. A typical connection diagram is shown in Fig. 16.25(c), and the typical outputs are shown in Fig. 16.25(d).

FIGURE 16.25 Voltage-controlled oscillator NE/SE-566 (Courtesy of Philips Semiconductors)



The output frequency is determined by an external resistor R_1 , capacitor C_1 , and the voltage v_{CN} applied to control terminal 5. The nominal dc value V_{CN} of v_{CN} is set by the voltage divider formed by R_2 and R_3 and must be in the range of

$$V_{CN} = \frac{R_3}{R_2 + R_3} V_{CC} \quad (16.47)$$

where V_{CC} is the dc supply voltage. V_{CN} must satisfy the following constraint:

$$\frac{3}{4} V_{CC} \leq V_{CN} \leq V_{CC} \quad (16.48)$$

The modulating signal v_{cn} is ac-coupled with capacitor C_3 , and its value must be < 3 V pp. Since v_{cn} is superimposed on V_{CN} , the control voltage v_{CN} is the sum of V_{CN} and v_{cn} ; that is, $v_{CN} = V_{CN} + v_{cn}$. If we substitute $I_Q = (V_{CC} - v_{CN})/R_1$ in Eq. (16.41), the frequency of the output waveforms can be found approximately from

$$f_o = \frac{V_{CC} - v_{CN}}{2R_1C_1(V_H - V_L)} \quad (16.49)$$

which, if we assume $V_H - V_L = V_{CC}/4$, can be approximated by

$$f_o \approx \frac{2(V_{CC} - v_{CN})}{R_1C_1V_{CC}} \quad (16.49)$$

where R_1 should be in the range of $2 \text{ k}\Omega < R_1 < 20 \text{ k}\Omega$. The frequency can be varied over a 10-to-1 range by choosing R_1 between $2 \text{ k}\Omega$ and $20 \text{ k}\Omega$ for a fixed v_{CN} and constant C_1 or by choosing the control voltage v_{CN} for a constant RC product. A small capacitor of $C_2 = 0.001 \text{ }\mu\text{F}$ should be connected between pins 5 and 6 to eliminate possible oscillations in the internal current control source.

EXAMPLE 16.6**D****Designing a voltage-controlled oscillator (VCO)**

- (a) Design a VCO as in Fig. 16.25(c) that has a nominal frequency of $f_o = 20 \text{ kHz}$. Assume $V_{CC} = 12 \text{ V}$.
 (b) Calculate the modulation in the output frequencies if v_{CN} is varied by $\pm 10\%$ because of the modulating signal v_{cn} .

SOLUTION

- (a) The steps used to design the VCO are as follows.

Step 1. Find the limiting values of V_{CN} . From Eq. (16.48), $9 \text{ V} \leq V_{CN} \leq 12 \text{ V}$.

Step 2. Choose a suitable value of C_1 : Let $C_1 = 0.001 \text{ }\mu\text{F}$.

Step 3. Choose a value of R_1 between $2 \text{ k}\Omega$ and $20 \text{ k}\Omega$: Let $R_1 = 10 \text{ k}\Omega$.

Step 4. Find the value of V_{CN} . From Eq. (16.49), V_{CN} is given by

$$\begin{aligned} V_{CN} &= V_{CC} \left(1 - \frac{R_1 C_1 f_o}{2} \right) \\ &= 12 \left(1 - \frac{10 \text{ k}\Omega \times 0.001 \text{ }\mu\text{F} \times 20 \text{ kHz}}{2} \right) = 12 \times 0.9 = 10.8 \text{ V} \end{aligned} \quad (16.50)$$

which falls within the range specified in step 1. If the calculated value falls outside of the specified range, choose a different value for R_1 and/or C_1 and recalculate V_{CN} .

Step 5. Find the values of R_2 and R_3 . From Eq. (16.47),

$$\begin{aligned} 1 + \frac{R_2}{R_3} &= \frac{V_{CC}}{V_{CN}} \\ &= 12/10.8 = 1.11 \end{aligned} \quad (16.51)$$

so $R_2/R_3 = 1.11 - 1 = 0.11$. Let $R_3 = 100 \text{ k}\Omega$; then

$$R_2 = 0.11 \times R_3 = 11 \text{ k}\Omega$$

- (b) For a 10% increase in v_{CN} ,

$$v_{CN} = V_{CN} + v_{cn} = 1.1 \times V_{CN} = 1.1 \times 10.8 = 11.88 \text{ V}$$

The corresponding value of output frequency can be calculated from Eq. (16.49):

$$f_{o1} \approx \frac{2 \times (12 - 11.88)}{10 \text{ k}\Omega \times 0.001 \text{ }\mu\text{F} \times 12} = 2 \text{ kHz}$$

For a 10% decrease in v_{CN} ,

$$v_{CN} = V_{CN} - v_{cn} = 0.9 \times V_C = 0.9 \times 10.8 = 9.72 \text{ V}$$

The output frequency is

$$f_{o2} \approx \frac{2 \times (12 - 9.72)}{10 \text{ k}\Omega \times 0.001 \text{ }\mu\text{F} \times 12} = 38 \text{ kHz}$$

Thus, the change in the output frequency is

$$\Delta f_o = f_{o2} - f_{o1} = 38 \text{ k} - 2 \text{ k} = 36 \text{ kHz}$$

Using Eq. (16.49), we can find the V/F transfer coefficient K_{vf} :

$$\begin{aligned} K_{vf} &= \frac{df_o}{dv_{CN}} = -\frac{2}{R_1 C_1 V_{CC}} \\ &= -\frac{2}{10 \text{ k}\Omega \times 0.001 \text{ }\mu\text{F} \times 12} = -16.67 \text{ kHz/V} \end{aligned} \quad (16.52)$$

Thus, for $\Delta v_{CN} = 2v_{CN} = -2 \times 0.1 \times 10.8 = -2.16 \text{ V}$,

$$\Delta f_o = f_{o2} - f_{o1} = K_{vf} \Delta v_{CN} = -16.67 \text{ kHz/V} \times (-2.16 \text{ V}) = 36.01 \text{ kHz}$$

which is the same as the value obtained by calculating individual frequencies.

- **NOTE:** If the modulating signal is a sine wave so that $v_{cn} = V_m \sin \omega t$, then the control voltage becomes $v_{CN} = V_{CN} + v_m \sin \omega t$. During the positive half-cycle of the modulating signal, the control voltage will increase and the frequency f_o of the output voltage will decrease. However, during the negative half-cycle of the modulating signal, the control voltage will decrease and the frequency f_o of the output voltage will increase.

KEY POINTS OF SECTION 16.8

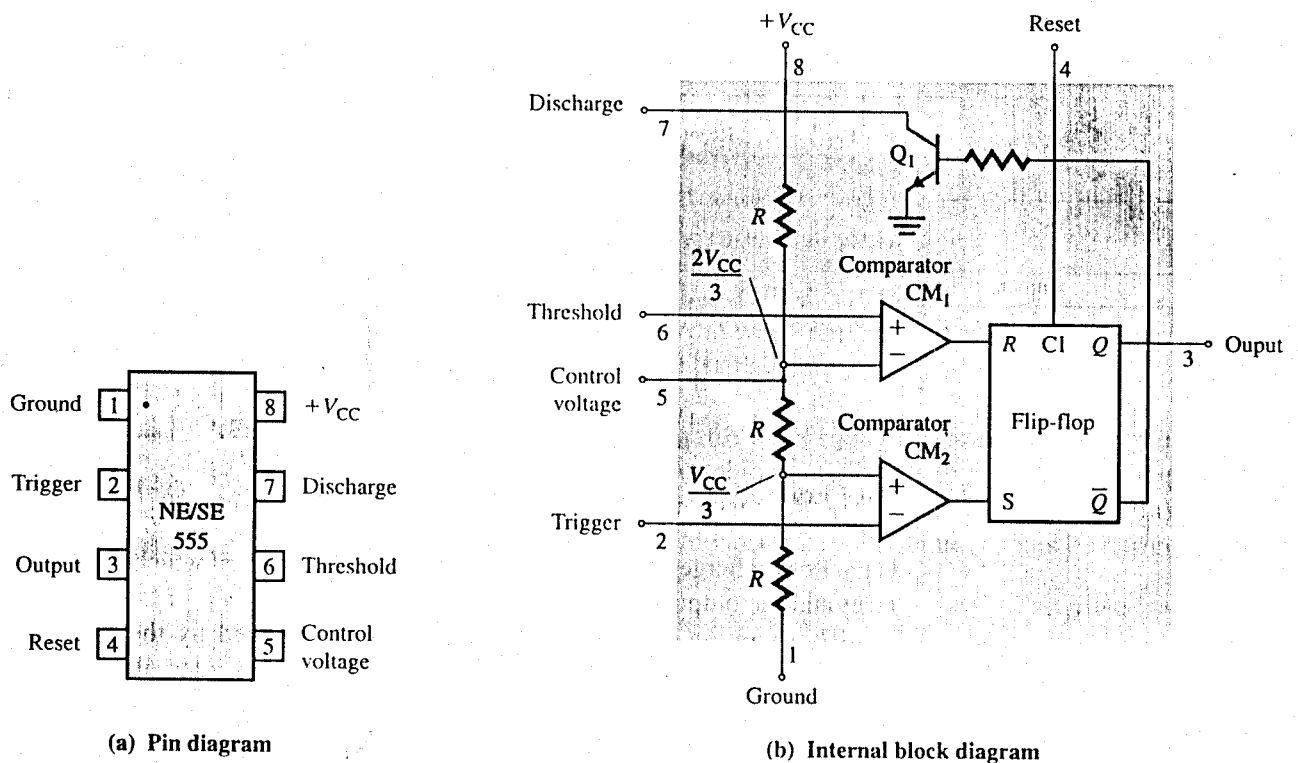
- A *voltage-controlled oscillator (VCO)* is an oscillator circuit in which the oscillation frequency is controlled by an externally applied voltage.
- In order to convert a voltage to frequency, a capacitor is normally charged and then discharged at a constant current whose value depends on an externally applied voltage. The output of a Schmitt trigger controls the charging and discharging time of the capacitor.
- The NE/SE-566 VCO can produce simultaneous square-wave and triangular-wave outputs at frequencies of up to 1 MHz. The output frequency is determined by an external resistor R_1 , capacitor C_1 , and the voltage v_{CN} applied to control terminal 5.

16.9 ► The 555 Timer

The 555 timer, introduced by Signetics Corporation in early 1970, is one of the most versatile integrated circuits. The 555 is a monolithic timing circuit that can produce highly accurate and highly stable delays or oscillation. It is used in many applications, such as monostable and astable multivibrators, digital logic probes, analog frequency meters, tachometers, infrared transmitters, and burglar and toxic gas alarms. Several versions of the 555 timer are available from various manufacturers. In addition to looking briefly at its internal structure, we will consider two common applications of the 555 timer: monostable multivibrator and astable multivibrator.

Functional Block Diagram

The pin diagram of a 555 timer is shown in Fig. 16.26(a); its functional block diagram is shown in Fig. 16.26(b). The timer consists of two comparators CM_1 and CM_2 , an RS flip-flop, a discharge transistor Q_1 , and a resistive voltage divider string. The voltage divider

FIGURE 16.26 Functional block diagram of 555 timer (Courtesy of Philips Semiconductors)

sets the voltage at the inverting terminal of CM_1 to $2V_{CC}/3$ and the voltage at the noninverting terminal of CM_2 to $V_{CC}/3$.

The reset, threshold, and trigger inputs control the state of the flip-flop. If the reset input is low, the Q output of the flip-flop is low and $\bar{Q}$ is high. With $\bar{Q}$ high, current flows through the base of transistor Q_1 , and the transistor is switched on (in saturation). This generally provides a path for an external capacitor to discharge its voltage.

The reset input has the highest priority in setting the state of the flip-flop. Thus, Q is low if the reset input is low, regardless of the inputs to the comparators. If the reset is not in use, then it is connected to the positive dc supply V_{CC} so that it does not affect the state of the flip-flop.

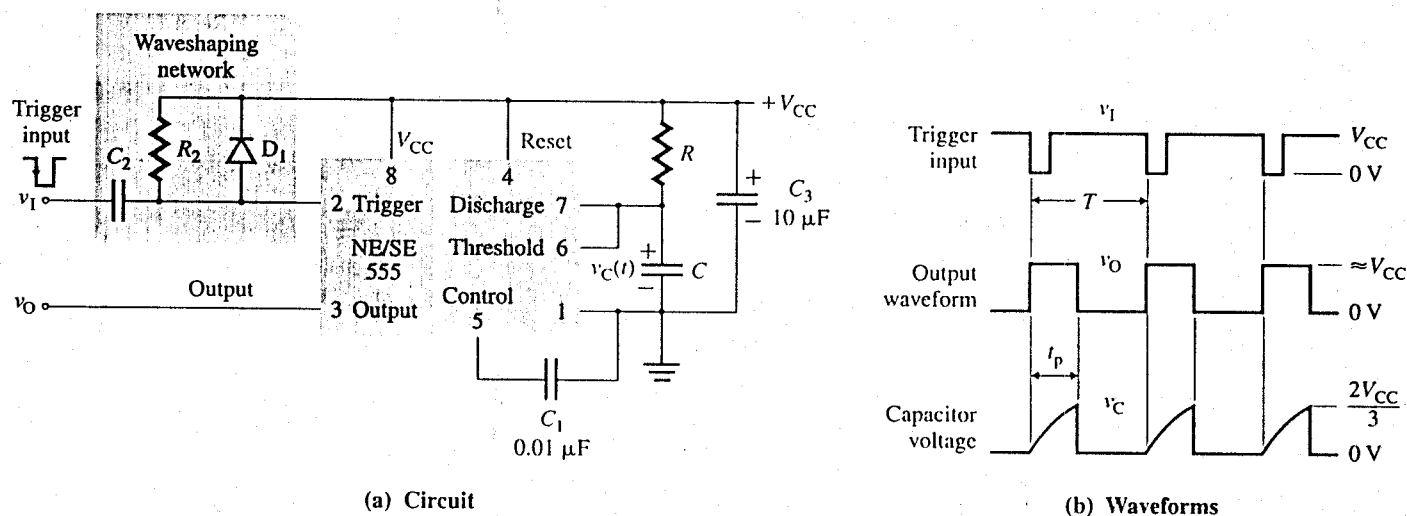
If the trigger input becomes lower than the voltage at the noninverting input of CM_2 (that is, $<V_{CC}/3$), the output of CM_2 (i.e., the S input to the flip-flop) will be high. As a result, the Q output of the flip-flop will be set to high. Thus, $\bar{Q}$ will be low, and the discharge transistor Q_1 will be off.

If the threshold input becomes higher than the voltage at the inverting input of CM_1 (that is, $>2V_{CC}/3$), the output of CM_1 will be high. As a result, the Q output of the flip-flop will be reset to low. Thus, $\bar{Q}$ will be high, and the discharge transistor Q_1 will be on (in saturation), providing a discharge path.

Monostable Multivibrator

A monostable multivibrator is a *one-shot* pulse-generating circuit. Normally, its output is zero—that is, at logic low level in the stable state. This circuit has only one stable state at output low—hence the name *monostable*. The circuit configuration of the 555 timer for monostable operation is shown in Fig. 16.27(a). The discharge and threshold terminals are connected together. The external pulse v_1 is applied to the trigger terminal through coupling capacitor C_2 .

If the external pulse v_1 is high, the Q output of the flip-flop is low; that is, the output of the timer is low. At the negative edge of the trigger signal, the flip-flop will be set to high. Thus, the output will be switched to high ($\approx V_{CC}$). It will remain high until the

FIGURE 16.27 555 timer connected as a monostable multivibrator

capacitor is charged to the threshold voltage of $2V_{CC}/3$, at which time the flip-flop will be reset and the output will return to zero.

The duration of the output pulse (t_p) is determined by the RC network connected externally to the 555 timer. At the end of the timing interval t_p , the output automatically reverts to its stable state of logic low. The output remains low until another negative-going trigger pulse is applied. Then the cycle repeats. The waveforms for the trigger input voltage $v_1(t)$, output voltage $v_o(t)$, and capacitor voltage $v_C(t)$ are shown in Fig. 16.27(b).

The width of the triggering pulse must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative-going signal and have an amplitude larger than $V_{CC}/3$. The time during which the output remains high is given by

$$t_p = 1.1RC \quad (16.53)$$

where R and C are the external resistance and capacitance, respectively.

It is important to note that once the monostable multivibrator is triggered and the output is in the high state, another trigger pulse will have no effect until after an interval of t_p . That is, the multivibrator cannot be retriggered during the timing interval t_p .

A decoupling capacitor C_3 , typically of $10 \mu\text{F}$, is normally connected between V_{CC} (pin 8) and ground (pin 1) to eliminate unwanted voltage spikes in the output waveform. A wavershaping circuit consisting of R_2 , C_2 , and diode D_1 is often connected between the trigger input (pin 2) and V_{CC} (pin 8) in order to prevent any possible mistripping by positive pulse edges. This circuit is shown in Fig. 16.27(a) within the shaded area. The values of R_2 and C_2 should be selected so that the output pulse width t_p is much larger than the time constant R_2C_2 . This condition is generally met by maintaining the following relationship:

$$t_p = 10R_2C_2 \quad (16.54)$$

EXAMPLE 16.7

Designing a monostable multivibrator Design a monostable multivibrator as in Fig. 16.27(a) so that $t_p = 5 \text{ ms}$. Assume $V_{CC} = 12 \text{ V}$.

SOLUTION

The steps used to design a monostable multivibrator are as follows.

Step 1. Choose a suitable value of C : Let $C = 0.1 \mu\text{F}$.

Step 2. Find the value of R . From Eq. (16.53),

$$R = \frac{t_p}{1.1C} = \frac{5 \text{ ms}}{1.1 \times 0.1 \mu\text{F}} = 45.5 \text{ k}\Omega \quad (\text{use a } 50\text{-k}\Omega \text{ potentiometer})$$

Step 3. Choose a suitable value of C_2 : Let $C_2 = 0.01 \mu\text{F}$.

Step 4. Find the value of R_2 . From Eq. (16.54),

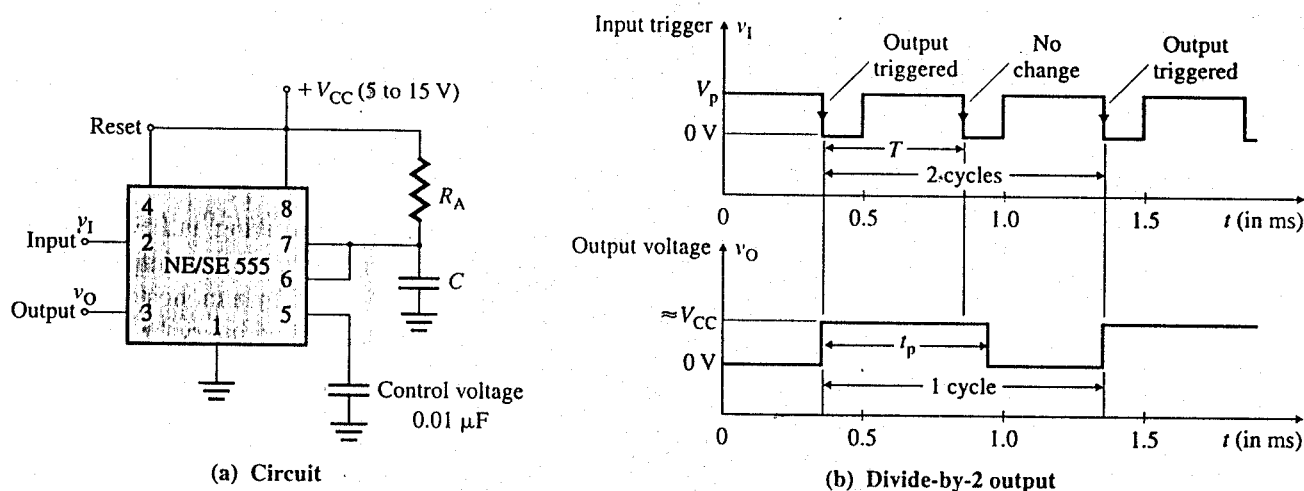
$$R_2 = \frac{t_p}{10C_2} = \frac{5 \text{ ms}}{10 \times 0.01 \mu\text{F}} = 50 \text{ k}\Omega$$

Applications of Monostable Multivibrators

Monostable multivibrators can be used in many applications such as frequency dividers, missing-pulse detectors, and pulse stretchers.

Frequency Divider If the frequency of the input signal is known, adjusting the length of the timing cycle t_p will permit a monostable multivibrator to be used as a frequency divider. The circuit configuration for a frequency divider is shown in Fig. 16.28(a). This application makes use of the fact that the monostable multivibrator cannot be retriggered during the timing interval.

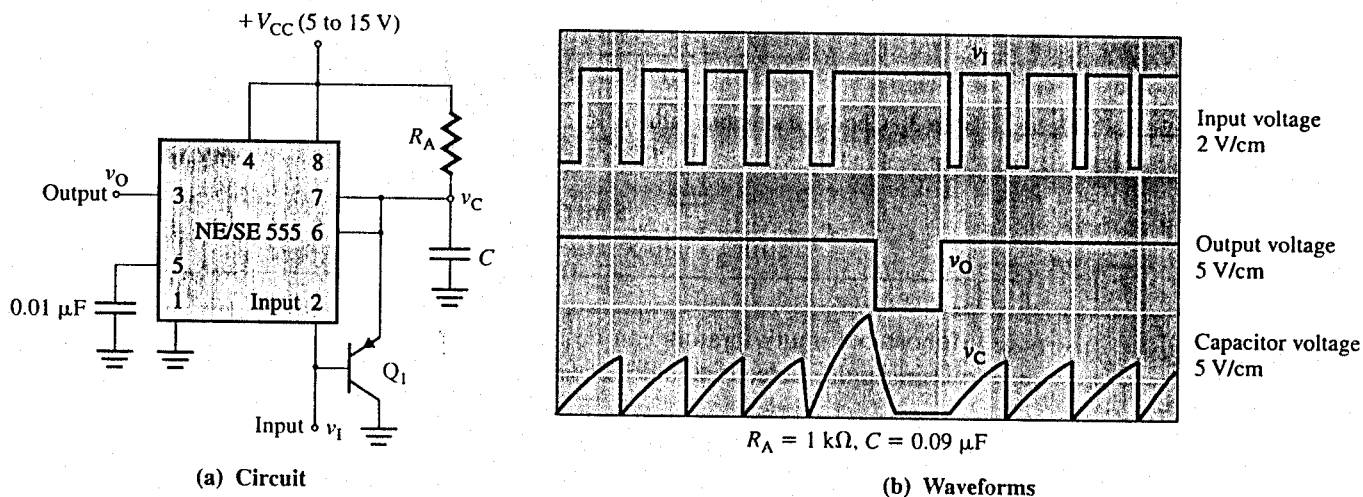
FIGURE 16.28 Monostable multivibrator as a frequency divider



For a monostable multivibrator to be used as a divide-by-2 circuit, the timing interval must be slightly larger (say, by 20%) than the period of the trigger signal T , as shown in Fig. 16.28(b); that is, $t_p = 1.2T$. At the first falling edge, the output is set to high. However, at the second falling edge, the capacitor is still charging and has not yet reached the threshold value of $2V_{CC}/3$. As a result, the second triggering signal has no effect on the output, and the output is set by the alternate trigger pulses.

For a monostable multivibrator to be used as a divide-by-3 circuit, t_p must be slightly larger than twice the period of the trigger signal. Thus, for a divide-by- n circuit, t_p must be slightly larger than $(n-1)T$; that is, $t_p = [0.2 + (n-1)]T$. For example, for a divide-by-2 circuit, if $f_o = 5 \text{ kHz}$ and $T = 1/f_o = 200 \mu\text{s}$, then $t_p = 1.2T = 240 \mu\text{s}$.

Missing-Pulse Detector In some applications, a train of regular pulses is needed for the normal operation of a circuit or system. Any missing pulse may cause malfunction. The configuration of a monostable multivibrator that can detect any missing pulse is shown in Fig. 16.29(a).

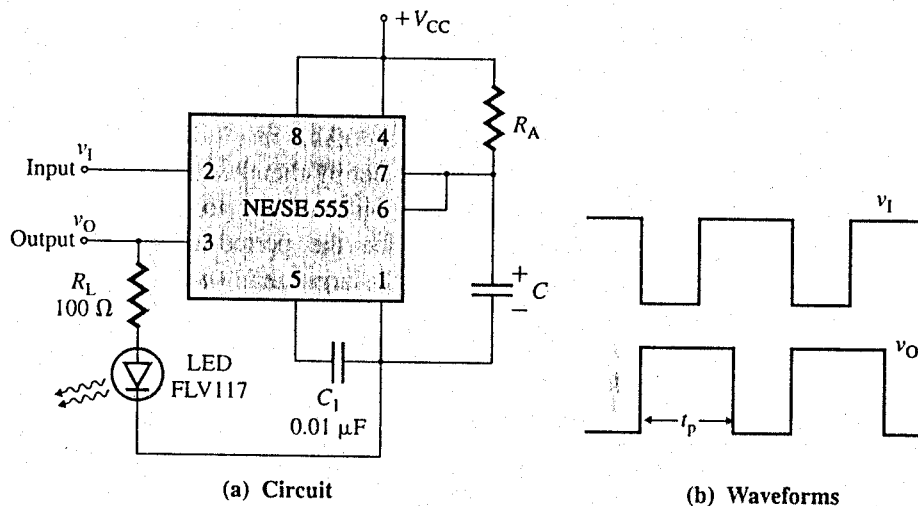
FIGURE 16.29 Monostable multivibrator as a missing-pulse detector

The timing cycle is continuously reset by the input pulse train, but the time duration is not enough to complete the timing cycle. When the trigger pulse becomes low, transistor Q_1 is turned on, and it provides a discharge path for capacitor C . As a result, the capacitor voltage cannot reach the threshold voltage $2V_{CC}/3$. A change in frequency, or a missing pulse, allows completion of the timing cycle so that v_C reaches $2V_{CC}/3$, causing a change in the output level due to the discharge of C through the internal transistor Q_1 in Fig. 16.26(b). The time delay t_p should be slightly longer than the normal time between input pulses. The waveforms are shown in Fig. 16.29(b).

Pulse Widener A narrow pulse is not desirable for driving an LED display, as the flashing of the LED will not be visible to the eyes if the on time is infinitesimally small compared to the off time. A narrow pulse can be widened by a monostable multivibrator. This application is possible because of the fact that the timing interval t_p is longer than the negative pulse width of the trigger input.

The circuit configuration for a pulse widener is shown in Fig. 16.30(a). At the falling trigger edge, the output will be high, and it will remain high until the capacitor voltage reaches $2V_{CC}/3$ after time t_p . The waveforms of the input and output voltages are shown

FIGURE 16.30
Monostable multivibrator
as a pulse widener

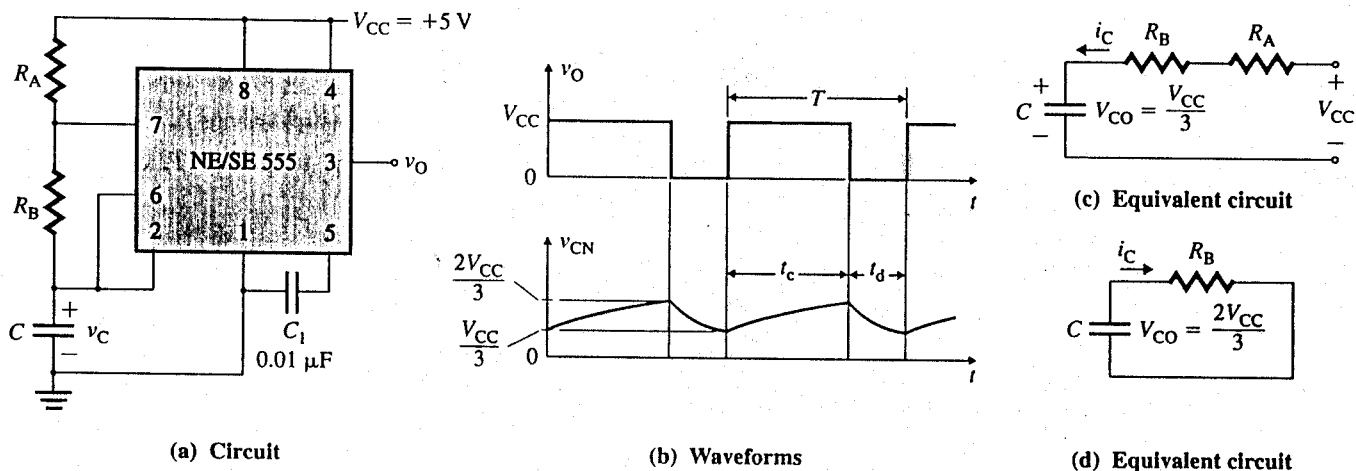


in Fig. 16.30(b). Since the output pulse can be viewed as the stretched version of the narrow input signal, this configuration is also known as a *pulse stretcher*.

Astable Multivibrator

An astable multivibrator is a rectangular-wave-generating circuit. Because this circuit does not require an external trigger to change the state of the output, it is often called a *free-running multivibrator*. A 555 timer connected as an astable multivibrator is shown in Fig. 16.31(a). The duration of the high or low output is determined by resistors R_A and R_B and capacitor C . When the output is high, capacitor C starts charging toward V_{CC} through R_A and R_B . As soon as the capacitor voltage equals $2V_{CC}/3$, the output switches to low and capacitor C discharges through R_B and the internal circuit of the timer. When the capacitor voltage equals $V_{CC}/3$, the output goes high and the capacitor charges through R_A and R_B . Then the cycle repeats. The waveforms for the output voltage and the voltage across the capacitor are shown in Fig. 16.31(b).

FIGURE 16.31 555 timer connected as an astable multivibrator



The capacitor is periodically charged and discharged between $2V_{CC}/3$ and $V_{CC}/3$. Assuming the initial capacitor voltage is $V_{CO} = V_{CC}/3$, the equivalent circuit during the charging period is as shown in Fig. 16.31(c). The charging current $i_C(t)$ and the capacitor voltage $v_C(t)$ are given by

$$i_C(t) = \frac{2V_{CC}}{3(R_A + R_B)} e^{-t/(R_A + R_B)C} \quad (16.55)$$

$$v_C(t) = V_{CC} - \frac{2V_{CC}}{3} e^{-t/(R_A + R_B)C} \quad (16.56)$$

At $t = t_c$, $v_C(t = t_c) = 2V_{CC}/3$, and Eq. (16.56) yields

$$\frac{2V_{CC}}{3} = V_{CC} - \frac{2V_{CC}}{3} e^{-t_c/(R_A + R_B)C}$$

which gives the charging time t_c as

$$t_c = C(R_A + R_B) \ln(2) = 0.69C(R_A + R_B) \quad (16.57)$$

During time t_d , capacitor C discharges from $2V_{CC}/3$ to $V_{CC}/3$ through R_B . Assuming the initial capacitor voltage is $V_{CO} = 2V_{CC}/3$, the equivalent circuit during the discharg-

ing period is as shown in Fig. 16.31(d). The current $i_C(t)$ and capacitor voltage $v_C(t)$ are given by

$$i_C(t) = \frac{2V_{CC}}{3R_B} e^{-t/R_B C} \quad (16.58)$$

$$v_C(t) = \frac{2V_{CC}}{3} e^{-t/R_B C} \quad (16.59)$$

At $t = t_d$, $v_C(t = t_d) = V_{CC}/3$, and Eq. (16.59) yields

$$\frac{V_{CC}}{3} = \frac{2V_{CC}}{3} e^{-t_d/R_B C}$$

which gives the discharging time t_d as

$$t_d = CR_B \ln(2) = 0.69CR_B \quad (16.60)$$

Thus, the period of the output waveform is given by

$$T = t_c + t_d = 0.69C(R_A + R_B) + 0.69CR_B = 0.69C(R_A + 2R_B) \quad (16.61)$$

and the frequency of the output voltage is therefore given by

$$f_o = \frac{1}{T} = \frac{1}{0.69C(R_A + 2R_B)} = \frac{1.45}{C(R_A + 2R_B)} \quad (16.62)$$

Duty cycle k , which is the ratio of charging time t_c to period T , can be found from Eqs. (16.57) and (16.61):

$$k = \frac{t_c}{T} = \frac{R_A + R_B}{R_A + 2R_B} \quad (16.63)$$

Thus, the duty cycle k can be set by selecting R_A or R_B .

EXAMPLE 16.8

D

SOLUTION

Designing an astable multivibrator Design an astable multivibrator as in Fig. 16.31(a) so that $k = 75\%$ and $f_o = 2.5$ kHz. Assume $V_{CC} = 12$ V.

$k = 75\% = 0.75$, and $T = 1/f_o = 1/2.5$ kHz = 400 μ s. The steps used to design an astable multivibrator are as follows.

Step 1. Find the charging time t_c and the discharging time t_d :

$$t_c = kT = 0.75 \times 400 \mu\text{s} = 300 \mu\text{s} \quad (16.64)$$

$$t_d = (1 - k)T = (1 - 0.75) \times 400 \mu\text{s} = 100 \mu\text{s} \quad (16.65)$$

Step 2. Choose a suitable value of C : Let $C = 0.1$ μ F.

Step 3. Find the value of R_B . From Eq. (16.60),

$$R_B = \frac{t_d}{0.69C} = \frac{100 \mu\text{s}}{0.69 \times 0.1 \mu\text{F}} = 1449 \Omega \quad (16.66)$$

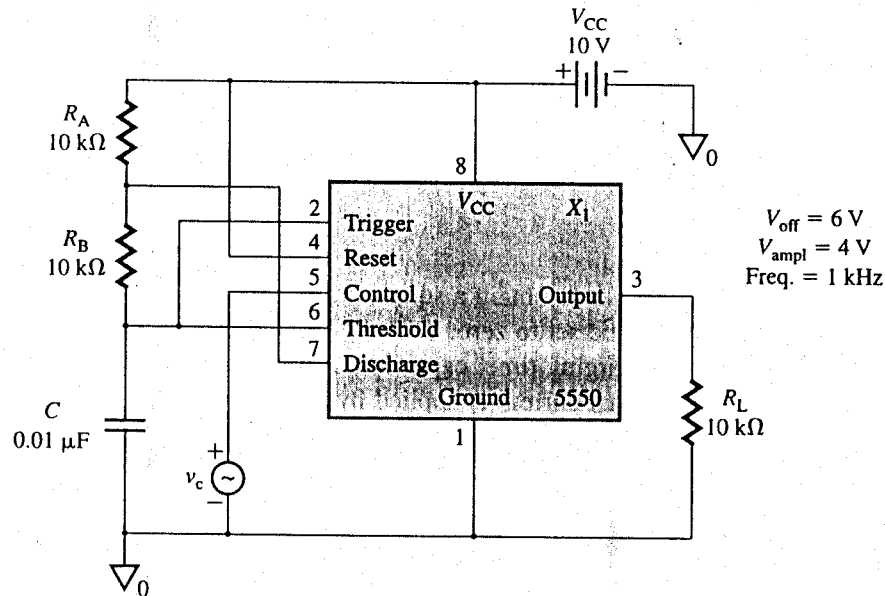
Step 4. Find the value of R_A . From Eq. (16.57),

$$R_A = \frac{t_c}{0.69C} - R_B = \frac{300 \mu\text{s}}{0.69 \times 0.1 \mu\text{F}} - 1449 = 2899 \Omega \quad (16.67)$$

EXAMPLE 16.9

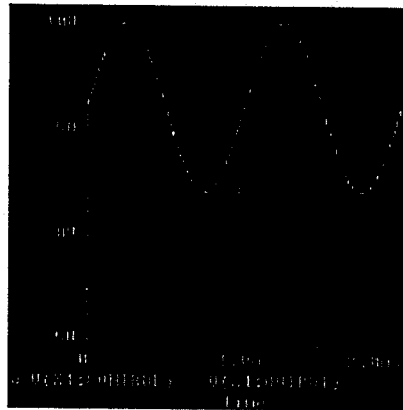
PSpice/SPICE simulation of an astable multivibrator An astable multivibrator can be used as a voltage-controlled oscillator (VCO) if an external control voltage is applied to terminal 5. This arrangement is shown in Fig. 16.32 for $v_{CN} = 6 + 4 \sin(2000\pi t)$. Use PSpice/SPICE to plot the output voltage $v_O(t)$ from 0 to 2 ms with an increment of 10 ns.

FIGURE 16.32 Astable multivibrator as a VCO for PSpice simulation

**SOLUTION**

The PSpice plots of the control and output voltages are shown in Fig. 16.33. As expected, the frequency becomes lower—that is, the period becomes larger—as the control voltage increases in magnitude.

FIGURE 16.33 Control and output voltages for Example 16.9



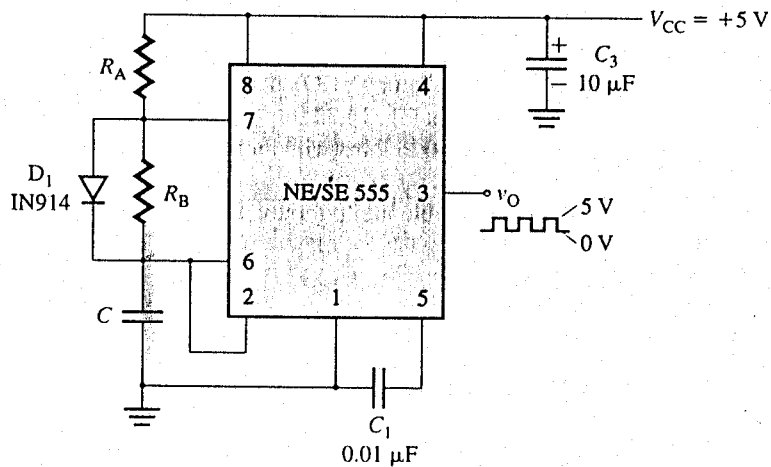
Applications of Astable Multivibrators

As examples of applications of an astable multivibrator, we will consider a square-wave generator, a ramp generator, and an FSK modulator.

Square-Wave Generator The astable multivibrator in Fig. 16.31(a) can be modified to produce a square wave. A diode is connected across resistor R_B , as shown in Fig. 16.34. For a finite value of R_A in Eq. (16.57), $t_c > t_d$, and the duty cycle is $k > 50\%$. However,

FIGURE 16.34

555 timer connected as a square-wave generator



in order to obtain a square wave, the duty cycle k must be 50%. That is, the value of R_A must be set to zero. With $R_A = 0 \Omega$, terminal 7 is connected directly to V_{CC} . During the discharging time, capacitor C discharges through the internal circuit of the timer and an external current is applied by V_{CC} to the same internal path. The current flowing through the internal path may be large enough to damage the timer. This situation can be avoided by connecting a diode across R_B so that R_B is bypassed during the charging time. In that case, Eqs. (16.61) and (16.62) are reduced, respectively, to

$$T = 0.69C(R_A + R_B) \quad \text{for } k = 0.5 \quad (16.68)$$

$$\text{and} \quad f_o = \frac{1}{T} = \frac{1.45}{C(R_A + R_B)} \quad \text{for } k = 0.5 \quad (16.69)$$

EXAMPLE 16.10**D****SOLUTION**

Designing a square-wave generator Design a square-wave generator as in Fig. 16.34 so that $k = 50\%$ and $f_o = 2.5 \text{ kHz}$. Assume $V_{CC} = 12 \text{ V}$.

$k = 50\% = 0.5$, and $T = 1/f_o = 1/2.5 \text{ kHz} = 400 \mu\text{s}$. The steps used to design the square-wave generator are as follows.

Step 1. Find the charging time t_c and the discharging time t_d :

$$\begin{aligned} t_c &= t_d = kT \\ &= 0.5 \times 400 \mu\text{s} = 200 \mu\text{s} \end{aligned} \quad (16.70)$$

Step 2. Choose a suitable value of C : Let $C = 0.1 \mu\text{F}$.

Step 3. Find the value of R_B . From Eq. (16.60),

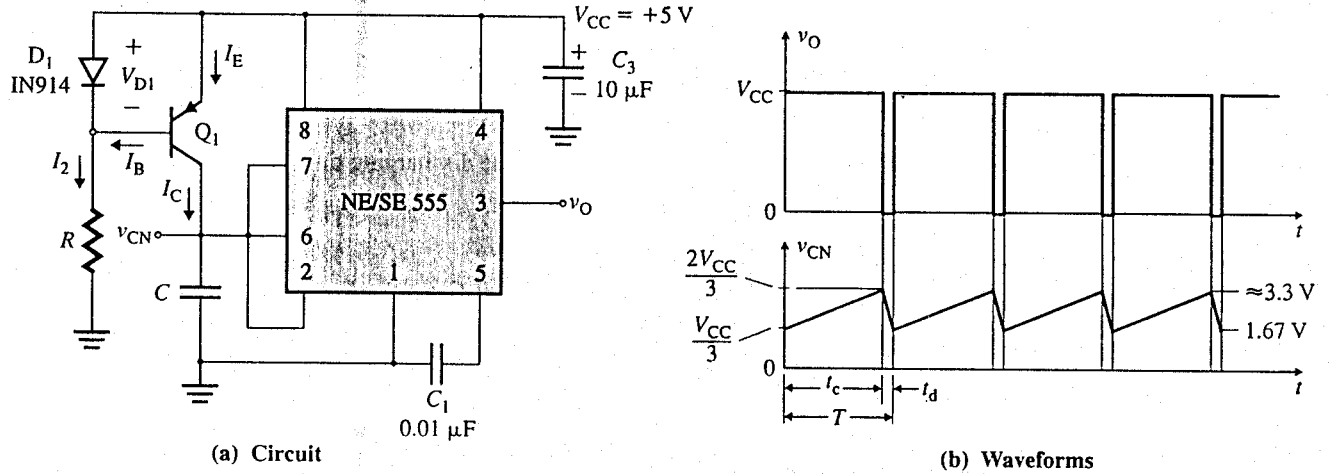
$$\begin{aligned} R_B &= \frac{t_d}{0.69C} \\ &= \frac{200 \mu\text{s}}{0.69 \times 0.1 \mu\text{F}} = 2899 \Omega \end{aligned} \quad (16.71)$$

Step 4. Find the value of R_A . From Eq. (16.69),

$$\begin{aligned} R_A &= \frac{1.45}{Cf_o} - R_B \\ &= \frac{1.45}{0.1 \mu\text{F} \times 2.5 \text{ kHz}} - 2899 = 2901 \Omega \end{aligned} \quad (16.72)$$

Ramp Generator The astable multivibrator in Fig. 16.31(a) can be used as a free-running ramp generator. This is accomplished by charging the capacitor through a constant current source and discharging through the internal circuit of the timer. That is, resistors R_A and R_B are replaced by a current source, as shown in Fig. 16.35(a). The waveforms for the output voltage and the capacitor voltage are shown in Fig. 16.35(b).

FIGURE 16.35 555 timer connected as a ramp generator



The collector current, which is the charging current, is given by

$$I_C = I_E - I_B$$

Assuming that the voltage drop of diode D_1 is approximately equal to the base-emitter voltage V_{BE} of the transistor, the diode current $I_D \approx I_E$. Thus,

$$\begin{aligned} I_C &= I_D - I_B = I_2 \\ &= \frac{V_B}{R} = \frac{V_{CC} - V_{BE}}{R} \end{aligned} \quad (16.73)$$

The capacitor charges from $V_{CC}/3$ to $2V_{CC}/3$ at a constant current of I_C . For a charging time of t_c , the change in the capacitor voltage Δv_C is given by

$$\Delta v_C = \frac{2V_{CC}}{3} - \frac{V_{CC}}{3} = \frac{1}{C} \int_0^{t_c} I_C dt = \frac{1}{C} I_C t_c$$

which gives the charging time t_c as

$$t_c = \frac{CV_{CC}}{3I_C} \quad (16.74)$$

The charging time is related to the duty cycle k and period T by

$$\begin{aligned} kT &= t_c \\ &= \frac{CV_{CC}}{3I_C} \end{aligned} \quad (16.75)$$

Therefore, the free-running frequency of the ramp generator is given by

$$f_o = \frac{1}{T} = \frac{3kI_C}{CV_{CC}} \quad (16.76)$$

$$= \frac{3k(V_{CC} - V_{BE})}{CRV_{CC}} \quad (16.77)$$

If the discharging time t_d of the capacitor is negligible compared to its charging time t_c , then $k \approx 1$ and the free-running frequency becomes

$$f_o = \frac{3(V_{CC} - V_{BE})}{CRV_{CC}} \quad (16.78)$$

EXAMPLE 16.11**D****SOLUTION**

Designing a ramp generator Design a ramp generator using the circuit in Fig. 16.35(a) so that $k = 50\%$ and $f_o = 2.5$ kHz. Assume $V_{CC} = 12$ V, $V_{BE} = 0.7$ V, and a transistor of $\beta_F = 150$.

$k = 50\% = 0.5$, and $T = 1/f_o = 1/2.5$ kHz = 400 μ s. The steps used to design the ramp generator are as follows.

Step 1. Find the charging time t_c and the discharging time t_d :

$$\begin{aligned} t_c &= t_d = kT \\ &= 0.5 \times 400 \mu\text{s} = 200 \mu\text{s} \end{aligned} \quad (16.79)$$

Step 2. Choose a suitable value of C : Let $C = 0.1$ μ F.

Step 3. Find the value of R . From Eq. (16.77),

$$\begin{aligned} R &= \frac{3k(V_{CC} - V_{BE})}{V_{CC}Cf_o} \\ &= \frac{3 \times 0.5 \times (12 - 0.7)}{12 \times 0.1 \mu\text{F} \times 2.5 \text{ kHz}} = 5.65 \text{ k}\Omega \end{aligned} \quad (16.80)$$

Step 4. Find the collector current I_C of the transistor. From Eq. (16.73),

$$I_C = \frac{V_{CC} - V_{BE}}{R} = \frac{12 - 0.7}{5.65 \text{ k}\Omega} = 2 \text{ mA}$$

Step 5. Find the current I_D through the diode:

$$I_D = I_E = I_C + I_B = I_C \frac{1 + \beta_F}{\beta_F} = 2 \text{ mA} \times \frac{1 + 150}{150} \approx 2.01 \text{ mA}.$$

FSK Modulator In computer peripheral and radio (wireless) communication, the binary data or code is transmitted by means of a carrier frequency that shifts between two preset frequencies. This technique for data transmission is called *frequency-shift keying* (FSK). The frequency shift is usually accomplished by driving a VCO with the binary data signal so that the 0 to 1 states (commonly called *space* and *mark*) of the binary data signal produce two frequencies, known as the *space* and *mark frequencies*. For example, when teletypewriter information is transmitted using a modulator/demodulator (*modem*, for short), a 1070-Hz (for mark) and 1270-Hz (for space) pair will represent the original signal, whereas a 2025-Hz (for mark) and 2250-Hz (for space) pair will represent the answer signal.

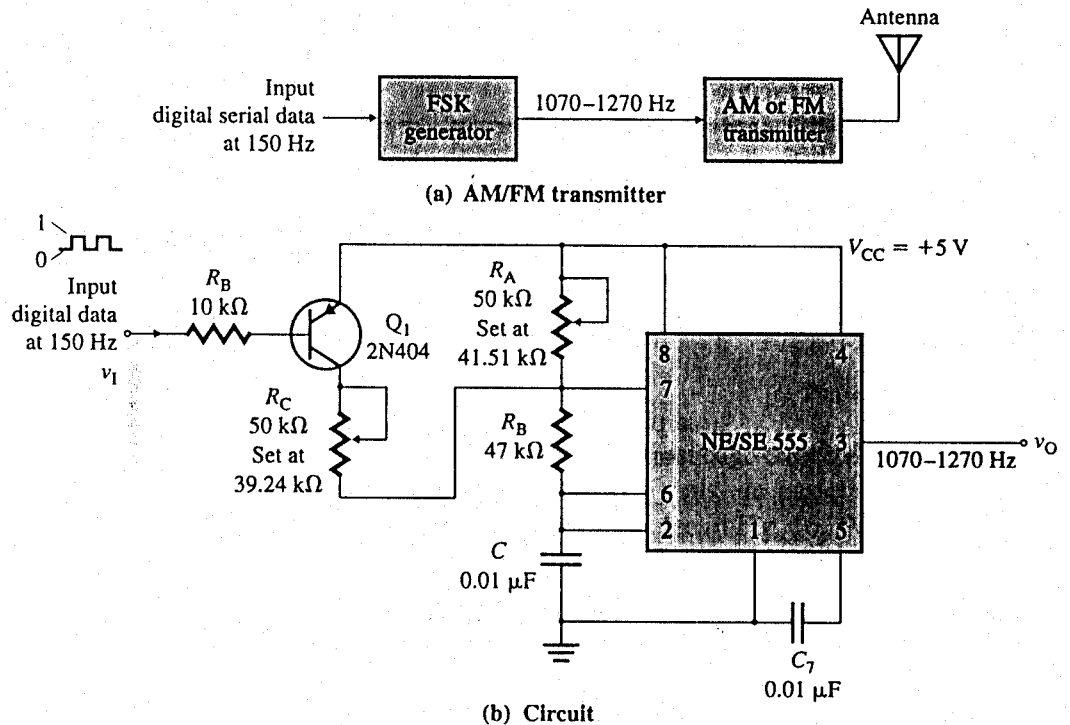
FSK modulators are often used in AM/FM transmitters, as shown in Fig. 16.36(a). The 555 astable multivibrator can be used as an FSK generator; the connection is shown in Fig. 16.36(b). The on or off condition of transistor Q_1 will depend on the input signal. Thus, the output frequency depends on the logic state of the digital input signal. A signal frequency of 150 Hz is commonly used for data transmission.

When the input signal is 1, transistor Q_1 is off and the 555 operates in its normal mode as an astable multivibrator. Thus, the output frequency corresponding to logic 1 can be found from Eq. (16.62) as

$$f_{o(\text{mark})} = \frac{1.45}{C(R_A + 2R_B)}$$

The values for C , R_A , and R_B can be selected so as to give 1070 Hz.

FIGURE 16.36
Astable multivibrator as
an FSK modulator
(Courtesy of Philips
Semiconductors)



When the input signal is 0, transistor Q_1 is turned on (in saturation). As a result, R_C is effectively connected in parallel with R_B . This reduces the charging time of capacitor C and increases the output frequency. Thus, the output frequency corresponding to logic 0 can be found from

$$f_{o(\text{space})} = \frac{1.45}{C(R_A \parallel R_C + 2R_B)}$$

The value for R_C can be selected so as to give 1270 Hz.

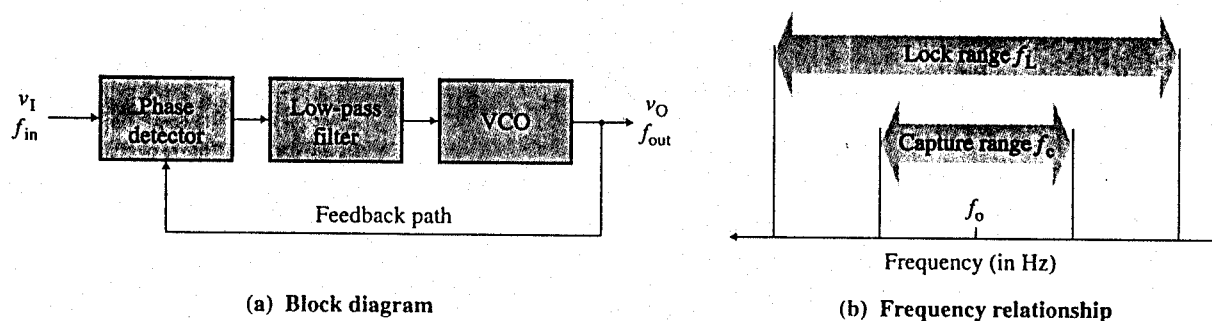
Thus, with properly selected values of C , R_A , R_B , and R_C , the 555 astable multivibrator can produce frequencies of 1070 Hz and 1270 Hz corresponding to 1 and 0, respectively. The difference between the FSK signals of 1270 Hz and 1070 Hz (i.e., 300 Hz) is called the *frequency shift*.

KEY POINTS OF SECTION 16.9

- The 555 timer is one of the most versatile integrated circuits. It is used as a monostable or astable multivibrator in many applications.
- A monostable multivibrator is a *one-shot* pulse-generating circuit. This circuit has only one stable state at output low—hence the name *monostable*. The 555 can be configured as a monostable multivibrator, which can be used as a frequency divider, a missing-pulse detector, or a pulse widener.
- An astable multivibrator is a rectangular-wave-generating circuit. Because it does not require an external trigger to change the state of the output, it is often called a *free-running* multivibrator. The 555 can be configured as an astable multivibrator, which can be used as a square-wave generator, a ramp generator, or an FSK modulator.

16.10 ► Phase-Lock Loops

The phase-lock loop (PLL) is one of the fundamental building blocks of electronic circuits used in such applications as motor-speed controllers, FM stereo decoders, tracking filters, frequency-synthesized transmitters and receivers, and FSK decoders. A block diagram of

FIGURE 16.37 Block diagram of a phase-lock loop

a phase-lock loop is shown in Fig. 16.37(a). The loop consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator (VCO).

The phase detector (or comparator) compares the phase of the input voltage with that of the VCO output voltage and produces a dc or low-frequency voltage proportional to their phase difference. The output of the phase detector, which is called the *error voltage*, is applied to a low-pass filter. The filter removes any high-frequency components and produces a smooth dc voltage. This dc voltage is then applied to the control input of the VCO, whose output frequency is proportional to the dc value. If the frequency of the input voltage shifts slightly, the phase difference between the input signal and the VCO output voltage will begin to increase with time. This will change the control voltage to the VCO in such a way as to bring the VCO frequency back to the same value as the input voltage. The VCO frequency is continuously adjusted until it is equal to the input frequency.

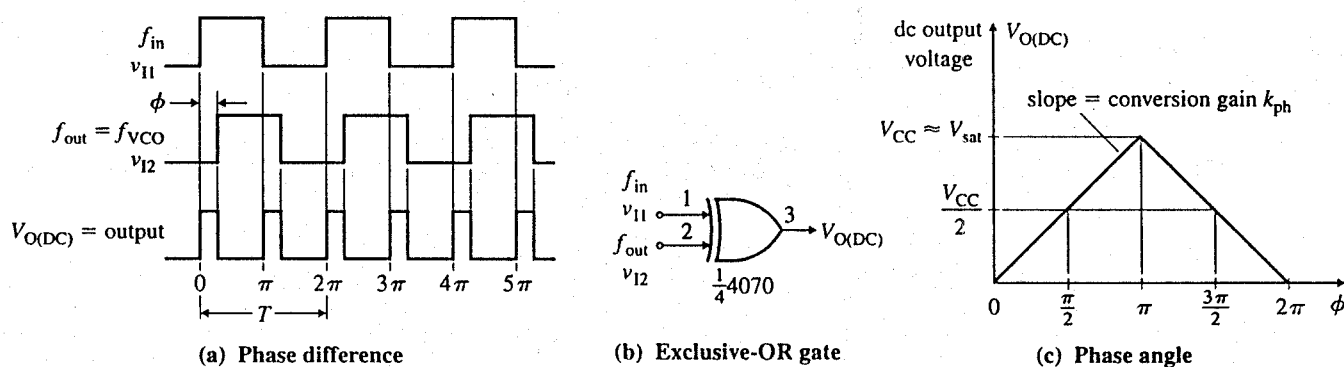
The operation of a PLL involves three modes: a *free-running mode*, a *capture mode*, and a *phase-lock mode*. During the free-running mode, there is no input frequency (or voltage) and the VCO runs at a fixed frequency corresponding to zero applied input voltage. This frequency is called the *center*, or *free-running frequency* f_o . Once an input frequency is applied, the VCO frequency starts to change and the PLL is said to be in the capture mode. The VCO frequency changes continuously to match the input frequency. When the input frequency becomes equal to the output frequency, the PLL is said to be in the phase-lock mode. The feedback loop maintains the lock when the input signal frequency changes.

The center frequency f_o is the free-running frequency of the VCO. The *lock range* f_L is defined as the range of input frequencies around the center frequency for which the loop can maintain lock. The *capture range* f_c is defined as the range of input frequencies around the center frequency for which the loop will become locked from an unlocked condition. The relations among f_o , f_L , and f_c are shown in Fig. 16.37(b).

Phase Detector

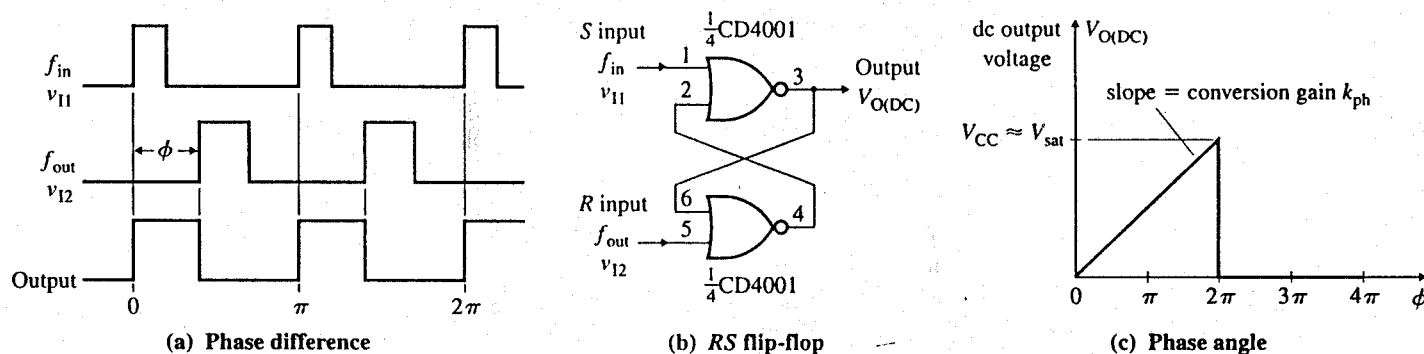
A phase detector takes two input voltages and produces a dc voltage proportional to their phase difference. To understand the principle of operation, consider two voltages v_{I1} and v_{I2} , as shown in Fig. 16.38(a), with a phase difference of ϕ . An output voltage is obtained when they differ in phase—that is, when only one input is high. A phase detector can be implemented using either an exclusive-OR gate, as shown in Fig. 16.38(b), or an analog multiplier [3]. Integrating the output voltage will give an average output voltage, which will be a linear function of the phase difference ϕ , as shown in Fig. 16.38(c). The average output voltage $V_{O(DC)}$ can be expressed as

$$V_{O(DC)} = \begin{cases} \frac{V_{CC}}{\pi} \phi & \text{for } 0 \leq \phi \leq \pi \\ \frac{V_{CC}}{\pi} (2\pi - \phi) & \text{for } \pi \leq \phi \leq 2\pi \end{cases} \quad (16.81)$$

FIGURE 16.38 Phase detector

The phase difference can also be detected by using an edge-triggered RS flip-flop. Two input signals are shown in Fig. 16.39(a). If these signals are passed through an edge-triggered RS flip-flop, the output voltage will be as shown in Fig. 16.39(b). Integrating the output voltage will give an average output voltage, as shown in Fig. 16.39(c). The average output voltage $V_{O(DC)}$ is given by

$$V_{O(DC)} = \frac{V_{CC}}{2\pi} \phi \quad \text{for } 0 \leq \phi \leq 2\pi \quad (16.82)$$

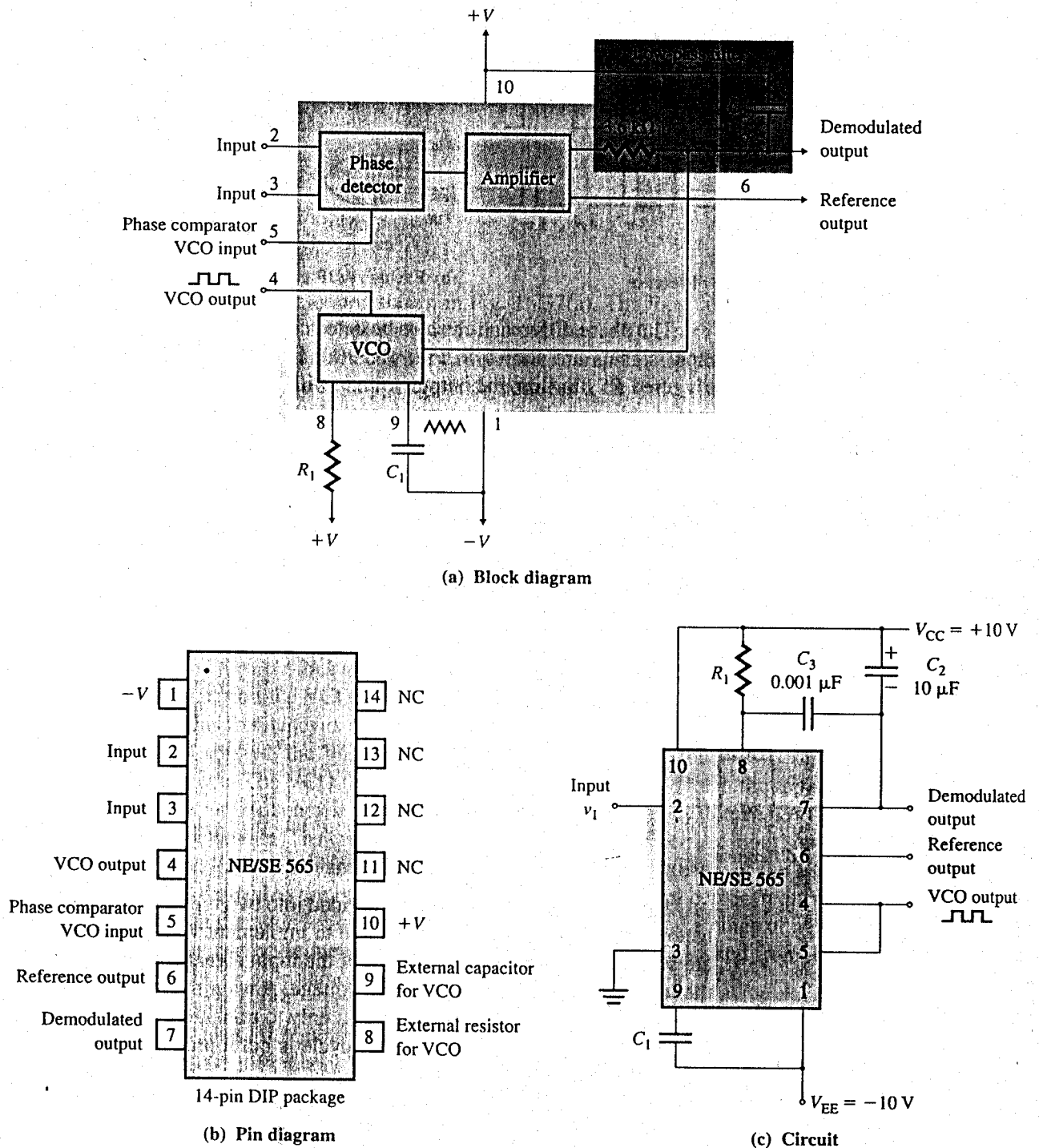
FIGURE 16.39 Edge-triggered phase detector

Phase detectors can be broadly divided into two types: digital detectors and analog detectors. The digital detectors are simple to implement with digital devices. However, they are sensitive to the harmonic content of the input signal and changes in the duty cycles of the input signal and the VCO output voltage. Analog detectors are monolithic types such as CMOS MC4344/4044. They respond only to transitions in the input signals. Thus, sensitivity to harmonic content and duty cycle is not a problem. The output voltage is independent of variations in the amplitude and duty cycle of the input waveform. Analog detectors are generally preferred over digital detectors, especially in applications in which accuracy is a critical factor.

Integrated Circuit PLL

The NE/SE 565 PLL is one of the most commonly used IC devices. The elements of the PLL in Fig. 16.37(a) are built into the 565 IC. The internal block diagram of the 565 is shown in Fig. 16.40(a), and the pin configuration is shown in Fig. 16.40(b). A typical connection diagram for the NE/SE 565 PLL is shown in Fig. 16.40(c). A small capacitor C_3 , typically of $0.001 \mu\text{F}$, is connected between pins 7 and 8 to eliminate possible oscillations. The center frequency of the PLL is given approximately by

$$f_o \approx \frac{1.2}{4R_1C_1} \quad (16.83)$$

FIGURE 16.40 NE/SE 565 PLL connection diagram

where R_1 and C_1 are an external resistance and a capacitance connected to pins 8 and 9, respectively. C_1 can have any value, but R_1 must have a value between $2\text{ k}\Omega$ and $20\text{ k}\Omega$. A capacitor C_2 is connected between pins 7 and 10 to form a first-order low-pass filter with an internal resistance of $3.6\text{ k}\Omega$. The filter capacitor C_2 should be large enough to eliminate variations in the demodulated output voltage at pin 7 in order to stabilize the VCO frequency.

The 565 PLL can typically lock to and track an input signal over a bandwidth of $\pm 60\%$ of the center frequency f_o . The lock range f_L is given by

$$f_L = \frac{8f_o}{V_{CC} - V_{EE}} \quad (16.84)$$

where V_{CC} and $-V_{EE}$ are the positive and negative power supplies in volts, respectively. The capture range f_c is given by

$$f_c = \left[\frac{f_L}{2\pi \times 3.6 \times 10^3 C_2} \right]^{1/2} \quad (C_2 \text{ in farads}) \quad (16.85)$$

EXAMPLE 16.12**D****SOLUTION**

Designing a PLL Design a PLL as shown in Fig. 16.40(c) so that $f_o = 2.5$ kHz and $f_c = 50$ Hz. Assume $V_{CC} = -V_{EE} = 12$ V.

The steps used to design the 565 PLL are as follows.

Step 1. Choose a suitable value of C_1 : Let $C_1 = 0.01$ μ F.

Step 2. Find the value of R_1 . From Eq. (16.83),

$$R_1 = \frac{1.2}{4C_1 f_o} = \frac{1.2}{4 \times 0.01 \mu\text{F} \times 2.5 \text{ kHz}} = 12 \text{ k}\Omega$$

Step 3. Find the lock range f_L . From Eq. (16.84),

$$f_L = \frac{8 \times 2.5 \text{ kHz}}{12 - (-12)} = 833 \text{ Hz}$$

Step 4. Find the value of C_2 . From Eq. (16.85),

$$C_2 = \frac{f_L}{2\pi \times 3.6 \times 10^3 f_c^2} = \frac{833}{2\pi \times 3.6 \times 10^3 \times 50^2} = 14.17 \mu\text{F}$$

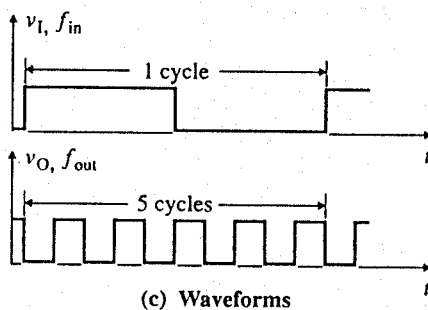
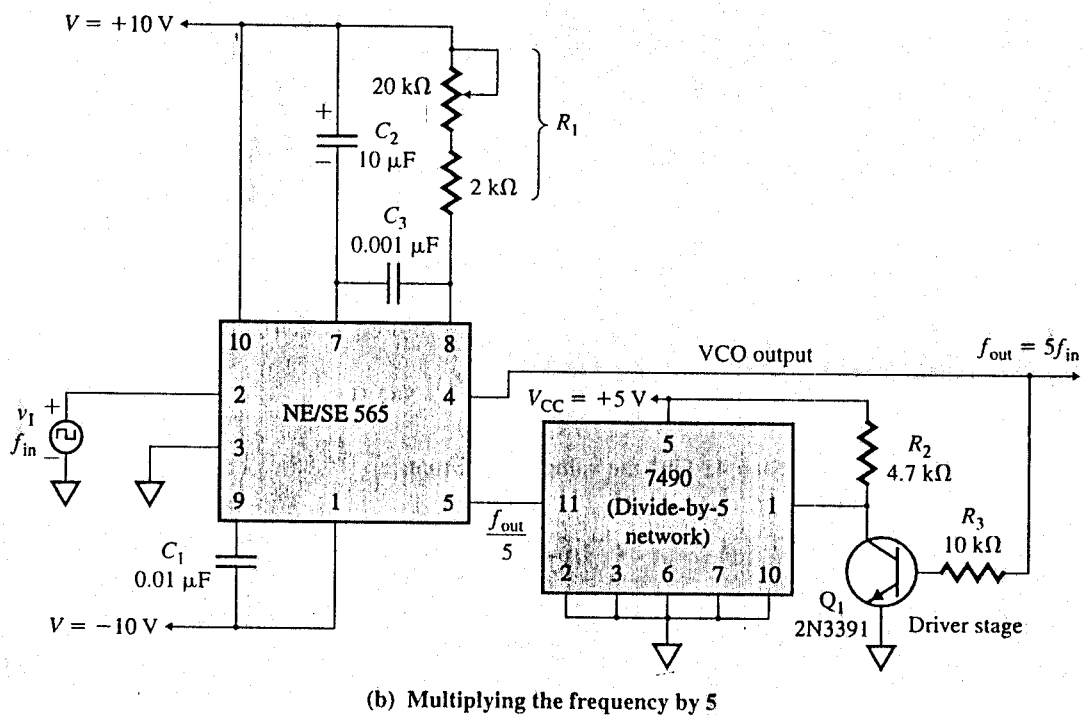
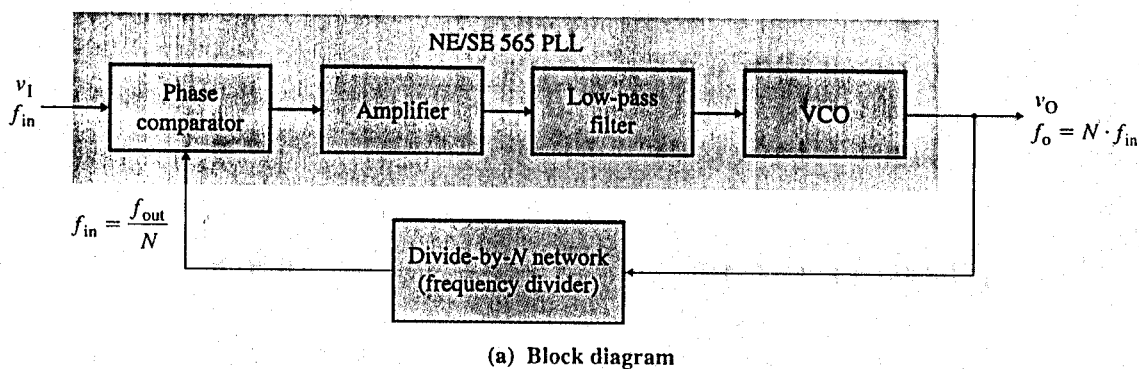
Choose $C_2 = 14$ μ F.

Applications of the 565 PLL

As examples of applications of the 565 PLL, we will consider a frequency multiplier, an FSK demodulator, and an SCA (subsidiary carrier authorization) decoder [2].

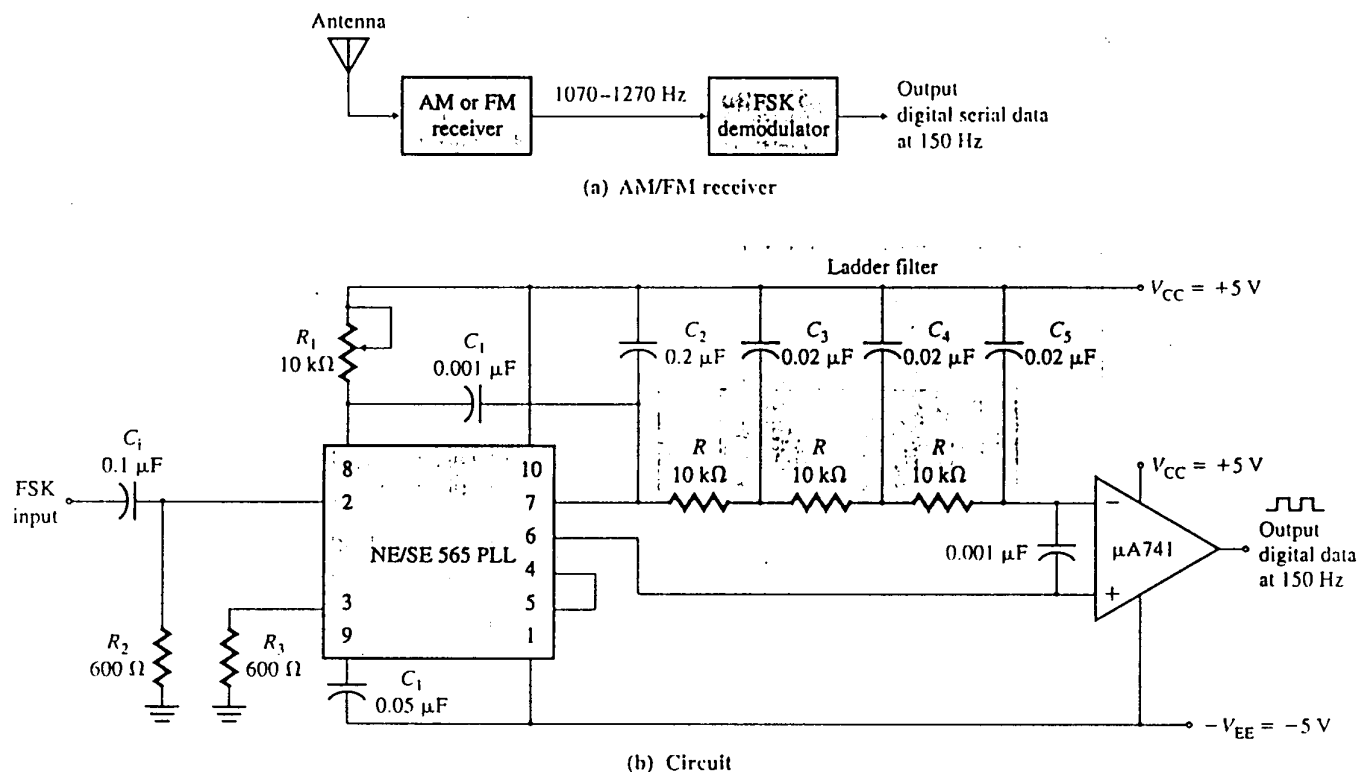
Frequency Multiplier A block diagram of a frequency multiplier using the 565 PLL is shown in Fig. 16.41(a). A frequency divider is inserted between the VCO and the phase detector. Since the output frequency of the divider is locked to the input frequency, the VCO will actually be running at a multiple of the input frequency. That is, $f_o = Nf_{in}$, where N is an integer. The amount of multiplication desired can be obtained by selecting the appropriate divide-by network. A typical connection of the 565 PLL to give an output frequency of $f_o = 5f_{in}$ is shown in Fig. 16.41(b).

To set up the circuit, you must know the frequency limits of the input signal. The free-running frequency of the VCO then can be adjusted by means of R_1 and C_1 so that the output frequency of the divider is midway between the input frequency limits. That is, for $f_{in} = 400$ Hz to 4 kHz, the output frequency would be $f_o = 2$ kHz to 20 kHz, with a midway frequency of $f_{o(\text{mid})} = 11$ kHz. The filter capacitance C_2 should be large enough (typically 10 μ F) to eliminate variations in the demodulated output voltage (at pin 7) in order to stabilize the VCO frequency. The output of the VCO will be a square wave whose

FIGURE 16.41 565 PLL as a frequency multiplier

frequency will be the multiple of the input frequency as long as the loop is in lock. The input and output waveforms are shown in Fig. 16.41(c).

FSK Demodulator An FSK demodulator is often used in AM/FM receivers, as shown in Fig. 16.42(a). One very useful application of the 565 PLL is as an FSK demodulator to receive FSK signals of 1070 Hz and 1270 Hz; the configuration is shown in Fig. 16.42(b). As the signal appears at the input, the PLL locks to the input frequency and tracks it

FIGURE 16.42. 565 PLL as an FSK demodulator

between the two frequencies, with a corresponding dc shift at the output. The input signal is connected through a coupling capacitor C_i to block the dc level from the FSK receiver. Both input terminals are connected to the ground through identical resistors R_2 and R_3 .

The loop filter capacitor C_2 determines the dynamic characteristics of the demodulator, and its value should be smaller than usual to eliminate overshoot on the output pulse. A three-stage RC-ladder low-pass filter is used to remove the carrier component from the output. The high cutoff frequency of the ladder filter—that is, $f_H = 1/2\pi RC$ —should be approximately halfway between the maximum keying rate (150 Hz) and twice the input frequency ($2 \times 1070\text{ Hz}$ is approximately 2200 Hz).

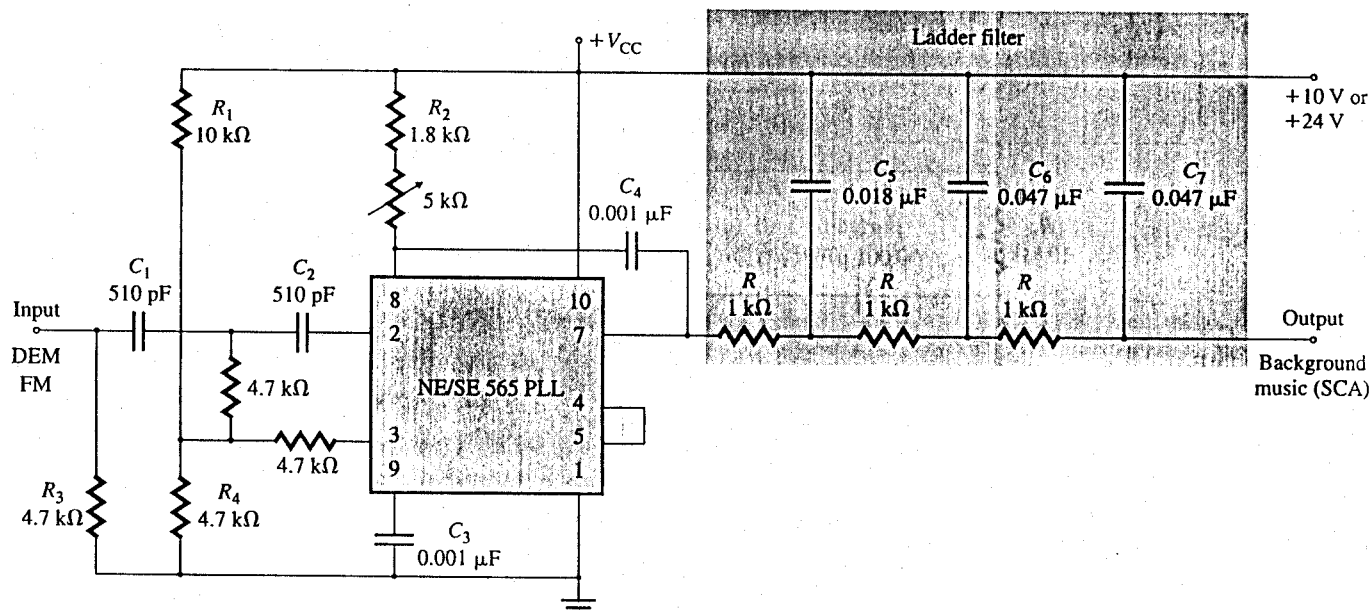
The output signal of 150 Hz can be made logic-compatible by connecting a voltage comparator between the output and pin 6 of the 565 PLL. R_2 and C_1 determine the free-running frequency of the VCO. The free-running frequency is adjusted with R_1 so as to produce a slightly positive voltage with $f_o = 1070\text{ Hz}$.

SCA (Background Music) Decoder Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use, using a frequency-modulated subcarrier of 67 kHz. This frequency was chosen so as not to interfere with the frequency spectrum of normal stereo or monaural FM program material, which is substantially lower. In addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

A PLL may be used to recover the SCA (subsidiary carrier authorization, or storecast music) signal from the combined signal of many commercial FM broadcast stations. This application involves demodulation of a frequency-modulated subcarrier of the main channel. The SCA signal can be filtered out and demodulated by the 565 PLL without the use

of any resonant circuits. A connection diagram is shown in Fig. 16.43. The PLL is tuned to 67 kHz with a 5-k Ω potentiometer; only approximate tuning is required, since the loop will seek the signal.

FIGURE 16.43 565 PLL as an SCA (background music) decoder



The demodulated output (pin 7) is passed through a three-stage low-pass filter to provide deemphasis and attenuate the high-frequency noise that often accompanies SCA transmissions. Since no capacitor is provided directly at pin 7, the circuit operates as a first-order loop. The demodulated output signal is on the order of 50 mV, and the frequency response extends to 7 kHz. By connecting the circuit of Figure 16.43 to a point between the FM discriminator and the deemphasis filter of a commercial-band (home) FM receiver and tuning the receiver to a station that broadcasts an SCA signal, one can obtain hours of commercial-free background music.

KEY POINTS OF SECTION 16.10

- A phase-lock loop (PLL) consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator. PLLs find applications as frequency multipliers, FSK demodulators, and SCA (background music) decoders.
- The operation of a PLL involves three modes: a free-running mode, a capture mode, and a phase-lock mode. The VCO frequency is continuously adjusted until it is equal to the input frequency. When the input frequency becomes equal to the output frequency, the PLL is said to be in the phase-lock mode.
- The 565 PLL can typically lock to and track an input signal over a bandwidth of $\pm 60\%$ of the center frequency.

16.11

Voltage-to-Frequency and Frequency-to-Voltage Converters

The NE/SE 566 VCO discussed in Sec. 16.8 can be used as a voltage-to-frequency converter. In many applications, it is also necessary to convert frequency to voltage. The TelCom 9400 series converters can be used as either *voltage-to-frequency* (V/F) or *frequency-to-voltage* (F/V) converters, and they can produce pulse and square-wave outputs with a frequency range of 1 Hz to 100 kHz. For V/F conversion, the device accepts an analog input signal and generates an output pulse train whose frequency is linearly

proportional to the input voltage. For F/V conversion, the device accepts any input frequency waveform and provides a linearly proportional voltage output. The complete V/F or F/V conversion requires only the addition of two capacitors, three resistors, and a reference voltage. The 9400 series consists of CMOS devices and bipolar devices that can operate on single or dual supply voltages.

V/F Converter

The 9400 V/F converter operates on the principle of charge balancing. The functional block diagram is shown in Fig. 16.44(a). The input voltage v_I is converted to a current I_{in} by the input resistor R_{in} . This current $I_{in} = v_I/R_{in}$ is then converted to a charge by the internal integrating capacitor C_{int} and gives a linearly decreasing voltage v_{O3} at the output of the op-amp integrator. That is,

$$v_{O3} = -\frac{I_{in}}{C_{int}} t = -\frac{v_I}{R_{in}C_{int}} t \quad (16.86)$$

As soon as voltage v_{O3} falls below the threshold level of the threshold detector, the switch closes and causes reference voltage V_{ref} to be applied to reference capacitor C_{ref} for a time long enough to charge the capacitor to reference voltage V_{ref} . This action also reduces the charge on the integrating capacitor by a fixed amount ($q = C_{ref}V_{ref}$), causing the integrator output to step up by a certain amount. At the end of the charging period, C_{ref} is shorted out, dissipating the charge stored on the reference capacitor so that the system is ready to repeat the cycle when the output again crosses the zero.

The continued charging of the integrating capacitor C_{int} by the input voltage is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases, causing the output frequency to increase also. Since each charge increment is fixed (i.e., $q = C_{ref}V_{ref}$), the increase in frequency with voltage is linear. The output frequency f_o is related to the input voltage by

$$f_o = \frac{v_I}{|V_{ref}|R_{in}C_{ref}} \quad (16.87)$$

where

$$\begin{aligned} v_I &= \text{input voltage} \\ |V_{ref}| &= \text{reference voltage} \\ C_{ref} &= \text{reference capacitance} \end{aligned}$$

The pin diagram of the 9400 V/F converter is shown in Fig. 16.44(b), and its internal block diagram is shown in Fig. 16.44(c). The threshold detector senses the output of the integrator. The output of the detector triggers a 3- μ s network when its input voltage passes through the threshold. The nominal threshold of the detector is halfway between the power supplies, or $(V_{DD} + V_{SS})/2 \pm 400$ mV. The output of the 3- μ s network is applied to the output transistor M_1 , the divide-by-2 network, and the C_{ref} charge/discharge control circuit.

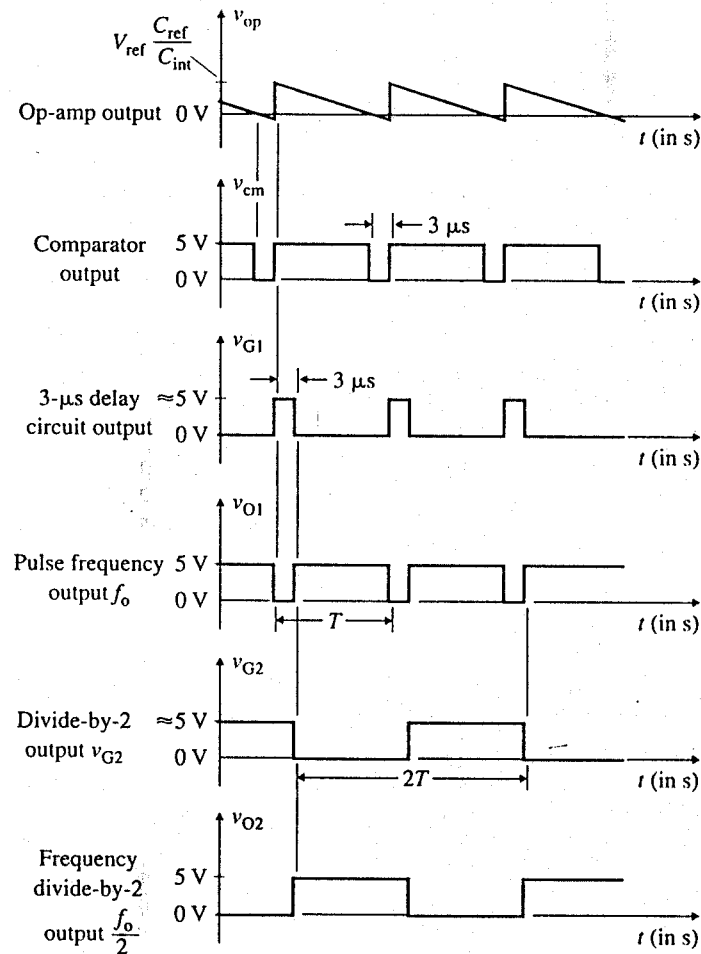
The self-start circuit ensures that the V/F converter operates properly when the power is first applied. If the integrator output is below the threshold voltage (i.e., 0 V) of the threshold detector and C_{ref} is already charged, then a positive voltage step will not occur when the power is turned on. The integrator output will continue to decrease until it crosses the -3.0-V threshold of the self-start comparator. When this happens, an internal resistor of 20 k Ω is connected to the op-amp integrator input, thereby forcing the output to become positive. As soon as the op-amp output becomes positive, the self-start circuit is disabled and the 9400 operates in its normal mode.

Pulse f_{out} ($=f_o$) output is an open-drain n -channel FET that provides a pulse waveform whose frequency is proportional to the input voltage v_I . Pulse $f_{out}/2$ ($=f_o/2$) output is an open-drain n -channel FET that provides a square wave whose frequency is one-half that of

the pulse waveform. This output will change state on the rising edge of f_o . Both f_o and $f_o/2$ outputs require a pull-up resistor and interface directly with MOS, CMOS, and TTL logic circuits.

The waveforms of the V/F converter are shown in Fig. 16.45. Three microseconds after the output V_d of the detector switches to low, the output V_{G1} of the delay circuit switches from low to high. When V_{G1} is low, transistor M_1 is off and f_{out} is high (i.e., 5 V). The divide-by-2 network is a negative-edge-triggered flip-flop whose output V_{G2} is a complement (inversion) of V_{G1} . Thus, transistor M_2 will be on, and $f_{out}/2$ will be low. With V_{G1} low, the charge/discharge control is disabled and capacitor C_{ref} remains discharged (that is, shorted out).

FIGURE 16.45
Waveforms of the 9400
V/F converter



EXAMPLE 16.13

D

SOLUTION

Designing a V/F converter Using the 9400 as shown in Fig. 16.46, design a V/F converter so that $f_o = 5$ kHz at $v_1 = 5$ V. The input voltage v_1 can vary between 10 mV and 10 V. Assume $V_{DD} = -V_{SS} = 5$ V.

The steps used to design the V/F converter are as follows.

Step 1. Choose V_{DD} and V_{SS} such that

$$4 \text{ V} \leq V_{DD} \leq 7.5 \text{ V} \quad \text{and} \quad -7.5 \text{ V} \leq V_{SS} \leq -4 \text{ V}$$

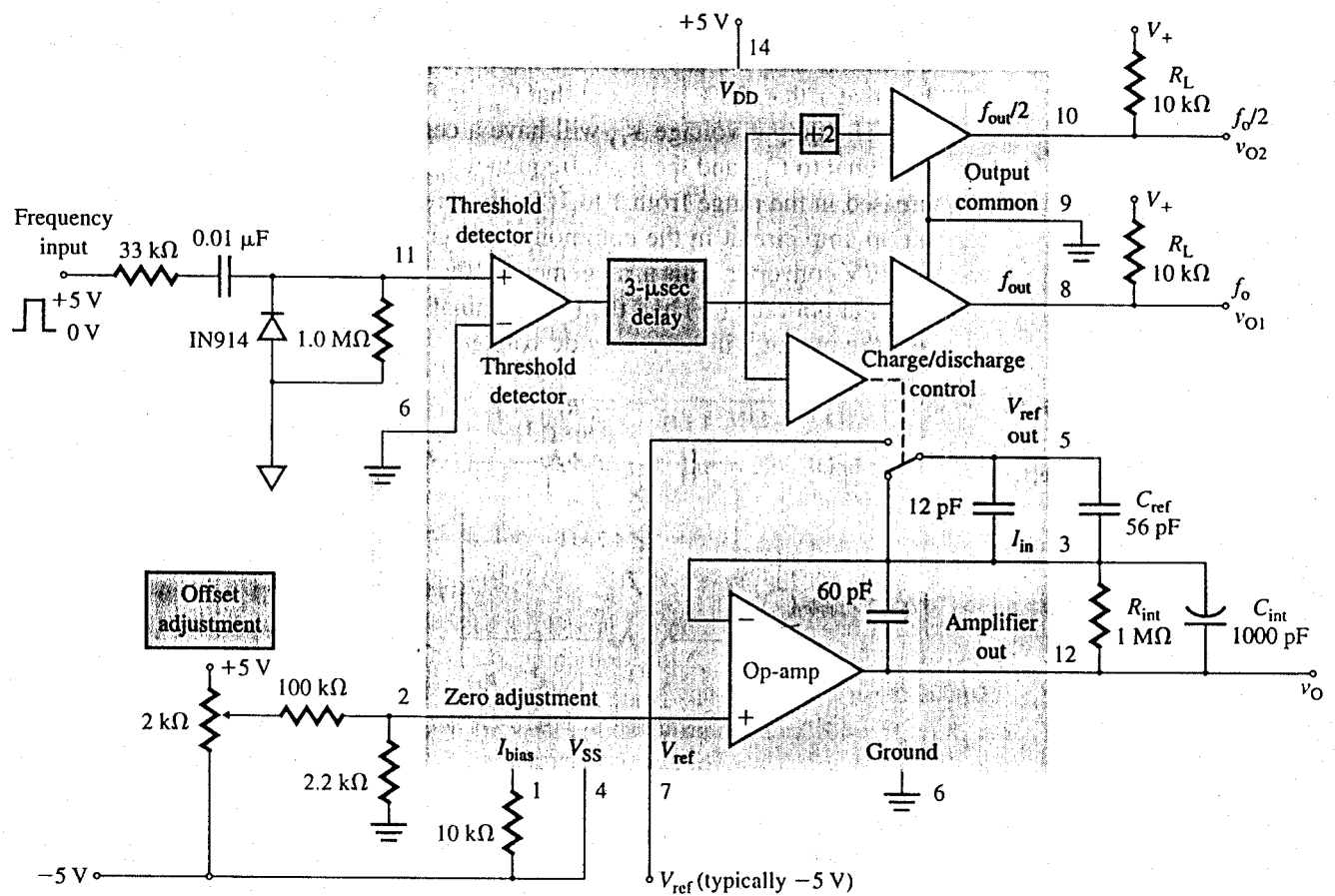
Choose $V_{DD} = 5$ V and $V_{SS} = -5$ V.

Step 2. Choose the capacitors such that $C_3 = C_4 = 0.1 \mu\text{F}$. These capacitors should be close to pins 4 and 14, respectively.

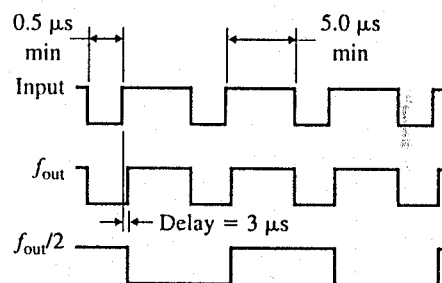
F/V Converter

When used as an F/V converter, the 9400 generates an output voltage that is linearly proportional to the input frequency f_{in} . The internal block diagram of the 9400 F/V converter is shown in Fig. 16.47(a). The input signal is differentiated by an RC network whose output is then applied to the (+) input of the threshold detector (i.e., at pin 11). The threshold detector has about ± 200 mV of hysteresis. Each time the input to the detector at pin 11 crosses zero in the negative direction, its output goes to low. Three microseconds later, the charge/discharge circuit is enabled, instantaneously connecting the reference capacitor C_{ref} , which remains discharged, to the reference voltage V_{ref} . This causes a precise amount of charge ($q = C_{ref}V_{ref}$) to be dispensed into the op-amp's summing junction. This charge in turn flows through feedback resistor R_{int} and generates a voltage pulse at the output of the op-amp. Capacitor C_{int} across R_{int} averages these pulses into a dc signal that is

FIGURE 16.47 Internal block diagram of 9400 F/V converter (Courtesy of TelCom Semiconductor, Inc.)



(a) Circuit connection



(b) F/V digital output

linearly proportional to the input frequency. The waveforms of the F/V converter are shown in Fig. 16.47(b). For charge q dispensed to capacitor C_{int} in time period T , we get

$$q = iT = \frac{V_O}{R_{\text{int}}} T$$

which, for $q = C_{\text{ref}} V_{\text{ref}}$, relates average output voltage V_O to input frequency f_{in} as follows:

$$V_O = |V_{\text{ref}}| R_{\text{int}} C_{\text{ref}} f_{\text{in}} \quad (16.88)$$

where

f_{in} = input frequency, in Hz

$|V_{\text{ref}}|$ = reference voltage, in V

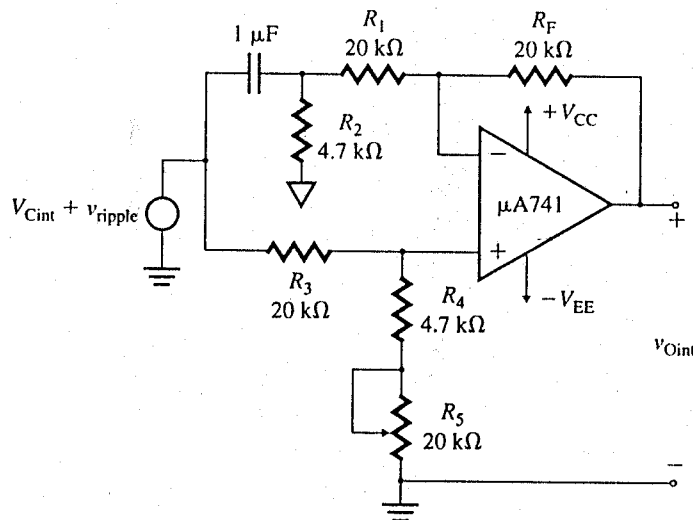
R_{int} = internal integrating resistance, in Ω

C_{ref} = reference capacitance, in F

The F/V converter will accept any input wave shape. However, the positive pulse width of the detector input (pin 11) must be at least $5 \mu\text{s}$, and the negative pulse width must be greater than $0.5 \mu\text{s}$. When the input frequency is less than 1 kHz, the duty cycle should be greater than 20% to ensure that C_{ref} is fully charged and discharged.

The output voltage V_O will have a certain amount of ripple, which is inversely proportional to C_{int} and the input frequency f_{in} . Therefore, for low frequencies, C_{int} can be increased in the range from 1 to $100 \mu\text{F}$ to reduce the ripple. To eliminate the ripple on V_O , an op-amp circuit in the common-mode configuration may be connected at the output of the F/V converter. This arrangement is shown in Fig. 16.48. Since the ac ripple content appears at both the (+) and the (−) terminals of the op-amp, the ac ripple will be canceled, and the output will have only dc voltage.

FIGURE 16.48
Ripple elimination in an
F/V converter



EXAMPLE 16.14

D

SOLUTION

Designing an F/V converter Using the 9400 as shown in Fig. 16.49, design an F/V converter so that $V_O = 2.5 \text{ V}$ at $f_{\text{in}} = 5 \text{ kHz}$. The input frequency f_{in} can vary between 0 Hz and 10 kHz. Assume $V_{\text{DD}} = -V_{\text{SS}} = 5 \text{ V}$.

The steps used to design the F/V converter are as follows.

Step 1. Choose V_{DD} and V_{SS} such that

$$4 \text{ V} \leq V_{\text{DD}} \leq 7.5 \text{ V} \quad \text{and} \quad -7.5 \text{ V} \leq V_{\text{SS}} \leq -4 \text{ V}$$

Choose $V_{\text{DD}} = 5 \text{ V}$ and $V_{\text{SS}} = -5 \text{ V}$.

Step 2. Choose the capacitors such that $C_3 = C_4 = 0.1 \mu\text{F}$. These capacitors should be close to pins 4 and 14, respectively.

- In a V/F converter, the input voltage is converted to charge by an op-amp integrator and gives a linearly decreasing output voltage. As soon as this voltage falls below a threshold level, a threshold detector causes the output to step up by a certain amount so that the system is ready to repeat the cycle when the output again crosses the zero.
- In an F/V converter, a precise amount of charge dispensed into the op-amp's summing junction generates a voltage pulse at the output of the op-amp. A capacitor is then used to average these pulses into a dc signal that is linearly proportional to the input frequency.

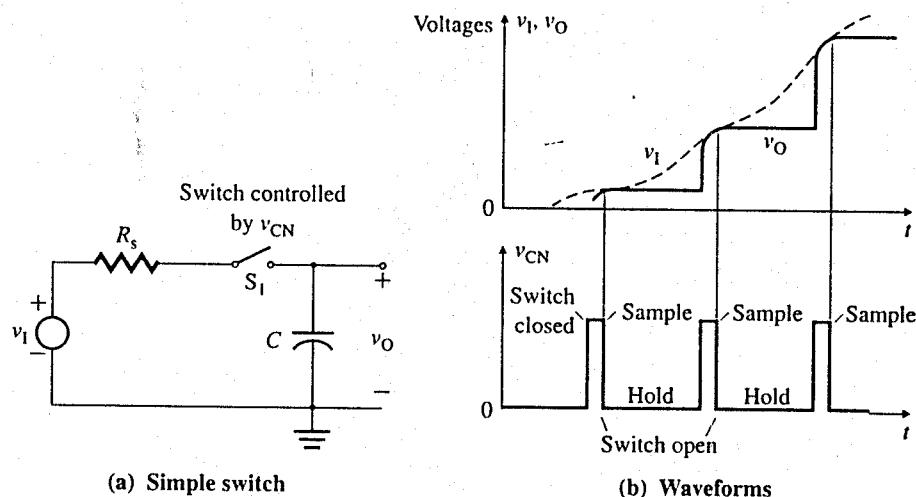
16.12 Sample-and-Hold Circuits

Sample-and-hold (SAH) circuits are used as an interface between an analog signal and a digital circuit in a wide variety of applications such as data acquisition, analog-to-digital (A/D) conversion, and synchronous data demodulation. An SAH circuit is used to *sample* an analog signal at a particular instant of time and *hold* the value of the sample as long as required. The sampling instants and hold duration are determined by a logic control signal. The hold duration depends on the type of application. For example, in A/D conversion, samples must be held long enough for the conversion to be completed.

The principle of operation of a sample-and-hold circuit can be explained with Fig. 16.50(a), which shows a circuit consisting of capacitor C , switch S_1 , and internal resistor R_s . The capacitor is used to hold the sample. The switch provides a means of rapidly charging the capacitor to the sample voltage and then removing the input so that the capacitor can retain the desired voltage. When the control signal v_{CN} is high, the switch is closed. If the time constant $R_s C$ is very small, the output voltage v_O will be very close to the input voltage v_I and will be equal to it at the instant the control signal becomes low and the switch is opened. The idealized waveforms for output voltage v_O , input voltage v_I , and control voltage v_{CN} are shown in Fig. 16.50(b).

FIGURE 16.50

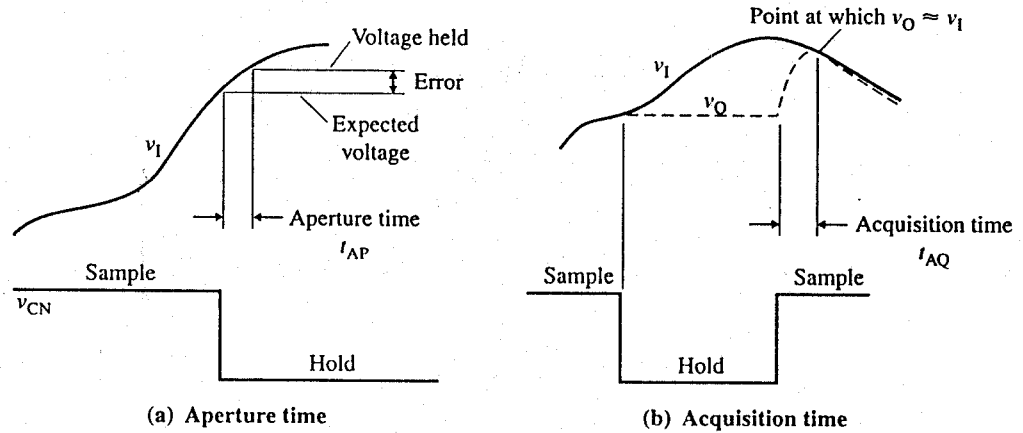
Principle of a sample-and-hold circuit



In practice, the capacitor can neither charge instantly nor hold a constant voltage. Also, the switch cannot open and close instantaneously. As a result, the practical output waveform will differ from the ideal one. Among the important specifications given by the manufacturers of sample-and-hold circuits are aperture time, acquisition time, settling time, and drop.

Aperture time t_{AP} , shown in Fig. 16.51(a), is the maximum time required for the sample-and-hold circuit to open. It is the delay between application of the control signal to open the switch and the instant when the switch actually does open. This time depends

FIGURE 16.51
Aperture time and
acquisition time



on the type of switch, but typically ranges from 4 to 20 μs . The t_{AP} of FET switches is in the range of 50 to 100 ns. The aperture time should be much less than the sampling period (i.e., the reciprocal of the sampling rate). Since the input signal is changing continuously, the hold voltage will change slightly during the aperture time, causing an error in the hold voltage.

Once the switch is closed for sampling, it takes a finite amount of time for the output voltage to become identical to the input signal, because the input was changing during the holding interval. *Acquisition time* t_{AQ} , shown in Fig. 16.51(b), is the minimum time, after application of the sample signal, required for the output voltage to reach the input voltage (with the necessary degree of accuracy).

Settling time t_s is the delay between the opening of the switch and the instant when the output reaches within a specified percentage of its final value (usually 0.99% of full-scale output). If the SAH circuit is followed by an A/D converter, conversion should not begin until the signal has settled; otherwise the wrong signal will be converted.

Drop, or output decay rate, is the voltage drop across capacitor C during the hold time. It is inversely proportional to the capacitance, since $dv_O/dt = I/C$, where I is the capacitor leakage current. This leakage current can arise as a result of biasing current in an op-amp, leakage current through the switch, or internal leakage in the capacitor.

The speed with which the output follows the input depends on the characteristics of the input signal v_i . v_O will follow v_i exponentially with time constant $R_s C$. In order for v_O to be within 0.01% of the output, its time period should be approximately $9R_s C$. In addition, the signal source must be able to supply the charging current required by capacitor C . Usually, the analog signal is buffered from the switch by a unity-gain op-amp follower in order to ensure a low value of R_s .

An SAH circuit can be implemented using an op-amp and a switch, as shown in Fig. 16.52(a). When switch S_1 is closed, the circuit operates as an RC filter. For a step input voltage of V_I , the output voltage $v_O(t)$ can be found from

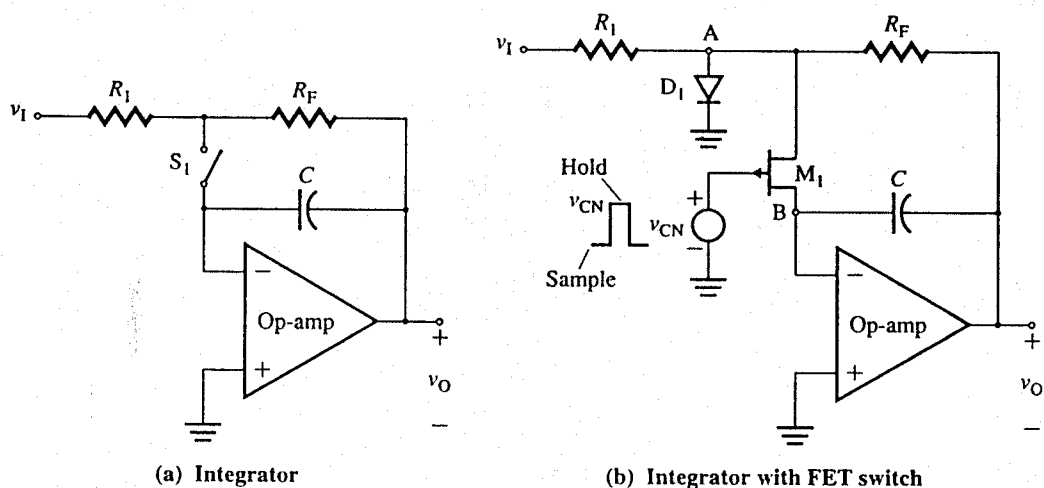
$$v_O(t) = -\frac{R_F}{R_I} V_I (1 - e^{-t/R_F C}) \quad (16.89)$$

For v_O to reach V_I in the shortest time, the time constant $R_F C$ must be shorter than the sample interval so that the output can track the input. When switch S_1 is opened, the capacitor will hold its voltage of $-V_I$. To minimize the output voltage drop, the op-amp should have a low input biasing current (as does an op-amp with an FET input stage, for example). Also, a high-quality capacitor with a low leakage current should be used.

Sample-and-Hold Op-Amp Circuits

FIGURE 16.52

Inverting sample-and-hold op-amp circuit



(a) Integrator

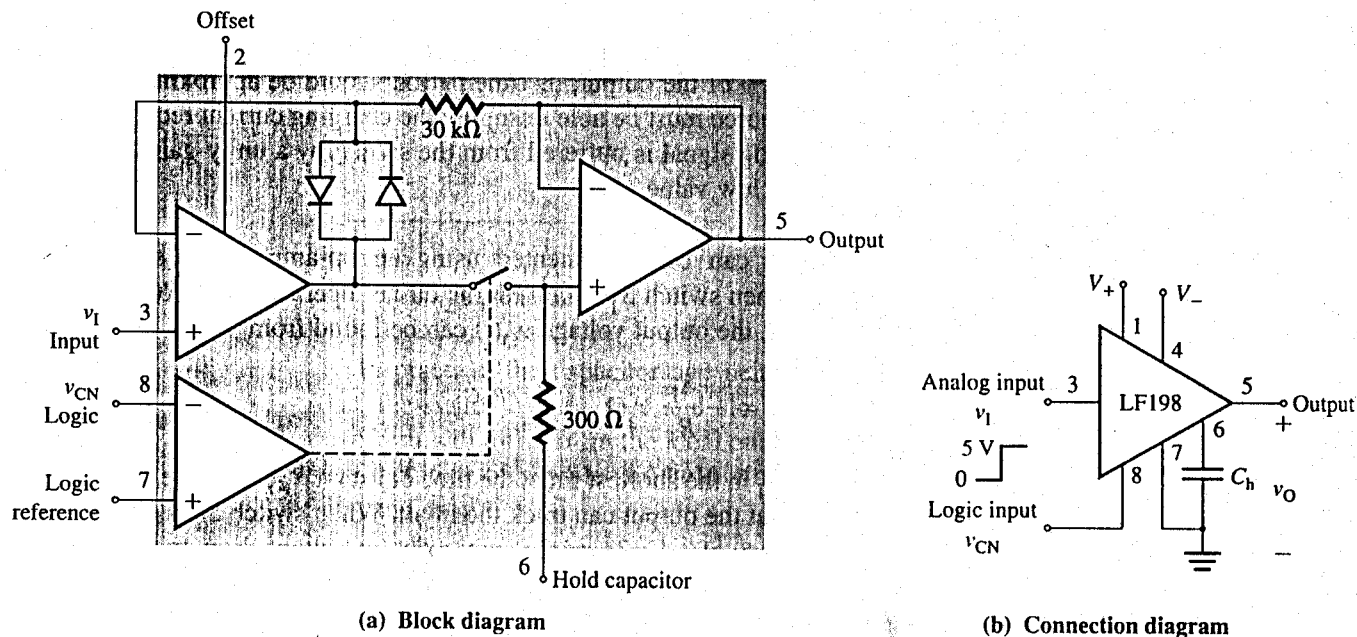
(b) Integrator with FET switch

Switch S_1 can be replaced by a transistor M_1 (i.e., a p -channel FET), as shown in Fig. 16.52(b). If the control voltage v_{CN} is low (say, 0 V), the FET M_1 will be on (that is, the switch will be closed) and the capacitor will be in sample mode, charging to V_I . Whereas if the control voltage v_{CN} is high (say, +5 V), the FET will be off (that is, the switch will be open) and the capacitor will be in hold mode.

Diode D_1 clamps the voltage at node A to 0.7 V. When M_1 is on, the diode effectively becomes connected across the FET (that is, between its drain and source). Since the voltage drop across the FET is low, the voltage across the diode will also be small—much less than 0.7 V. Thus, the diode will have no effect during the sampling time.

Sample-and-Hold ICs

Sample-and-hold ICs such as the LF198 use BiFET technology to obtain ultra-high dc accuracy (within 0.01%) with fast signal acquisition (4 μ s) and a low drop (3 mV/s). The functional block diagram of the LF198 is shown in Fig. 16.53(a), and its connection diagram is shown in Fig. 16.53(b). The manufacturers give curves showing the variation in acquisition time t_{AQ} with hold capacitance C_h . For example, $t_{AQ} = 4 \mu$ s for hold capacitance $C_h = 1000$ pF, and $t_{AQ} = 20 \mu$ s for $C_h = 0.01 \mu$ F.

FIGURE 16.53 Sample-and-hold LF198 (Courtesy of National Semiconductor, Inc.)

(a) Block diagram

(b) Connection diagram

KEY POINTS OF SECTION 16.12

- A sample-and-hold circuit uses a capacitor to sample an analog signal at a particular instant of time and hold the value of the sample as long as required. A switch is closed to charge the capacitor rapidly to the sample voltage and then is opened to remove the input so that the capacitor can retain the desired voltage.
- The specifications of a sample-and-hold circuit include acquisition time, aperture time, settling time, and drop, or output decay rate.

16.13 Digital-to-Analog Converters

Digital systems are used in a wide variety of applications because of their efficiency, reliability, and economical operation. Applications include process and industrial control, measurement and testing, graphics and displays, data telemetry, voice and video communication, and arithmetic operations. Data processing, which has become an integral part of various systems, involves the transfer of data to and from digital devices such as microprocessors via input and output devices.

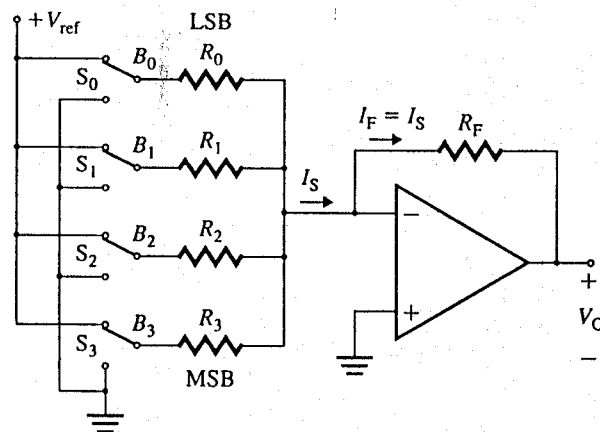
The output of digital systems is in binary form: ones and zeros. After processing is accomplished using digital methods, the processed signal is converted back to analog form. The circuit that performs this conversion is called a *digital-to-analog (D/A) converter*. A D/A system normally contains four separate parts: a reference quantity; a set of binary switches to simulate binary coefficients $B_0, \dots, B_N$; a resistive network, and an output summing means.

A simple D/A converter is shown in Fig. 16.54(a). This converter can convert a 4-bit parallel digital word ($B_0B_1B_2B_3$) to an analog voltage that is proportional to the binary number corresponding to the digital word. Four switches are used to simulate the binary inputs. (In practice, a 4-bit binary counter may be used instead.) The logic voltages, which represent the individual bits B_0, B_1, B_2 , and B_3 , are used to operate switches S_0, S_1, S_2 , and S_3 , respectively. When a B is a 1, the corresponding switch is connected to reference voltage V_{ref} ; when a B is a 0, the corresponding switch is grounded.

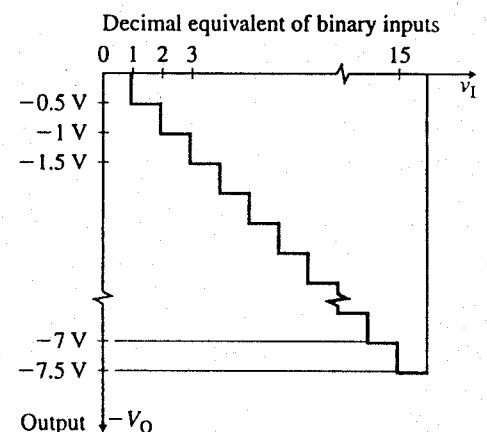
The inverting terminal of the op-amp is at virtual ground (i.e., $V_d \approx 0$), so the total current I_S is given by

$$I_S = V_{\text{ref}} \left(\frac{B_3}{R_3} + \frac{B_2}{R_2} + \frac{B_1}{R_1} + \frac{B_0}{R_0} \right)$$

FIGURE 16.54 Weighted-resistor D/A converter



(a) Circuit



(b) Output voltage

Weighted-Resistor D/A Converter

Since the current flowing into the op-amp is negligible, $I_S \approx I_F$. Thus, the analog output voltage is given by

$$V_O = -R_F I_F = -R_F V_{\text{ref}} \left(\frac{B_3}{R_3} + \frac{B_2}{R_2} + \frac{B_1}{R_1} + \frac{B_0}{R_0} \right) \quad (16.90)$$

Resistors are weighted so that successive resistor values are related by a factor of 2 and the value of each individual resistor is inversely proportional to the numerical significance of the appropriate binary digit. That is,

$$\text{LSB (least significant bit)} \rightarrow R_0 = \frac{R}{2^0} = R$$

$$R_1 = \frac{R}{2^1} = \frac{R}{2}$$

$$R_2 = \frac{R}{2^2} = \frac{R}{4}$$

$$\text{MSB (most significant bit)} \rightarrow R_3 = \frac{R}{2^3} = \frac{R}{8}$$

Substituting these weighted resistor values into Eq. (16.90) gives the analog output voltage V_O as

$$V_O = -\frac{V_{\text{ref}} R_F}{R} (2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0) \quad (16.91)$$

where $B_i = 1$ if switch S_i is connected to V_{ref} and $B_i = 0$ if switch S_i is grounded. For an input of $B_3 B_2 B_1 B_0 = 1111$, $V_O = -15 V_{\text{ref}} R_F / R$; for $B_3 B_2 B_1 B_0 = 0110$, $V_O = -6 V_{\text{ref}} R_F / R$; and for $B_3 B_2 B_1 B_0 = 0001$, $V_O = -V_{\text{ref}} R_F / R$. Thus, the output V_O is directly proportional to the numerical value of the binary number $B_3 B_2 B_1 B_0$. Since there are 16 (that is, 2^4) combinations of the binary inputs B_3 , B_2 , B_1 , and B_0 , the analog output will have 16 possible corresponding values. For $V_{\text{ref}} = 5 \text{ V}$ and $R = 10 R_F$, Eq. (16.91) gives V_O as

$$V_O = -0.5 \times (2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0)$$

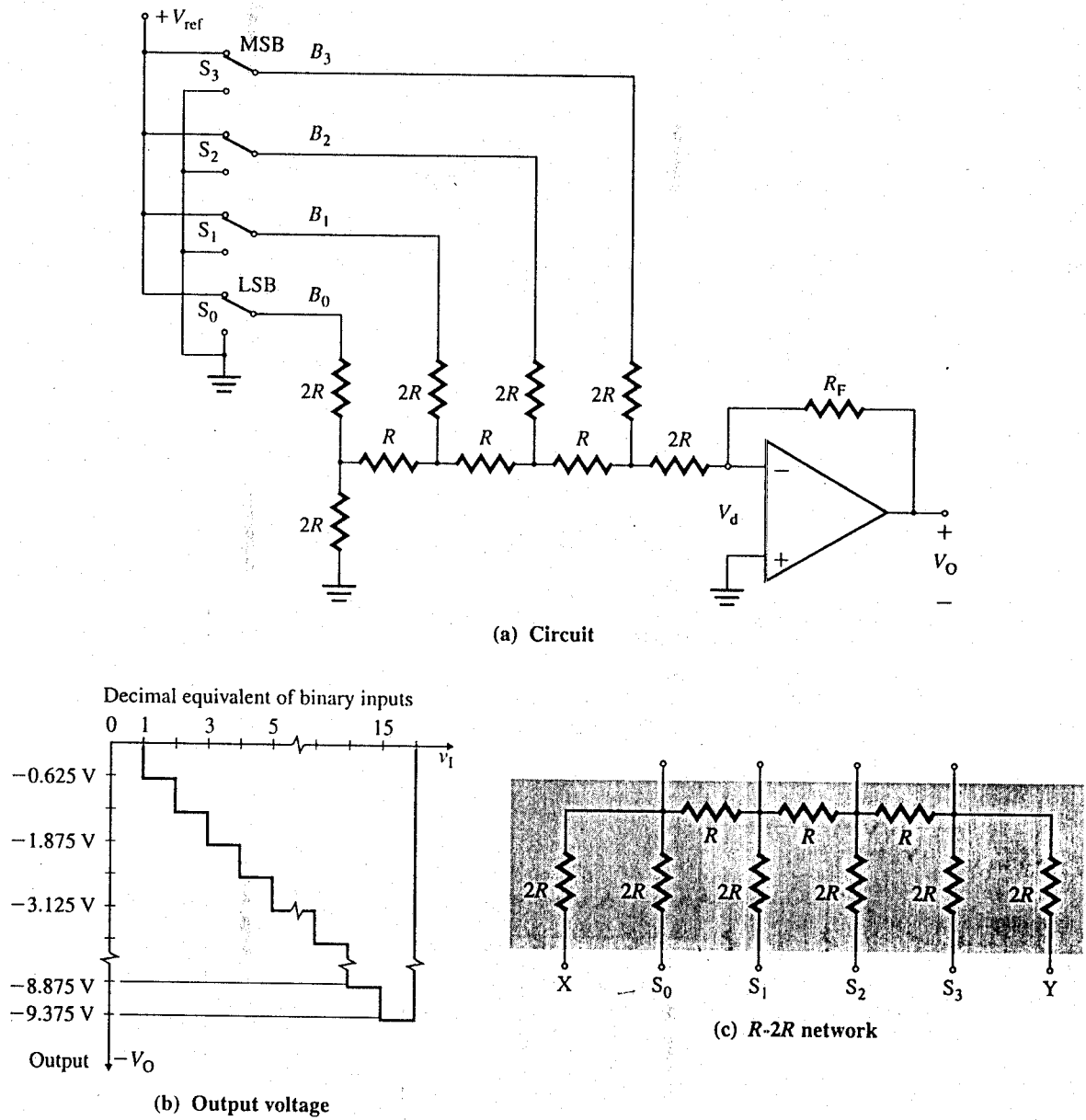
The plot is shown in Fig. 16.54(b). The major disadvantage of this D/A converter is the wide variety of resistor values required to weight the network. If the resistor values change in response to temperature changes, it will be difficult to obtain identical tracking characteristics. As a result, the accuracy and the stability of the D/A will be degraded.

R-2R Ladder Network D/A Converter

The R-2R D/A ladder converter, shown in Fig. 16.55(a), has only two resistor values R and $2R$, rather than a wide range of resistor values. The plot of the output (which is known as a "resistance ladder") is shown in Fig. 16.55(b). Figure 16.55(c) exhibits the property that the equivalent resistance, looking into any of the terminals X , Y , S_3 , S_2 , S_1 , or S_0 with the remainder of the terminals grounded, is $3R$.

Consider the circuit with LSB = 1 only—that is, switch S_0 is closed. The equivalent circuit for LSB = 1 only is shown in Fig. 16.56(a). Successive Thevenin's conversions lead [through the circuits shown in Figs. 16.56(b) and 16.56(c)] to the final circuit shown in Fig. 16.56(d), which gives the output due to LSB = 1 as

$$V_O = -\frac{V_{\text{ref}} R_F}{3R} \left(\frac{B_0}{2^4} \right) \quad \text{for LSB} = 1 \text{ only}$$

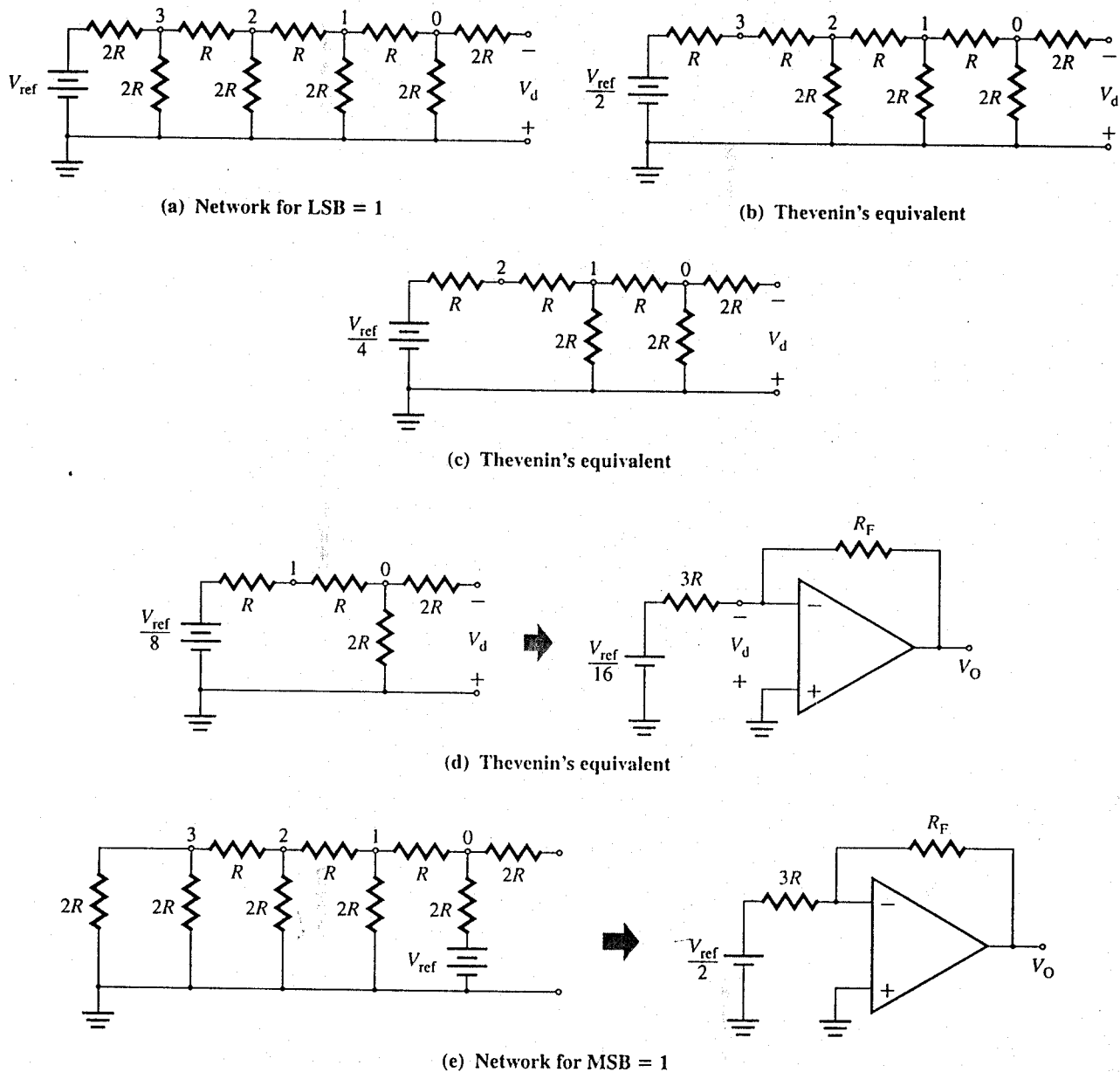
FIGURE 16.55 *R-2R ladder D/A converter*

Now consider the circuit with $\text{MSB} = 1$ only—that is, switch S_3 is closed. The equivalent circuit for $\text{MSB} = 1$ only is shown in Fig. 16.55(e), which can be simplified by applying the series and parallel rule for R s. The simplified circuit shown gives the output due to $\text{MSB} = 1$ as

$$V_O = -\frac{V_{\text{ref}} R_F}{3R} \left(\frac{B_3}{2^1} \right) \quad \text{for MSB} = 1 \text{ only}$$

Thus, the output voltage is scaled up by the numerical value of the binary digit. Applying the superposition theorem, we can find the output voltage when all switches are on (i.e., switch S_i is connected) as

$$V_O = -\frac{V_{\text{ref}} R_F}{3R} \left(\frac{B_3}{2^1} + \frac{B_2}{2^2} + \frac{B_1}{2^3} + \frac{B_0}{2^4} \right) \quad (16.92)$$

FIGURE 16.56 Equivalent R - $2R$ ladder for $\text{LSB} = 1$ only and $\text{MSB} = 1$ only

which can be simplified to

$$V_O = -\frac{V_{\text{ref}} R_F}{48R} (2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0) \quad (16.93)$$

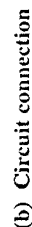
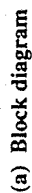
where $B_i = 1$ if switch S_i is connected to V_{ref} and $B_i = 0$ if switch S_i is grounded. For an input of $B_3 B_2 B_1 B_0 = 1111$, $V_O = -15V_{\text{ref}} R_F / 48R$; for $B_3 B_2 B_1 B_0 = 0110$, $V_O = -6V_{\text{ref}} R_F / 48R$; and for $B_3 B_2 B_1 B_0 = 0001$, $V_O = -V_{\text{ref}} R_F / 48R$. For $V_{\text{ref}} = 5 \text{ V}$ and $R = R_F$, Eq. (16.93) gives V_O as

$$V_O = -(5/48) \times (2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0)$$

whose plot is shown in Fig. 16.55(b).

IC D/A Converters

Switches in IC D/A converters are made either of BJTs or of FETs. They are generally one of two types: voltage driven or current driven. Voltage-driven converters, which use BJTs or FETs as on or off switches, are generally used for relatively low-speed low-resolution



the D/A converter is not zero when the binary inputs are all zero. This error stems from input offsets (in voltages and currents) of the op-amp as well as the D/A converter. *Settling time* is the time required for the output of the D/A converter to reach within $\pm \frac{1}{2}$ LSB of the final value for a given digital input—that is, go from zero to full-scale output. *Stability* is a measure of the independence of the converter parameters from variations in external conditions such as temperature and supply voltage.

KEY POINTS OF SECTION 16.13

- A D/A converter can convert a digital word to an analog voltage that is proportional to the binary number corresponding to the digital word.
- The specifications for a D/A converter include resolution, accuracy, nonlinearity (or linearity error), gain error, offset error, settling time, and stability. The resolution of an N -bit converter is $1/2^N$.

16.14 ► Analog-to-Digital Converters

A large number of physical devices generate output signals that are analog or continuous variables; examples include temperature and pressure gauges and flow transducers. For digital processing, the input signal must be converted into a binary form of ones and zeros. The circuit that performs this conversion is called an analog-to-digital (A/D) converter. There are many types of A/D converters, depending on the type of conversion technique used, such as counting, tracking (up-down), successive approximation, single-ramp integrating, or dual-ramp integrating. The successive-approximation technique is the one most commonly used, mainly because it offers excellent tradeoffs in resolution, speed, accuracy, and cost.

Successive- Approximation A/D Converter

A successive-approximation A/D converter operates by successively dividing in half the voltage range of the converter. The simplified block diagram of a 4-bit A/D converter is shown in Fig. 16.59(a). The converter consists of five parts: an analog comparator, a 4-bit register which has independent set and reset capability for each stage, a 4-bit D/A converter, a ring counter, and a logic control. The ring counter provides a timing (or clock) signal to control the operation of the converter. The logic control synchronizes the operation of the converter with the clock. The combination of the logic control, 4-bit register, and ring counter is often known as the *successive-approximation register* (SAR).

The comparator converts analog voltages to digital signals. It has two inputs, V_a and V_b , and gives a binary voltage. If $V_a > V_b$, the output is high (logic 1); if $V_a < V_b$, the output is low (logic 0). Thus, the comparator output V_{com} is

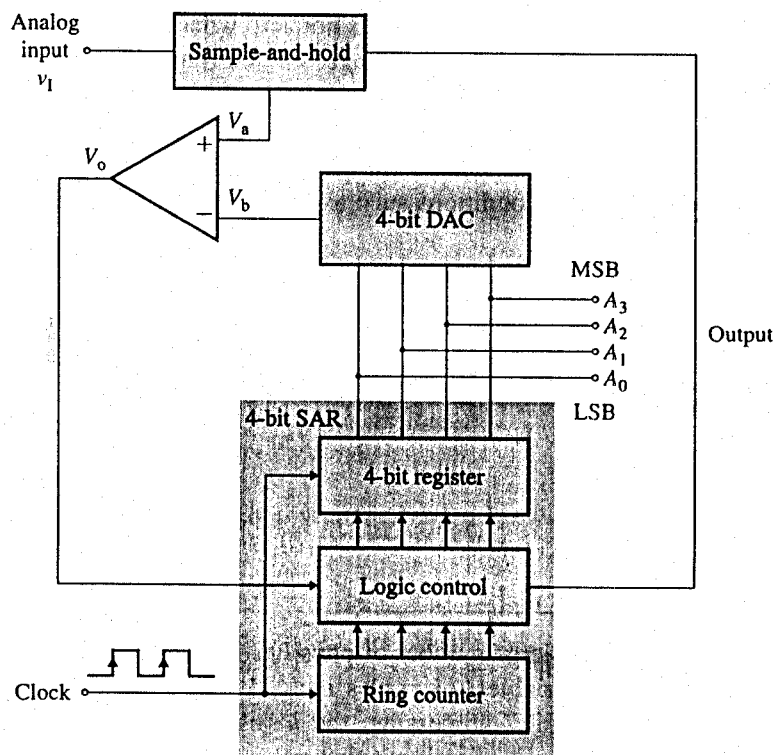
$$V_{com} \equiv \text{sgn}(V_a - V_b) = \begin{cases} 1 & \text{for } V_a > V_b \\ 0 & \text{for } V_a < V_b \end{cases}$$

A sample-and-hold circuit is commonly used to hold the input voltage constant during the conversion process. There is no need for a sample-and-hold circuit if the input signal varies slowly enough and has a low enough noise level that the input will not change during the conversion.

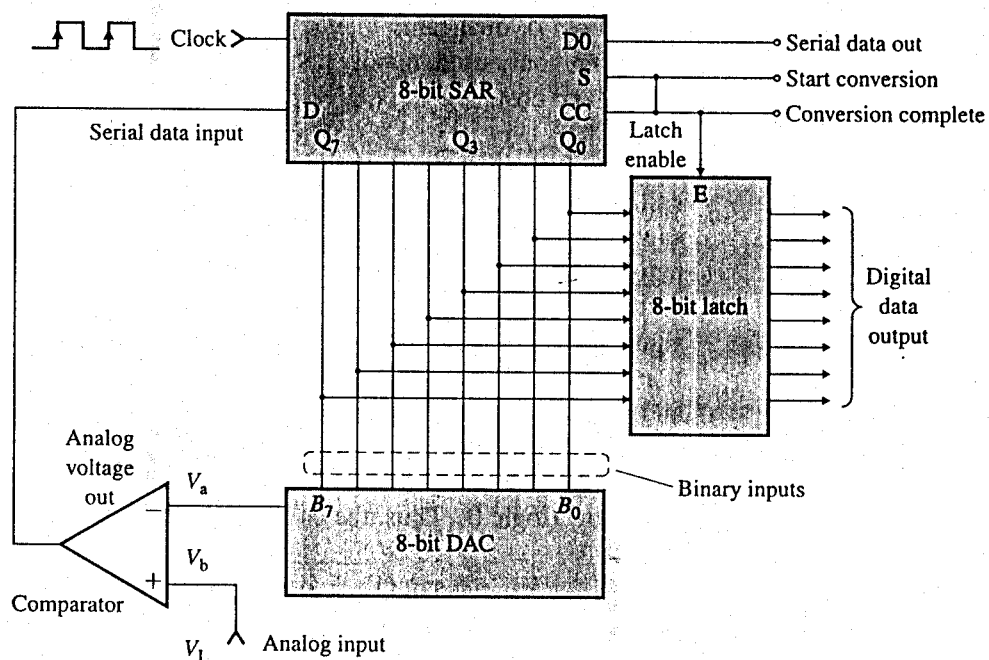
The algorithm for the operation of a successive-approximation A/D converter can be best described by an example. The steps in converting an analog voltage of, say, 10 V are as follows:

Step 1. The first pulse from the ring counter sets the D/A converter, 4-bit register, and ring counter so that MSB = 1 and all others are 0. That is, $B_3 = 1$, and $B_2 = B_1 = B_0 = 0$. Thus, for $B_3B_2B_1B_0 = 1000$, the output V_b of the D/A is 8 V, which is compared by the

FIGURE 16.59
Successive-approximation
A/D converter



(a) 4-bit A/D converter



(b) 8-bit A/D converter

comparator. If $V_a \geq 8 \text{ V}$, the MSB in the register (B_3) is maintained at 1; otherwise it is set to 0. At the end of step 1, $B_3 = 1$ for $V_a = 10 \text{ V}$.

Step 2. The second pulse from the ring counter sets $B_2 = 1$. B_1 and B_0 remain at 0, and B_3 remains at either 1 or 0, depending on the condition in step 1. That is, $B_3 = B_2 = 1$, and $B_1 = B_0 = 0$. Thus, for $B_3 B_2 B_1 B_0 = 1100$, the output V_b of the D/A is 12 V, which is

compared by the comparator. If $V_a \geq 12$ V, the B_2 in the register is maintained at 1; otherwise it is set to 0. At the end of step 2, $B_2 = 0$ for $V_a = 10$ V.

Step 3. The third pulse from the ring counter sets $B_1 = 1$. B_0 remains at 0. B_2 and B_3 remain as they were at the end of step 2. That is, $B_3 = 1$, $B_2 = 0$, $B_1 = 1$, and $B_0 = 0$. Thus, for $B_3B_2B_1B_0 = 1010$, the output V_b of the D/A is 10 V, which is compared by the comparator. If $V_a \geq 10$ V, the B_1 in the register is maintained at 1; otherwise it is set to 0. At the end of step 3, $B_1 = 1$ for $V_a = 10$ V.

Step 4. The fourth pulse from the ring counter sets $B_0 = 1$. B_3 , B_2 , and B_1 remain as they were at the end of step 3. That is, $B_3 = 1$, $B_2 = 0$, $B_1 = 1$, and $B_0 = 1$. Thus, for $B_3B_2B_1B_0 = 1011$, the output V_b of the D/A is 11 V, which is compared by the comparator. If $V_a \geq 11$ V, the B_0 in the register is maintained at 1; otherwise it is set to 0. That is, $B_0 = 0$ for $V_a = 10$ V.

At the end of the fourth step, the desired number, which is in the counter, will give Read output. The results of the conversion steps are shown in Table 16.2. For an N -bit A/D converter, the conversion process will take N clock periods. That is, for an 8-bit A/D converter and a 10-MHz clock, the conversion will take $8/10 \times 10^6 = 8 \times 10^{-7} = 800$ ns.

The successive-approximation technique can be extended to the higher-bit converter shown in Fig. 16.59(b), in which the successive-approximation register (SAR) also performs the functions of logic control and ring counter. The conversion complete (CC) signal enables the latch. Digital data appear at the output of the latch and are also available serially as the SAR determines each bit. The cycle of the conversion process is normally repeated continuously, and the CC signal is connected to the Start-Conversion input.

TABLE 16.2
Successive approximation
process for $V_a = 10$ V

Step	V_b	B_3	B_2	B_1	B_0	Comparisons	Answer
1	8 V	1	0	0	0	Is $V_a \geq 8$ V?	Yes
2	12 V	1	1	0	0	Is $V_a \geq 12$ V?	No
3	10 V	1	0	1	0	Is $V_a \geq 10$ V?	Yes
4	11 V	1	0	1	1	Is $V_a \geq 11$ V?	No
	10 V	1	0	1	0	Read output	

IC A/D Converters

There are many types of IC A/D converters, such as the integrating A/D converter, the integrating A/D converter with three-stage outputs, and the tracking A/D converter with latched output. Also, the output can be in straight binary, binary-coded decimal (BCD), complementary binary (1s or 2s), or sign-magnitude binary form.

The NE5034 is an example of an IC A/D converter. Its internal block diagram is shown in Fig. 16.60(a). It is a high-speed microprocessor-compatible 8-bit A/D converter that uses the successive-approximation technique. It includes a comparator, a reference D/A converter, an SAR, an internal clock, and three-stage buffers all on the same chip. The connection diagram for the NE5034 is shown in Fig. 16.60(b). Upon receipt of the Start pulse, successive bits are applied to the input of the internal 8-bit current D/A converter by the I^2L SAR, beginning with the MSB (DB7). During the successive approximations, the sequence Data-Ready (DR) remains at 1. OE is the Output-Enable input. When OE is at logic 1, the data outputs assume a high-impedance status. When OE is at logic 0, the data are placed on the outputs. External capacitor C_L sets the internal clock frequency, as shown in Fig. 16.60(c). For $C_L = 100$ pF, for example, $f_{\text{clock}} = 100$ kHz.

because of the finite resolution of the discrete output. It is usually $\pm \frac{1}{2}$ LSB. For a 10-bit converter with an analog input range of 0 to 10 V, the quantizing error will be $1/2^{10} \times 10 \text{ V} \approx 10 \text{ mV}$. *Accuracy* is the deviation of the actual bit transition value from the ideal transition value at any level over the range of the A/D converter. Accuracy includes errors from both the analog and the digital parts. With a digital error of 10 mV and a quantizing error of 10 mV, the overall error becomes 20 mV. With this amount of error, the converter will operate as a 9-bit A/D converter, because a 9-bit converter has a quantizing error of $1/2^9 \times 10 \text{ V} \approx 20 \text{ mV}$.

KEY POINTS OF SECTION 16.14

- An A/D converter can convert an analog signal to a digital word that is proportional to the analog signal. Although there are many conversion techniques, the successive-approximation technique is the one most commonly used, mainly because of its excellent tradeoffs in resolution, speed, accuracy, and cost.
- The specifications for an A/D converter include input signal range, conversion speed, quantizing error, and accuracy.

16.15 ►

Circuit Design Using Analog ICs

There are many analog integrated circuits for general and special-purpose applications. They include operational amplifiers, voltage comparators, instrument amplifiers, timers, buffers, interfacing circuits, voltage/frequency converters, data conversion circuits, power conversion and control circuits, and voltage regulators. The circuit design for an application using an IC is very simple and requires the selection of external components only. The steps involved are as follows:

Step 1. Identify the function(s) to be performed and the specifications, including available power supplies, range of input and output signals, and operating frequency range.

Step 2. Find a suitable IC that can perform the desired function(s), and look for application examples and/or guidelines for that IC. Usually the manufacturer provides application examples and guidelines.

Step 3. Determine the values of external components (usually capacitors and resistors). Generally, the manufacturer provides selection charts or curves. Unless otherwise specified, use standard values of components, with tolerances of, say, 5%.

Step 4. Simulate the circuit with a simulator such as PSpice/SPICE or Electronics Workbench, if the IC is supported by the simulator.

Step 5. Build and test the circuit, if possible.

Summary

Various waveforms are often required in electronic and control circuits. There are many integrated circuits (ICs) that can be used to generate these waveforms. The design of wave generators is very simple and requires the selection of the external circuit components only. ICs such as op-amps, comparators, the NE/SE 566 VCO, the 555 timer, the NE/SE 565 PLL, and the 9400 series converters can be used to generate various waveforms.

References

1. M. H. Rashid, *SPICE for Circuits and Electronics Using PSpice*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1995, Chapter 10.
2. S. Soclof, *Design and Applications of Analog Integrated Circuits*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1991, Chapters 15, 16, and 17.

3. P. R. Gray and R. G. Meyer, *Analysis and Design of Integrated Circuits*. New York: John Wiley & Sons, 1992.
4. R. A. Gayakwad, *Op-Amps and Linear Integrated Circuits*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1993.

Review Questions

1. What are the differences between a comparator and an op-amp?
2. What is the principle of operation of a zero-crossing detector?
3. What is a Schmitt trigger?
4. What circuit parameters determine the upper and lower threshold voltages of a Schmitt trigger?
5. What are the effects of hysteresis on output voltage?
6. What is the principle of operation of a square-wave generator?
7. Why is a square-wave generator called an astable multivibrator?
8. What is saturation of an op-amp?
9. What is the purpose of series resistors in the input terminals of an op-amp in a square-wave generator?
10. What circuit parameters determine the frequency of a square wave?
11. What is the principle of operation of a triangular-wave generator?
12. What circuit parameters determine the frequency of a triangular wave?
13. What is the principle of operation of a sawtooth-wave generator?
14. What circuit parameters determine the frequency of a sawtooth wave?
15. What is the duty cycle of a sawtooth wave?
16. What is a VCO?
17. What is the principle of operation of a VCO?
18. What circuit parameters determine the output frequency of a VCO?
19. What is the 555 timer?
20. What is a monostable multivibrator?
21. What advantages does the 555 timer connected as an astable multivibrator have over an op-amp astable multivibrator?
22. What circuit parameters determine the output frequency of the 555 timer connected as ramp generator?
23. What is a PLL?
24. What are the main components of a PLL?
25. What is the principle of operation of a PLL?
26. What is the free-running mode of a PLL?
27. What is the capture mode of a PLL?
28. What is the phase-lock mode of a PLL?
29. What is the capture range of a PLL?
30. What is the lock range of a PLL?
31. What are the relationships among the free-running frequency, capture frequency, and lock frequency of a PLL?
32. What are some applications of the TelCom 9400 series converter?
33. What is a sample-and-hold circuit?
34. What are the main parts of a sample-and-hold circuit?
35. What is a D/A converter?
36. What are the main parts of a D/A converter?
37. What is an A/D converter?
38. What are the main parts of an A/D converter?

Problems

The symbol **D** indicates that a problem is a design problem. The symbol **P** indicates that you can check the solution to a problem using PSpice/SPICE or Electronics Workbench.

► 16.2 & 16.4 Comparators and Schmitt Triggers

For Probs. 16.1 through 16.5, use comparator LM111 and $v_S = 10 \sin(2000\pi t)$ to plot the hysteresis characteristic using PSpice/SPICE.

- D** 16.1 Design a Schmitt trigger as in Fig. 16.7(a) so that $V_{th} = | +V_{th} | = | -V_{th} | = 5$ V. Assume $V_{sat} = | -V_{sat} | = 12$ V.
- P** 16.2 The parameters of the Schmitt trigger in Fig. 16.7(a) are $R_1 = 100 \Omega$ and $R_F = 47$ k Ω . Calculate the threshold voltages $+V_{th}$ and $-V_{th}$. Assume $V_{sat} = | -V_{sat} | = 12$ V.
- D** 16.3 Design an inverting Schmitt trigger with the reference voltage of Fig. 16.7(a) so that $V_{Ht} = -8$ V and $V_{Lt} = -4$ V. Assume $V_{sat} = | -V_{sat} | = 12$ V.
- D** 16.4 Design a noninverting Schmitt trigger as in Fig. 16.10(a) so that $V_{th} = | +V_{th} | = | -V_{th} | = 5$ V. Assume $V_{sat} = | -V_{sat} | = 12$ V.
- D** 16.5 Design a noninverting Schmitt trigger with the reference voltage of Fig. 16.11(a) so that $V_{Ht} = 8$ V and $V_{Lt} = 4$ V. Assume $V_{sat} = | -V_{sat} | = 12$ V.

► 16.5–16.7 Square-, Triangular-, and Sawtooth-Wave Generators

For Probs. 16.6 through 16.10, use op-amp LF411 to plot the output using PSpice/SPICE.

- D** 16.6 Design the square-wave generator shown in Fig. 16.16(a) so that $f_o = 2$ kHz. Assume $V_{sat} = | -V_{sat} | = 10$ V.
- P** 16.7 The parameters of the square-wave generator of Fig. 16.16(a) are $R_1 = 10$ k Ω , $R_F = 15$ k Ω , $R = 10$ k Ω , and $C = 0.047$ μ F. Calculate the output frequency f_o .
- D** 16.8 Design the triangular-wave generator shown in Fig. 16.19(a) so that $f_o = 2$ kHz and $V_{th} = 5$ V. Assume $V_{sat} = | -V_{sat} | = 12$ V.
- P** 16.9 The parameters of the triangular-wave generator of Fig. 16.19(a) are $R_1 = 10$ k Ω , $R_F = 40$ k Ω , $R = 10$ k Ω , and $C = 0.047$ μ F. Calculate the output frequency f_o .
- D** 16.10 Design the sawtooth-wave generator shown in Fig. 16.22(a) so that $f_o = 5$ kHz, $V_{th} = 5$ V, and the circuit has a duty cycle of $k = t_1/T = 0.4$. Assume $V_{sat} = | -V_{sat} | = 12$ V.

► 16.8 Voltage-Controlled Oscillators

- D** 16.11 (a) Design a VCO as shown in Fig. 16.25(c) that has a nominal frequency of $f_o = 10$ kHz. Assume $V_{CC} = 15$ V.
- (b) Calculate the modulation in the output frequencies if v_{CN} is varied by $\pm 10\%$.
- 16.12 The parameters of the VCO in Fig. 16.25(c) are $R_A = 2.5$ k Ω , $R_1 = R_B = 10$ k Ω , and $C = 0.01$ μ F.
- (a) Calculate the nominal frequency of the output waveform f_o .
- (b) Calculate the modulation in the output frequencies if v_{CN} is varied by $\pm 10\%$. Assume $V_{CC} = 12$ V.

► 16.9 The 555 Timer

For Probs. 16.13 through 16.20, use the 555D timer to plot the output by PSpice/SPICE.

- D** 16.13 Design a monostable multivibrator as in Fig. 16.27(a) so that $t_p = 2$ ms. Assume $V_{CC} = 15$ V.
- D** 16.14 Design an astable multivibrator as in Fig. 16.31(a) so that $k = 80\%$ and $f_o = 5$ kHz. Assume $V_{CC} = 15$ V.
- P** 16.15 The parameters of the astable multivibrator in Fig. 16.31(a) are $R_A = 2.2$ k Ω , $R_B = 3.9$ k Ω , and $C = 0.1$ μ F. Determine (a) the charging time t_c , (b) discharging time t_d , and (c) the free-running frequency f_o .
- D** 16.16 Design a square-wave generator as in Fig. 16.34 so that $k = 50\%$ and $f_o = 5$ kHz. Assume $V_{CC} = 15$ V.

- P** 16.17 The parameters of the square-wave generator in Fig. 16.34 are $R_A = 2.7 \text{ k}\Omega$, $R_B = 4.7 \text{ k}\Omega$, and $C = 1 \text{ }\mu\text{F}$. Determine (a) the charging time t_c , (b) the discharging time t_d , and (c) the free-running frequency f_o .
- D** **P** 16.18 Design a ramp generator as in Fig. 16.35(a) so that $k = 50\%$ and $f_o = 5 \text{ kHz}$. Assume $V_{CC} = 15 \text{ V}$, $V_{BE} = 0.7 \text{ V}$, and a transistor of $\beta_F = 100$.
- P** 16.19 The parameters of the ramp generator in Fig. 16.35(a) are $R = 10 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, $V_{BE} = 0.7 \text{ V}$, and a transistor of $\beta_F = 100$. Determine the free-running frequency f_o .
- D** **P** 16.20 Design the FSK modulator shown in Fig. 16.36(a) to produce frequencies of 1270 Hz and 1570 Hz corresponding to 1 (mark) and 0 (space), respectively.
- **16.10 Phase-Lock Loops**
- D** 16.21 Design a PLL as shown in Fig. 16.40(c) so that $f_o = 5 \text{ kHz}$ and $f_c = \pm 50 \text{ Hz}$. Assume $V_{CC} = -V_{EE} = 15 \text{ V}$.
- 16.22 The parameters of the PLL in Fig. 16.40(c) are $R_1 = 12 \text{ k}\Omega$, $C_1 = 0.01 \text{ }\mu\text{F}$, $C_2 = 10 \text{ }\mu\text{F}$, and $V_{CC} = -V_{EE} = 15 \text{ V}$. Determine (a) the free-running frequency f_o , (b) the lock frequency f_L , and (c) the capture range f_c .
- **16.11 Voltage-to-Frequency and Frequency-to-Voltage Converters**
- D** 16.23 Design a V/F converter as shown in Fig. 16.46 so that $f_o = 2.5 \text{ kHz}$ at $v_i = 5 \text{ V}$. The input voltage v_i can vary between 10 mV and 10 V. Assume $V_{DD} = -V_{SS} = 5 \text{ V}$.
- D** 16.24 Design an F/V converter as shown in Fig. 16.49 so that $V_O = 2.5 \text{ V}$ at $f_{in} = 10 \text{ kHz}$. The input frequency f_{in} can vary between 0 Hz and 20 kHz. Assume $V_{DD} = -V_{SS} = 5 \text{ V}$.
- **16.12 Sample-and-Hold Circuits**
- D** 16.25 Design the sample-and-hold circuit shown in Fig. 16.52(a) so that the drop is within 0.5%. The leakage current in the hold mode is 1 nA, and the hold voltage is $V_h = 5 \text{ V}$. The internal hold time is $t_h = 100 \text{ }\mu\text{s}$. Find the holding capacitance C_h .
- D** 16.26 Design the sample-and-hold circuit shown in Fig. 16.52(a) so that the output tracks the input within 0.5%. The internal hold time is $t_h = 100 \text{ ns}$. The input biasing current of the op-amp is $I_B = 10 \text{ nA}$. Assume $R_F = R_1 = 20 \text{ k}\Omega$ and $v_i = 5 \text{ V}$.
- D** 16.27 Design the sample-and-hold circuit shown in Fig. 16.52(a) so that the drop is within 0.5%. The internal hold time is $t_h = 0.1 \text{ ms}$, and the hold voltage is $V_h = 5 \text{ V}$. The input biasing current of the op-amp is $I_B = 200 \text{ nA}$. Assume $R_F = R_1 = 20 \text{ k}\Omega$.
- **16.13 Digital-to-Analog Converters**
- 16.28 A 10-bit D/A converter of type 2R ladder, as shown in Fig. 16.55(a), has an input of 00 1001 1001, and the reference voltage is 5 V. Find the analog output voltage V_O .
- 16.29 A D/A converter is to have a full-scale output of 5 V and a resolution of less than 20 mV. What is the bit size?
- 16.30 The 8-bit D/A converter shown in Fig. 16.55(a) is to have a full-scale output of 10 V with a reference voltage of 5 V. Find the values of R_F and R .
- **16.14 Analog-to-Digital Converters**
- 16.31 An 8-bit A/D converter has a reference voltage of 10 V. Find (a) the analog input corresponding to the binary outputs 1010 1010 and 0101 0101, (b) the binary output if $V_a = 3 \text{ V}$, and (c) the resolution of the converter.
- 16.32 Construct a table similar to Table 16.2 for a 4-bit A/D converter if $V_a = 5 \text{ V}$ with a reference voltage of 16 V.
- 16.33 Construct a table similar to Table 16.2 for an 8-bit A/D converter if $V_A = 4 \text{ V}$ with a reference voltage of 10 V.