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15.1 Introduction

So far, we have discussed separately the analysis and design of transistor amplifiers, differential amplifiers, and output stages. An operational amplifier normally consists of these stages. In this chapter, we will examine the internal circuitry of ten commercially available op-amps. Much of the circuitry will be closely related to that of other ICs. We will analyze in detail one of the oldest but most popular amplifiers, the LM741.

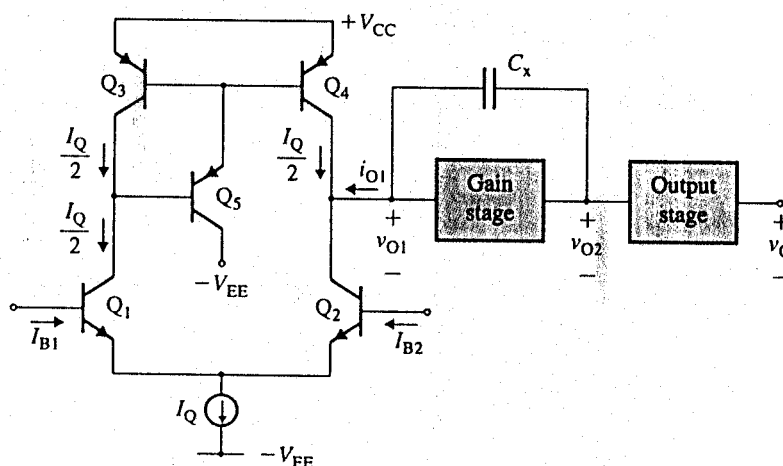
The learning objectives of this chapter are as follows:

- To understand the internal structure and types of op-amps and the effects of amplifier configurations on op-amp performance
- To study the parameters of the internal design that affect op-amp performance (i.e., offset voltage, offset current, and unity-gain frequency)
- To learn the typical values of performance parameters for different types of op-amps
- To analyze op-amp circuits to determine the dc biasing conditions and the performance parameters

15.2 Internal Structure of Op-Amps

The general configuration of an op-amp is shown in Fig. 15.1. All stages are direct coupled—that is, there are no coupling or bypass capacitors. Since capacitors and resistors of over 50 k Ω occupy large areas on IC chips and exhibit parasitic effects, they are usually

FIGURE 15.1
General configuration of
an op-amp



avoided in ICs. Therefore, op-amp circuits are designed using transistors with matching characteristics. Mismatches do exist, however, and cause offset voltages.

The voltage gain of each of the differential and gain stages is normally in the range from 300 to 1000. The output stage is an emitter follower, and its gain is unity. Thus, the overall open-loop voltage gain of an op-amp is on the order of 10^5 to 10^6 . The output stage provides a low output impedance so that it can drive a load with relatively low values of load resistance. It is normally operated in class AB mode to reduce crossover distortion. In general, BJT op-amps have a larger voltage gain, whereas FET op-amps have higher input resistances.

For stability of the op-amp, the phase shift of each stage is kept to a minimum. Since each stage contributes to the phase shift, the total number of stages is generally limited to three. A compensation capacitor C_x is normally connected across the second stage.

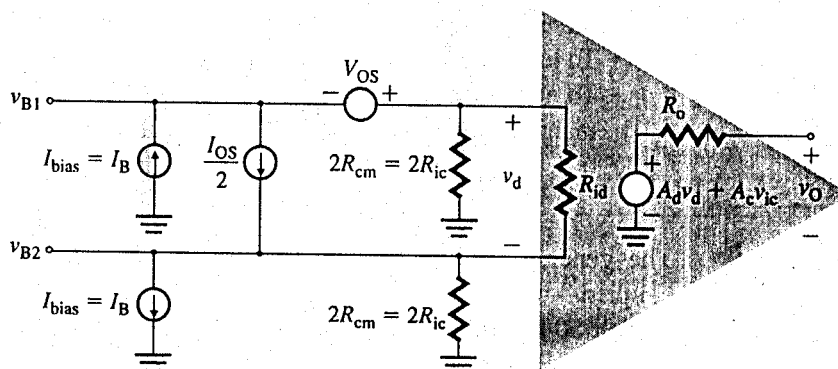
KEY POINT OF SECTION 15.2

- In general, an op-amp circuit consists of a differential input stage, a gain stage, an output stage, and protection circuitry. Each stage uses active biasing and an active load.

15.3 Op-Amp Parameters

Most op-amps contain a differential-coupled pair as an input stage. Practical op-amps exhibit characteristics that deviate significantly from the ideal characteristics. These deviations are discussed in detail in Chapter 6. Here we will consider some parameters that depend on the internal design of the op-amp. The effects of deviations from the ideal can be incorporated in the equivalent circuit of the op-amp, as shown in Fig. 15.2.

FIGURE 15.2
Equivalent circuit of an
op-amp



Input Biasing Current

The input biasing current I_B is defined as the average of the two dc input currents to the bases of Q_1 and Q_2 . That is,

$$I_B = \frac{I_{B1} + I_{B2}}{2} \quad (15.1)$$

$$\equiv \frac{I_C}{\beta_F} = \frac{I_Q}{2\beta_F} \quad (\text{for BJT input stage only}) \quad (15.2)$$

The polarity of I_B is shown for an *npn* transistor input stage in Fig. 15.2. For a *pnp* input stage, I_B would flow out of the amplifier terminals. Transistors in an ideal op-amp are assumed to have a large value of β_F , tending to infinity, and to draw zero dc input current. In a practical op-amp, however, β_F has a finite value. Thus, I_B has a small but finite value. The typical magnitudes of the biasing currents are 10 to 100 nA for BJT input devices and 1 to 10 pA for JFET input devices. This input biasing current will cause a small dc output voltage when the external input voltage is zero.

Input Offset Current

The dc input currents will be equal only if the two transistors have equal current gains (betas). However, even two theoretically identical transistors right next to each other on an IC chip will not be exactly identical. Geometrically identical devices on the same IC die typically display a mismatch that is normally distributed with a standard deviation of 5 to 10% of the mean value. This mismatch in the two biasing currents is random from circuit to circuit and is described by the input offset current I_{OS} , which is defined as the difference between the two base currents of the transistors:

$$I_{OS} = |I_{B1} - I_{B2}| \quad (15.3)$$

I_{OS} arises from mismatches in the area and β_F of the transistors. Beta and collector current values typically deviate by 10% and 1%, respectively. Thus, I_{OS} can be found approximately from

$$I_{OS} = (0.1 + 0.01)I_C/\beta_F = 0.11I_Q/2\beta_F = 0.055I_Q/\beta_F \quad (15.4)$$

Input Offset Voltage and Thermal Voltage Drift

Because of mismatches, an output voltage will exist even when the external input is zero. The differential voltage that must be applied to the input terminals of an amplifier to drive the output to zero is called the *input offset voltage* V_{OS} . This input offset voltage is a function of temperature. The rate of change of the input offset voltage V_{OS} per unit change in temperature is known as the *thermal voltage drift*, and it is expressed as

$$D_v = \frac{\Delta V_{OS}}{\Delta T} \quad (\text{in V/}^\circ\text{C}) \quad (15.5)$$

BJT Amplifiers The difference in the base-emitter voltages will cause an offset voltage. Using Eqs. (13.84) and (13.85), we can express this offset voltage as

$$v_{BE1} - v_{BE2} = V_T \left[\ln \frac{i_{C1}}{I_{S1}} - \ln \frac{i_{C2}}{I_{S2}} \right] = V_T \ln \left(\frac{i_{C1}}{I_{S1}} \times \frac{I_{S2}}{i_{C2}} \right) \quad (15.6)$$

Since the mismatch in the collector current is generally small (that is, $i_{C1} \approx i_{C2}$), we can find the input offset voltage V_{OS} from

$$V_{OS} = v_{BE1} - v_{BE2} = V_T \ln \left(\frac{I_{S2}}{I_{S1}} \right) \quad (15.7)$$

Thus, the saturation current I_S is the prime contributing factor to V_{OS} in a BJT amplifier and is proportional to the transistor base width W_B . Its value can vary from one transistor

to another. Assuming that $W_{B1} = W_B$ and $W_{B2} = W_B + \Delta W_B$ are the base widths of transistors Q_1 and Q_2 , respectively, Eq. (15.7) becomes

$$V_{OS} = V_T \ln \left(\frac{W_B + \Delta W_B}{W_B} \right) = V_T \ln \left(1 + \frac{\Delta W_B}{W_B} \right) \quad (15.8)$$

For $W_B \gg \Delta W_B$, which is usually the case, Eq. (15.8) can be approximated by

$$V_{OS} = V_T \left(\frac{\Delta W_B}{W_B} \right) \quad (15.9)$$

The beta of a transistor is inversely proportional to the base width W_B . Therefore, any change in W_B will cause an almost equal change in beta. That is, $\Delta \beta_F / \beta_F = \Delta W_B / W_B$. Since the change in the base width is generally within 10%, the offset voltage can be found approximately from

$$V_{OS} = 0.1 V_T \quad (15.10)$$

For BJT input devices, this value is typically 2 to 5 mV (for compound devices) and can often be nullified with an external potentiometer.

The ratio $\Delta W_B / W_B$ is relatively independent of temperature. Since $V_T = kT/q$, $dV_T/dT = k/q = V_T/T$. Thus, we can find the thermal drift from Eq. (15.9) as follows:

$$D_v = \frac{dV_{OS}}{dT} = \frac{V_T}{T} \left(\frac{\Delta W_B}{W_B} \right) \equiv \frac{V_{OS}}{T} \quad (15.11)$$

For example, if $V_{OS} = 2.6$ mV and $T = 25^\circ\text{C} = 273 + 25 = 298$ K,

$$D_v = 2.6 \text{ mV} / 298 = 8.72 \text{ } \mu\text{V/K}$$

JFET Amplifiers From Eq. (13.133), the transconductance of a JFET is given by

$$g_m = -\frac{2}{V_p} \sqrt{I_D I_{DSS}} \quad (15.12)$$

If the drain currents of JFETs differ from the quiescent value by a small amount ΔI_D , then a small gate differential voltage (that is, $\Delta V_{GS} = V_{OS}$) must be applied between the two gates to cancel the difference ΔI_D . Thus,

$$\Delta I_D = g_m \Delta V_{GS} = g_m V_{OS}$$

which gives the input offset voltage V_{OS} as

$$V_{OS} = -\frac{\Delta I_D}{\sqrt{I_D I_{DSS}}} \left(\frac{V_p}{2} \right) \quad (15.13)$$

If the transistors are biased at $V_{GS} = 0$, then $I_D = I_{DSS}$ and Eq. (15.13) becomes

$$V_{OS} = -\left(\frac{\Delta I_{DSS}}{I_{DSS}} \right) \left(\frac{V_p}{2} \right) \quad (15.14)$$

The variation in the drain current I_{DSS} is generally within 1%. Thus, V_{OS} can be found approximately from

$$V_{OS} \approx -0.005 V_p \quad (15.15)$$

Since $|V_p| \gg V_T$, the offset voltage of JFET amplifiers is generally considerably larger than that of BJT amplifiers.

For JFETs, the ratio $\Delta I_{DSS}/I_{DSS}$ is relatively independent of temperature. However, the pinch-down voltage V_p is primarily frequency dependent. Thus, from Eq. (15.14), we get the thermal drift D_v as

$$D_v = \frac{dV_{OS}}{dT} = -\left(\frac{\Delta I_{DSS}}{2I_{DSS}}\right)\left(\frac{dV_p}{dT}\right) \quad (15.16)$$

$$= \left(\frac{V_{OS}}{V_p}\right)\left(\frac{dV_p}{dT}\right) \quad (15.17)$$

Since dV_p/dT is generally about 1 mV/°C, Eq. (15.17) becomes

$$D_v = \left(\frac{V_{OS}}{V_p}\right) \quad (\text{in mV/°C}) \quad (15.18)$$

For example, if $V_p = -4$ V, then $V_{OS} \equiv 0.005 \times 4 = 20$ mV and $D_v = 0.02$ mV/4 = 5 μ V/°C.

CMOS Amplifiers From Eq. (13.158), the transconductance of a MOSFET is given by

$$g_m = 2K_P(V_{GS} - V_t) = \frac{2I_D}{V_{GS} - V_t} \quad (15.19)$$

If ΔI_D is the difference between the drain currents of MOSFETs, an input offset voltage $\Delta V_{GS} = V_{OS}$ must be applied between the two gates to cancel the difference. Any increase in ΔV_{GS} will cause an increase in ΔI_D . However, any differential increase ΔV_t in the threshold voltages will cause a decrease in drain current. That is,

$$\Delta I_D = \frac{g_m}{2}(\Delta V_{GS} - \Delta V_t) = \frac{g_m}{2}(V_{OS} - \Delta V_t)$$

which gives the input offset voltage V_{OS} as

$$V_{OS} = \Delta V_t + \frac{\Delta I_D}{I_D}(V_{GS} - V_t) \quad (15.20)$$

The ratio $\Delta I_D/I_D$ will depend on any change in the W/L ratio of the MOSFET. Thus, Eq. (15.20) can be written in terms of the W/L ratio:

$$V_{OS} = \Delta V_t + \frac{\Delta(W/L)}{W/L}(V_{GS} - V_t) \quad (15.21)$$

In CMOS amplifiers, the value of ΔV_t alone, which is absent in BJTs, can be as high as 2 mV—a magnitude larger than V_{OS} for BJTs. The value of $(V_{GS} - V_t)$ is usually much greater than V_T . Thus, the offset voltage of CMOS amplifiers will generally be considerably larger than that of BJT amplifiers. In order to have a low value of V_{OS} , MOSFETs should be operated with a low value of $(V_{GS} - V_t)$.

For MOSFET amplifiers, thermal drift cannot be correlated with the offset voltage. Its magnitude will be on the same order as that for JFETs. The thermal drift of $\Delta V_t/dT$ can be quite significant.

The CMRR, which is defined as the ratio of the differential voltage gain to the common-mode voltage gain, may also be defined as the change in input offset voltage per unit change in common-mode voltage. Let $v_{ic} = 0$, and apply v_{id} to drive the output voltage to zero. v_{id} should thus be equal to the input offset voltage V_{OS} . If we keep

v_{id} constant and increase v_{ic} by an amount Δv_{ic} , the output voltage will change by an amount

$$\Delta v_O = A_c \Delta v_{ic} \quad (15.22)$$

To drive the output voltage to zero, we have to change v_{id} by an amount Δv_{id} , where

$$\Delta v_{id} = \frac{\Delta v_O}{A_d} = \frac{A_c \Delta v_{ic}}{A_d} = \Delta V_{OS} \quad (15.23)$$

Equation (15.23) indicates that any change in v_{ic} causes a corresponding change in V_{OS} . From Eq. (15.23), we get

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{\Delta v_{ic}}{\Delta v_{id}} \bigg|_{v_o=0} = \frac{\Delta v_{ic}}{\Delta V_{OS}} = \frac{\delta v_{ic}}{\delta V_{OS}} \bigg|_{v_o=0} \quad (15.24)$$

which shows that the input offset voltage is dependent on the CMRR and the common-mode signal. For $\text{CMRR} = 10^5$ (or 100 dB) and $\Delta v_{ic} = 15$ V, the change in the input offset voltage will be $\Delta V_{OS} = 150 \mu\text{V}$.

Input Resistance

The input resistance for an FET input stage is very high, in the range of 10^9 to $10^{12} \Omega$. For a BJT input stage, however, the input resistance is typically in the range of 100 k Ω to 1 M Ω . Usually, the voltage gain is large enough that this input resistance has little effect on the circuit performance. In some differential amplifiers, a compound transistor configuration known as a *Darlington pair* is used to give a much higher input resistance and a much lower input biasing current than a single transistor would provide. A Darlington pair is shown in Fig. 15.3. The effective base-emitter voltage is

$$\begin{aligned} V_{BE} &= V_{BE1} + V_{BE2} = V_T \ln \left(\frac{I_{C1}}{I_{S1}} \right) + V_T \ln \left(\frac{I_{C2}}{I_{S2}} \right) \\ &= V_T \ln \left(\frac{I_{C1} I_{C2}}{I_{S1} I_{S2}} \right) \end{aligned} \quad (15.25)$$

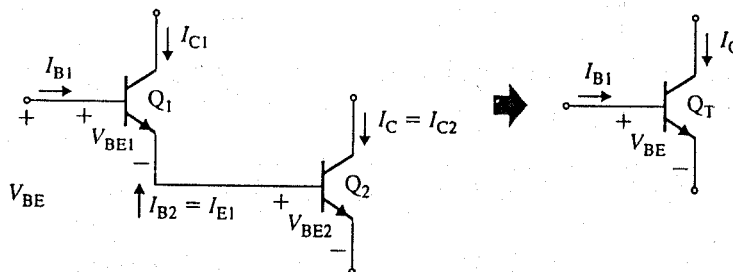
Since $I_C = I_{C2} = \beta_F I_{C1}$, Eq. (15.25) becomes

$$V_{BE} = V_T \ln \left(\frac{I_C^2}{\beta_F I_{S1} I_{S2}} \right) \quad (15.26)$$

Solving for I_C , we get

$$\begin{aligned} I_C &= \sqrt{\beta_F I_{S1} I_{S2}} \exp \left(\frac{V_{BE}}{2V_T} \right) \\ &= I_S \exp \left(\frac{V_{BE}}{V_T'} \right) \end{aligned} \quad (15.27)$$

FIGURE 15.3
Darlington pair



where $I_S = \sqrt{\beta_F I_{S1} I_{S2}}$ = effective saturation current

$V_T' = 2V_T$ = effective thermal voltage

The collector current I_C can be related to I_{B1} by

$$\begin{aligned} I_C &= I_{C2} = \beta_F I_{B2} = (1 + \beta_F) I_{C1} = \beta_F (1 + \beta_F) I_{B1} \\ &\equiv \beta_F^2 I_{B1} \end{aligned} \quad (15.28)$$

Thus, the effective input resistance of the compound pair is given by

$$r_\pi' = \frac{V_T'}{I_{B1}} \equiv \beta_F^2 \frac{2V_T}{I_C} \quad (15.29)$$

which will be $2\beta_F$ times greater than that for a single device. For a single transistor, $r_\pi' = 2\beta_F r_\pi$. Thus, if $I_C = 200 \mu\text{A}$, $\beta_F = 100$, and $V_T = 26 \text{ mV}$,

$$r_\pi = \beta_F V_T / I_C = 100 \times 26 \text{ mV} / 200 \mu\text{A} = 13 \text{ k}\Omega$$

for a single transistor and

$$r_\pi' = 100^2 \times 2 \times 26 \text{ mV} / 200 \mu\text{A} = 2.6 \text{ M}\Omega$$

for a Darlington pair. The input offset voltage V_{OS} , however, will increase (generally $\sqrt{2}$ times) as a result of the increase in the effective thermal voltage.

EXAMPLE 15.1

Finding the effective parameters of a Darlington pair The Darlington pair shown in Fig. 15.4 is biased in such a way that the collector biasing current I_{C2} of Q_2 is 1 mA. The current gains of the two transistors are the same, $\beta_{F1} = \beta_{F2} = \beta_F = 100$, and the Early voltage is $V_A = 75 \text{ V}$. Calculate (a) the effective input resistance r_π , (b) the effective transconductance g_m , (c) the effective current gain $\beta_{F(\text{eff})}$, and (d) the effective output resistance r_o .

FIGURE 15.4 Two transistors connected as a Darlington pair

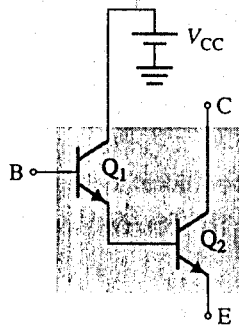
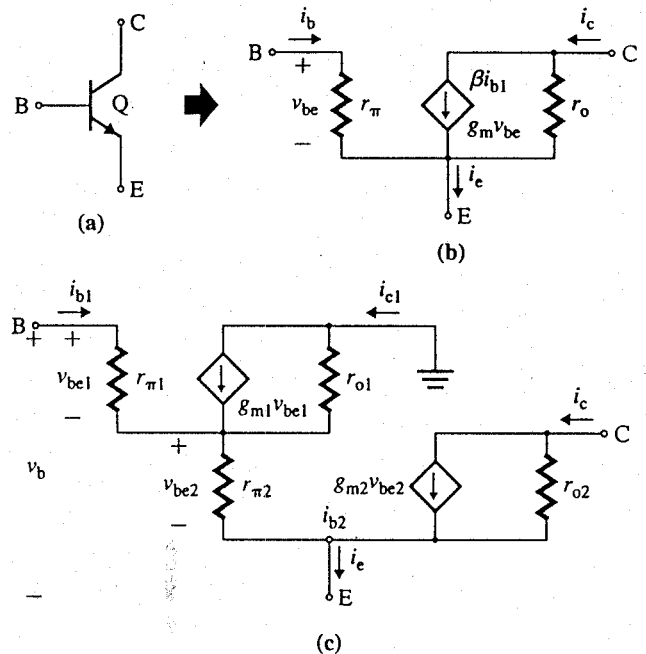


FIGURE 15.5 Equivalent model of Darlington pair



SOLUTION

The two transistors in Fig. 15.4 can be replaced by an equivalent transistor, shown in Fig. 15.5(a), which may be regarded as the subcircuit of the two transistors and can be modeled by the circuit in Fig. 15.5(b). Replacing each transistor by its model gives the small-signal equivalent circuit of a

Darlington pair shown in Fig. 15.5(c). Let us assume that $r_o \approx \infty$. The two collector and base currents of the transistors will be different. According to Eq. (5.8), r_π depends inversely on the collector current. Thus, the small-signal input resistances $r_{\pi 1}$ and $r_{\pi 2}$ of the transistors will be different. Assuming we have $V_T = 25.8$ mV,

$$\begin{aligned} g_{m2} &= I_{C2}/V_T = 1 \text{ mA}/25.8 \text{ mV} = 38.76 \text{ mA/V} \\ r_{\pi 2} &= \beta_F/g_{m2} = \beta_F V_T/I_{C2} = 100 \times 25.8 \text{ mV}/1 \text{ mA} = 2.58 \text{ k}\Omega \\ I_{B2} &= I_{E1} = I_{C2}/\beta_F = 1 \text{ mA}/100 = 10 \text{ }\mu\text{A} \\ r_{o2} &= V_A/I_{C2} = 75/(1 \text{ mA}) = 75 \text{ k}\Omega \\ I_{C1} &= I_{B2}\beta_F/(1 + \beta_F) = 10 \text{ }\mu\text{A} \times 100/(1 + 100) = 9.9 \text{ }\mu\text{A} \\ g_{m1} &= I_{C1}/V_T = 9.9 \text{ }\mu\text{A}/25.8 \text{ mV} = 383.7 \text{ }\mu\text{A/V} \\ r_{\pi 1} &= \beta_F/g_{m1} = 100/(383.7 \text{ }\mu\text{A}) = 260.6 \text{ k}\Omega \\ r_{o1} &= V_A/I_{C1} = 75/(9.9 \text{ }\mu\text{A}) = 7.6 \text{ M}\Omega \end{aligned}$$

(a) Figure 15.5(c) is similar to Fig. 5.11(b). Thus, Eq. (5.28) can be applied to Fig. 15.5(c) if r_π and R_E are replaced by $r_{\pi 1}$ and $r_{\pi 2}$, respectively. Replacing R_E in Eq. (5.28) with $r_{\pi 2}$ gives the input resistance

$$\begin{aligned} r_\pi &= r_{\pi 1} + (1 + \beta_F)r_{\pi 2} \parallel r_{o1} \\ &= 260.6 \text{ k} + (1 + 100) \times 2.58 \text{ k} \parallel 7.6 \text{ M}\Omega = 521.2 \text{ k}\Omega \end{aligned} \quad (15.30)$$

(b) The voltage v_{be2} in Fig. 15.5(c) is identical to v_o in Fig. 5.11(b) provided $r_{\pi 2}$ is substituted for R_E . Thus, v_{be2} can be related to the input voltage v_b by Eq. (5.35):

$$v_{be2} = \frac{(1 + \beta_{F1})r_{\pi 2}}{r_{\pi 1} + (1 + \beta_{F1})r_{\pi 2}} v_b \quad (15.31)$$

The collector current i_c of the second transistor can be found from

$$i_c = g_{m2}v_{be2} = g_{m2} \frac{(1 + \beta_{F1})r_{\pi 2}}{r_{\pi 1} + (1 + \beta_{F1})r_{\pi 2}} v_b$$

which gives the equivalent transconductance g_m as

$$g_m = \frac{i_c}{v_b} = g_{m2} \frac{(1 + \beta_{F1})r_{\pi 2}}{r_{\pi 1} + (1 + \beta_{F1})r_{\pi 2}} = g_{m2} \frac{1}{1 + r_{\pi 1}/(1 + \beta_{F1})r_{\pi 2}} \quad (15.32)$$

Since the emitter current I_{E1} of Q_1 is equal to the base current I_{B2} of Q_2 , the biasing base current I_{B2} of Q_2 will be related to the biasing base current I_{B1} of Q_1 by

$$I_{B2} = I_{E1} = (1 + \beta_{F1})I_{B1} \approx (1 + \beta_{F1})I_{B1}$$

According to Eq. (5.8), r_π is inversely proportional to the biasing base current I_B . Thus, $r_{\pi 1}$ and $r_{\pi 2}$ will be related by $r_{\pi 1} = (1 + \beta_{F1})r_{\pi 2}$. Therefore, Eq. (15.32) can be simplified to

$$\begin{aligned} g_m &= \frac{g_{m2}}{2} \\ &= 38.76/2 = 19.38 \text{ mA/V} \end{aligned} \quad (15.33)$$

(c) The collector current i_{c2} of Q_2 can also be written as

$$i_c = \beta_{F2}i_{b2}$$

Since $i_{b2} = (1 + \beta_{F1})i_{b1}$,

$$i_c = \beta_{F2}i_{b2} = \beta_{F2}(1 + \beta_{F1})i_{b1}$$

Thus, the effective current gain $\beta_{F(\text{eff})}$, which is the ratio of i_c to i_{b1} , is

$$\begin{aligned} \beta_{F(\text{eff})} &= \frac{i_c}{i_{b1}} = \beta_{F2}(1 + \beta_{F1}) \\ &= \beta_{F2}(1 + \beta_{F1}) = 100 \times (1 + 100) = 10100 \end{aligned} \quad (15.34)$$

(d) The effective output resistance r_o is

$$\begin{aligned} r_o &= r_{o2} \\ &= 75 \text{ k}\Omega \end{aligned} \quad (15.35)$$

Thus, a model that can represent the two CC or CE transistors is shown in Fig. 15.5(b).

Output Resistance

The output stage is usually an emitter follower in class AB operation, and hence it gives a low output resistance, on the order of 40 to 100 Ω . This resistance is low enough that it does not strongly affect performance. If $I_{C(\text{out})}$ is the collector biasing current of the output stage, then r_π of the output transistor becomes $r_\pi = \beta_F V_T / I_{C(\text{out})}$, which, if converted to the emitter terminal, will give approximately the output resistance of the op-amp. That is,

$$R_{\text{out}} = \frac{\beta_F V_T}{I_{C(\text{out})}(1 + \beta_F)} \equiv \frac{V_T}{I_{C(\text{out})}} \quad (15.36)$$

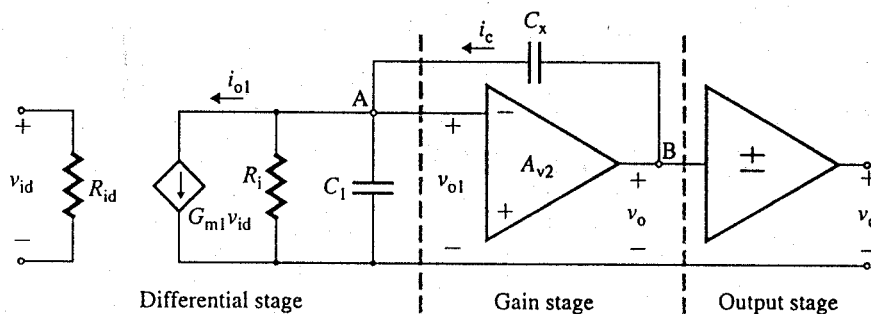
The collector biasing current of the output stage (which is in mA) is generally much greater than that of the differential stage (which is in μA). For example, if $\beta_F = 100$, $V_T = 26 \text{ mV}$, and $I_{C(\text{out})} = 1 \text{ mA}$, $R_{\text{out}} = 26 \text{ mV} / 1 \text{ mA} = 26 \Omega$.

Frequency Response

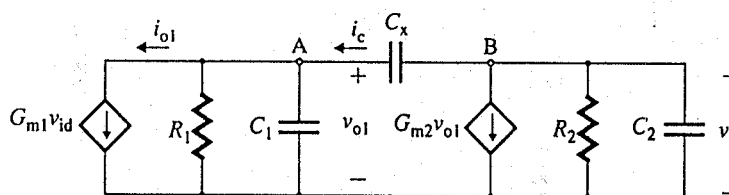
Because of the parasitic capacitances and the minority carrier charge storage in the devices within the op-amps, the voltage gain decreases at high frequency. The frequency at which the open-loop voltage gain falls to unity is defined as the *unity-gain bandwidth*, and it is in the range of 1 to 20 MHz. The differential stage in Fig. 15.1 can be represented by a voltage-controlled current source, as shown in Fig. 15.6(a). C_1 is the effective capacitance due to the output capacitance of the differential stage and the input capacitance of the second stage. R_1 is the effective resistance due to the output resistance of the differential stage and the input resistance of the second stage. G_{m1} is the transconductance of the differential stage.

The second stage generally has a common-emitter or common-source configuration with an active load for a large voltage gain. It can also be represented by another voltage-controlled current source, as shown in Fig. 15.6(b). G_{m2} is the transconductance of the sec-

FIGURE 15.6
High-frequency
equivalent circuit of an
op-amp



(a) Small-signal equivalent circuit of op-amp



(b) Small-signal high-frequency equivalent circuit

ond stage. C_2 and R_2 are the effective capacitance and the output resistance of the second stage, respectively. A_{v2} is the voltage gain of the second stage and is negative—that is, $A_{v2} = -G_{m2}R_2$.

The gain of the output stage is generally unity: $A_{v3} = 1$. Since the gain of the second stage is negative, the capacitance C_x will exhibit Miller's effect and split the poles. Also, C_x will influence both the frequency response and the slew rate considerably. From Eqs. (10.126) and (10.127), we can find the new poles:

$$\omega_{p1} \approx \frac{1}{g_{m2}C_xR_1R_2} \quad (15.37)$$

$$\omega_{p2} \approx \frac{g_{m2}C_x}{C_1C_2 + C_x(C_1 + C_2)} \quad (15.38)$$

If $C_x \gg C_1$ and C_2 , Eq. (15.38) can be approximated by

$$\omega_{p2} \approx \frac{g_{m2}C_x}{C_x(C_1 + C_2)} = \frac{g_{m2}}{C_1 + C_2} \quad (15.39)$$

The first pole is due to the Miller capacitance

$$C_M = C_x(1 + g_{m2}R_2) \equiv C_xg_{m2}R_2$$

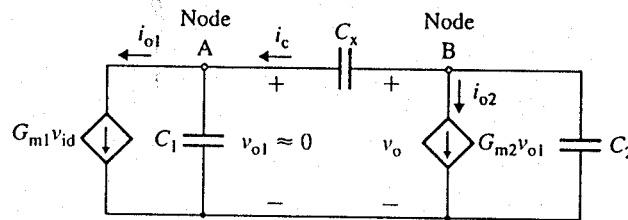
which is much larger than C_1 . To make ω_{p1} act as the unity-gain frequency ω_u , we can select the appropriate value of C_x . Since the values of C_1 and C_2 are small, the second pole ω_{p2} will become very large and move to the left, provided the value of g_{m2} is large enough.

Effects of C_x on Unity-Gain Bandwidth In order to determine the effect of C_x on the bandwidth, let us consider Fig. 15.7, which is a simplified version of Fig. 15.6(b) in which R_1 and R_2 are treated as open-circuited over the frequency range of interest. Under these assumptions, ω_{p1} moves to the extreme left—that is, $\omega_{p1} \approx 0$ —and does not give the unity-gain bandwidth. Using KCL at the input node of Fig. 15.7, we can write the node voltages as

$$(v_o - v_{o1})(j\omega C_x) = G_{m1}v_{id} + v_{o1}(j\omega C_1) \quad (15.40)$$

where $G_{m1} = I_Q/2V_T$ is the transconductance of the differential stage.

FIGURE 15.7
Simplified high-frequency
equivalent circuit of an
op-amp



Substituting $v_o = -A_{v2}v_{o1}$ (that is, $v_{o1} = -v_o/A_{v2}$) into Eq. (15.40) and simplifying, we get the overall voltage gain A_o :

$$A_o(j\omega) = \frac{v_o}{v_{id}} = \frac{G_{m1}}{(1 + 1/A_{v2})(j\omega C_x) + (j\omega C_1)/A_{v2}} \quad (15.41)$$

$$= \frac{G_{m1}/(j\omega C_x)}{(1 + 1/A_{v2}) + (C_1/C_x)/A_{v2}} \quad (15.42)$$

For $A_{v2} \gg 1$, which is usually the case, Eq. (15.42) can be simplified to

$$A_o(j\omega) = \frac{G_{m1}}{j\omega C_x} \quad (15.43)$$

At the unity-gain frequency ω_u , $|A(j\omega)| = 1$. Thus, ω_u is given by

$$\omega_u = \frac{G_{m1}}{C_x} \quad (15.44)$$

which gives the corresponding frequency (that is, the unity-gain bandwidth) f_u as

$$f_u = \frac{G_{m1}}{2\pi C_x} \quad (15.45)$$

$$= \frac{I_Q}{4\pi V_T C_x} \quad (15.46)$$

Thus, f_u is directly proportional to the biasing current I_Q of the differential stage and inversely proportional to the compensating capacitance C_x . A specific value of C_x is purposely added to the circuit, either on the chip for compensated op-amps or as an external capacitor, in order to set the desired value of f_u . For example, if $I_Q = 20 \mu\text{A}$, $V_T = 26 \text{ mV}$, and $C_x = 50 \text{ pF}$, we get $f_u = 1.22 \text{ MHz}$.

Effects of C_x on Zeros The capacitance C_x also has a Miller's effect on the output side of the second stage, given by

$$C_N = C_x \left(1 + \frac{1}{g_{m2} R_2} \right) \approx C_x$$

and introduces a right-half-plane zero on the transfer function. The zero ω_z can be found from Fig. 15.8 by making the output voltage $v_o \equiv 0$, as shown in Fig. 15.8(a). We get

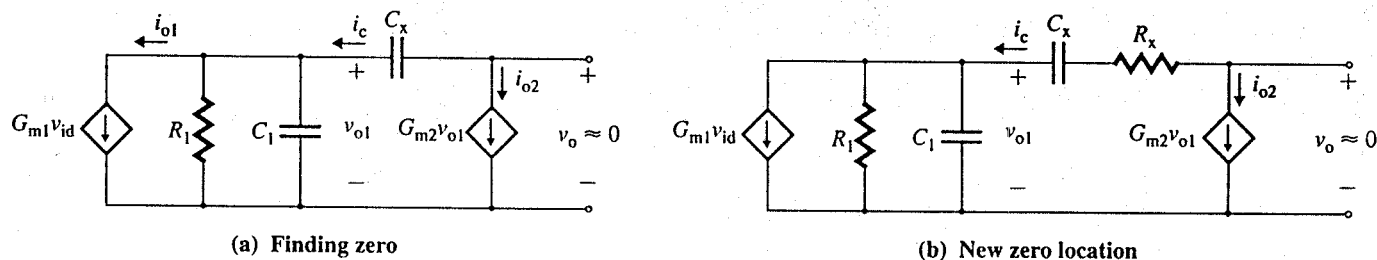
$$G_{m2} v_{o1} = (v_{o1} - v_o)(j\omega C_x) = v_{o1}(j\omega C_x)$$

which gives the zero frequency ω_z as

$$\omega_z = \frac{G_{m2}}{C_x} \quad (15.47)$$

If G_{m2} is large, which is usually the case for BJT amplifiers, then the zero will be at a very high frequency. However, if G_{m2} is of the same magnitude as G_{m1} , which is generally the case for CMOS amplifiers, the zero frequency will be close to the unity-gain frequency ω_u .

FIGURE 15.8 Equivalent circuit for determining zeros



Since a zero introduces a phase shift, the phase margin of the amplifier will be decreased, affecting the amplifier stability. However, it is possible to remedy the stability problem by adding a resistance R_x in series with C_x , as shown in Fig. 15.8(b). The combination of R_x and C_x can move the zero and make ω_z a very large frequency. The zero frequency ω_z can be found by making the output voltage $v_o \equiv 0$. That is,

$$G_{m2} v_{o1} = (v_{o1} - v_o) \left(j\omega C_x + \frac{1}{R_x} \right) = v_{o1} \left(j\omega C_x + \frac{1}{R_x} \right)$$

which gives the new zero frequency ω_z as

$$\omega_z = \frac{1}{C_x(1/G_{m2} - R_x)} \quad (15.48)$$

Thus, by selecting $R_x = 1/G_{m2}$, we can make the zero frequency ω_z infinite. It is important to note that, by making $R_x > 1/G_{m2}$, we can locate the zero frequency at the negative real axis, which will increase the phase margin.

According to Eq. (15.39), the second pole ω_{p2} may be close to the unity-gain frequency ω_u for a low value of g_{m2} . As a result, ω_{p2} may introduce an appreciable phase shift and thus decrease the phase margin. This problem can be resolved by increasing the value of C_x in order to split the poles further.

Slew Rate

Op-amps are limited by the *slew rate* (SR), which specifies the maximum rate at which the output voltage can change without introducing any significant amount of distortion. That is, $SR = (dv_o/dt)_{\max}$. Like the unity-gain frequency, the SR depends on the capacitance C_x . Figure 15.7 illustrates that the current i_c through the capacitor is related to the output voltage v_o by

$$\begin{aligned} i_c &= C_x \frac{d}{dt} (v_o - v_{o1}) \\ &= C_x \frac{d}{dt} \left(v_o + \frac{v_o}{A_{v2}} \right) \end{aligned} \quad (15.49)$$

(since $v_{o1} = -v_o/A_{v2}$), which gives dv_o/dt as

$$\frac{dv_o}{dt} = \frac{i_c}{C_x(1 + 1/A_{v2})} \quad (15.50)$$

Let us assume that $A_{v2} \gg 1$ and that i_c can be approximated by the output current of the differential amplifier (that is, $i_c = i_{o1} = G_{m1}v_{id}$). Then Eq. (15.50) can be approximated by

$$\frac{dv_o}{dt} \equiv \frac{i_c}{C_x} \equiv \frac{i_{o1}}{C_x} \quad (15.51)$$

Consider the unity-gain follower shown in Fig. 15.9(a). If a step input $v_I = V_m$ (say, 10 V) is applied to it, in zero time the output will not change, as shown in Fig. 15.9(b). Thus, V_m will appear as the differential voltage between the two input terminals, and the differential stage in Fig. 15.1 will be overdriven. Transistors Q_1 and Q_3 in

FIGURE 15.9 Unity-gain follower

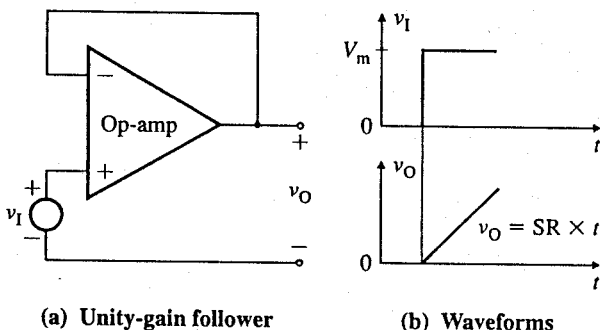


FIGURE 15.10 Integrating model of an op-amp

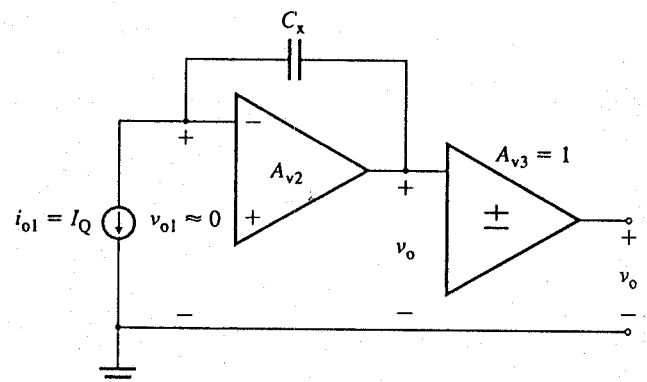


Fig. 15.1 will carry the whole biasing current I_Q , and transistor Q_4 will be cut off. Q_4 , however, is the mirror of Q_3 , and it will produce a current of I_Q , which will flow into the second stage.

The biasing current limits the maximum value of the output current i_{o1} of the differential stage to the value I_Q in one direction and the value $-I_Q$ in the other direction. That is, $i_{o1(\max)} = \pm I_Q$. Thus, the slew rate corresponding to $i_{o1(\max)}$ is given by

$$\text{SR} = \left. \frac{dv_o}{dt} \right|_{\max} \equiv \frac{i_{o1(\max)}}{C_x} \equiv \pm \frac{I_Q}{C_x} \quad (15.52)$$

Like the unity-gain frequency f_u , the slew rate is directly proportional to I_Q and inversely proportional to C_x . If the gain of the second stage is large, then the op-amp behaves as an integrator, as shown in Fig. 15.10.

Relation Between SR and f_u Substituting $I_Q = 4\pi V_T C_x f_u$ from Eq. (15.46) into Eq. (15.52), we can relate the positive SR (known simply as SR) to f_u . That is,

$$\text{SR} = \frac{4\pi V_T C_x f_u}{C_x} = 4\pi V_T f_u \quad (15.53)$$

or

$$f_u = \frac{\text{SR}}{4\pi V_T} \quad (15.54)$$

Thus, there is a direct relation between the slew rate and the unity-gain frequency of an op-amp. For example, if $I_Q = 20 \mu\text{A}$, $V_T = 26 \text{ mV}$, and $C_x = 50 \text{ pF}$, then $f_u = 1.22 \text{ MHz}$ and

$$\text{SR} = I_Q/C_x = 20 \mu\text{A}/50 \text{ pF} = 0.4 \text{ V}/\mu\text{s}$$

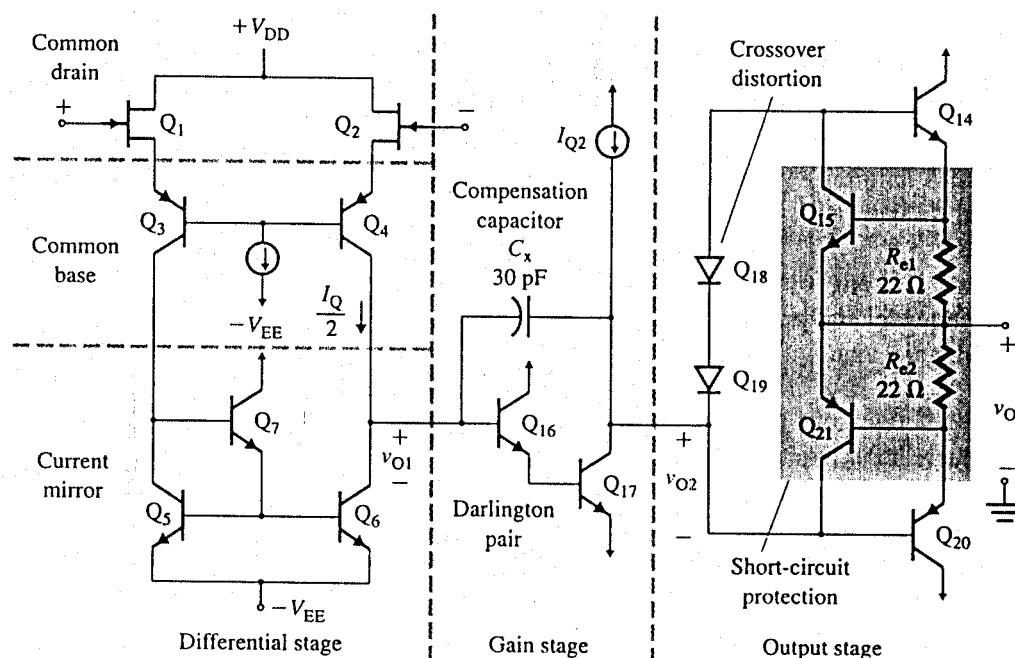
KEY POINTS OF SECTION 15.3

- The input offset voltage of FET amplifiers is considerably higher than that of BJT amplifiers. This difference is due to mismatches in base widths for BJTs, in I_{DSS} and V_p for JFETs, and in V_t and W/L for MOSFETs.
- A Darlington BJT pair is commonly used to provide high input resistance, low input base current, and high current gain.
- The unity-gain frequency f_u depends directly on the biasing current I_Q of the differential stage and inversely on the compensation capacitance C_x . The slew rate SR is directly proportional to f_u .
- If the transconductance of the gain stage is on the same order as that of the first stage, the zero frequency will be close to the unity-gain frequency and the phase margin will be reduced. A resistor R_x is usually connected in series with C_x to move the zero frequency to infinity.

15.4 JFET Op-Amps

JFET op-amps are generally hybrid-type amplifiers, using a pair of JFET transistors for the input stage differential amplifier and bipolar transistors for the rest of the circuit. Thus, JFET op-amps are often called BiFETs. This configuration allows a high input resistance and low input biasing currents while giving high gain through bipolar transistors. We will consider four examples.

FIGURE 15.11
Simplified schematic for
op-amp LH0022
(Courtesy of National
Semiconductor, Inc.)



JFET Op-Amp LH0022

The simplified schematic of the LH0022 op-amp is shown in Fig. 15.11. The LH0022 is designed to operate from a ± 15 -V power supply. It is capable of a peak output voltage swing of about 12 V into a 1-k Ω load over the entire frequency range of 1 MHz. The circuit can be divided into a differential stage, a gain stage, an output stage, overload protection, and a dc biasing circuit. Some parameters of the LH0022 are listed in Table 15.1.

Differential Stage The differential input stage consists of Q_1 through Q_4 . Transistors Q_1 and Q_2 are n -channel JFETs that operate in a common-drain (or source-follower) configuration. These JFETs drive transistors Q_3 and Q_4 , which operate in a common-base configuration. The current mirror, consisting of transistors Q_5 , Q_6 , and Q_7 , acts as the active load.

The combination of common-drain and common-base configurations provides a very high input resistance and a very low input biasing current from the JFETs while giving a large voltage gain from the BJTs. Also, the common-drain configuration performs

TABLE 15.1
Parameters of op-amp
LH0022

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 15	V
Input offset voltage V_{OS}		6.0	20	mV
Thermal drift D_v		10		$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		15	50	pA
Input offset current I_{OS}		2	10	pA
Differential input resistance R_{id}		10^{12}		Ω
Common-mode input resistance R_{ic}		10^{12}		Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.0		pF
Open-loop voltage gain A_o	25	100		V/mV
Common-mode rejection ratio CMRR	70	80		dB
Unity-gain bandwidth f_u		1.0		MHz
Slew rate SR	1.0	3.0		V/ μs
Power supply rejection ratio PSRR	70	80		dB

the function of shifting voltage levels toward the negative supply voltage $-V_{EE}$ so that the output signal can be shifted upward in the positive direction in the following stages. Note that the dc level of the output voltage of this stage will be approximately

$$-V_{EE} + V_{BE16} + V_{BE17} \approx -V_{EE} + 1.2 \text{ V}$$

Gain Stage The gain stage has the common-collector and common-emitter configurations forming a Darlington pair made up of Q_{16} and Q_{17} . This arrangement offers a high load resistance to the differential stage and hence provides a large voltage gain. Capacitor C_x is the pole-splitting compensating capacitor connected in shunt-shunt feedback, and it controls the unity-gain bandwidth and the slew rate.

Output Stage The output stage is a complementary class AB push-pull circuit consisting of transistors Q_{14} and Q_{20} . Diode-connected transistors Q_{18} and Q_{19} provide the biasing voltage for class AB operation in order to reduce crossover distortion.

Protection Circuitry Transistors Q_{15} and Q_{21} act as the current booster. Resistors R_{e1} and R_{e2} provide short-circuit protection by turning on Q_{15} and Q_{21} so as to limit the currents through Q_{14} and Q_{20} , respectively.

Biasing Circuitry The complete schematic, including the biasing circuitry, is shown in Fig. 15.12, which has an extra protection circuit (consisting of transistors Q_{23} and Q_{24}) to short the input terminal of Q_{16} (in the gain stage) to ground through Q_{23} . Transistors Q_{10} and Q_{11} form a Widlar current mirror, which biases transistors Q_3 and Q_4 of the common-base configuration. The current source consisting of transistors Q_{12} and Q_{13} biases the gain and output stages. The reference current I_{ref} can be found from

$$I_{ref} = \frac{V_{CC} + V_{EE} - V_{BE11} - V_{EB12}}{R_5} \quad (15.55)$$

Transistor Q_{13} is a multicollector lateral *pn*p device. Its geometry is shown in Fig. 15.13(a), and its symbol is shown in Fig. 15.13(b). The collector ring has been split into two parts—one part faces on three-fourths of the emitter periphery and collects the holes injected from that periphery, and the second one faces on one-fourth of the emitter periphery and collects the holes from that periphery. The structure is analogous to two *pn*p transistors whose base-emitter junctions are connected in parallel, one with an I_S that is one-fourth that of a standard *pn*p transistor and the other with an I_S that is three-fourths that of a standard *pn*p transistor. This electrical equivalence is shown in Fig. 15.13(c). Thus, the currents I_{Q2} and I_{Q3} are three-fourths and one-fourth of the reference current I_{ref} , respectively. That is,

$$I_{Q2} = \frac{3I_{ref}}{4} \quad \text{and} \quad I_{Q3} = \frac{I_{ref}}{4}$$

JFET Op-Amp LF411

The simplified schematic of the LF411 op-amp is shown in Fig. 15.14. Its internal structure is similar to that of the LH0022 op-amp. The differential input stage consists of *p*-channel transistors J_1 and J_2 with a current mirror load. This stage has low offset, low drift, and a high unity-gain bandwidth. The complete schematic appears in Fig. 15.15, which shows in detail the biasing circuitry. There is a resistor R_3 in the drain of J_2 , but none in that of J_1 . JFET J_2 operates in a common-source configuration, whereas JFET J_1 operates in a common-drain configuration. This type of arrangement gives a lower voltage gain but a wider bandwidth.

FIGURE 15.12 Schematic for op-amp LH0022 (Courtesy of National Semiconductor, Inc.)

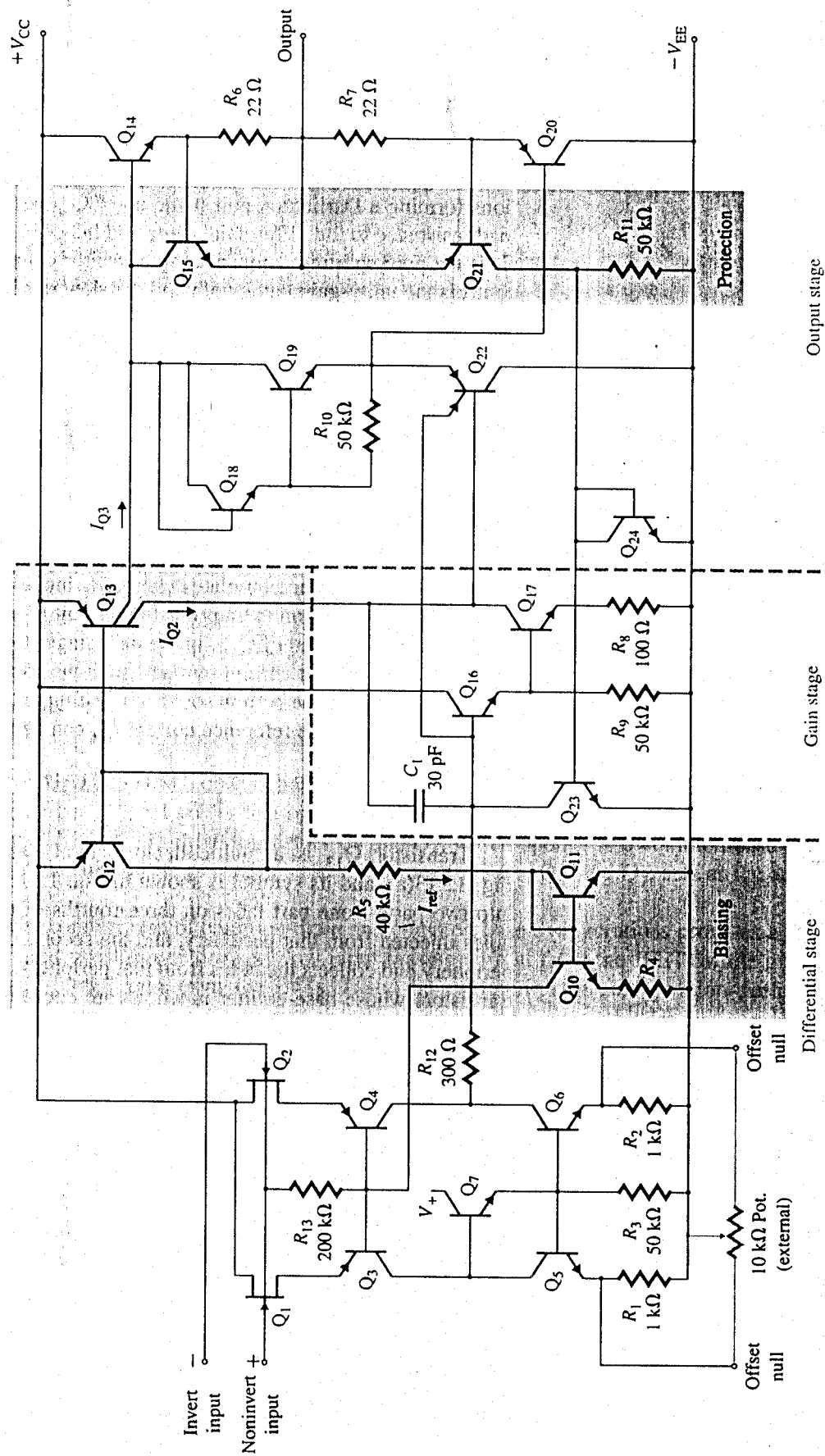
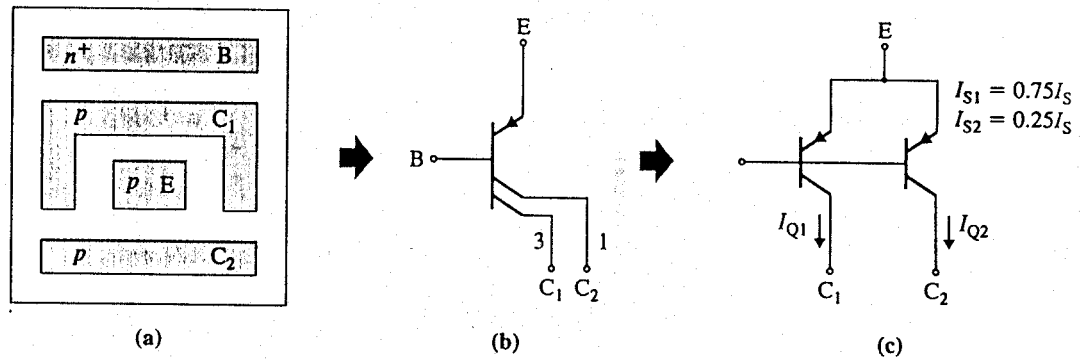


FIGURE 15.13

Electrical equivalent for multicollector lateral *pnp* transistor



A large value of dc biasing circuit I_Q (in mA) can be used for JFET differential amplifiers without significantly affecting the input biasing currents. On the other hand, for BJT differential amplifiers I_Q is kept small (in μA) in order to have a low input biasing current or high input resistance. Some parameters of the LF411 op-amp are listed in Table 15.2.

TABLE 15.2

Parameters of op-amp LF411

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 18	V
Input offset voltage V_{OS}		0.8	2.0	mV
Thermal drift D_v		7	20	$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		50	200	pA
Input offset current I_{OS}		25	100	pA
Differential input resistance R_{id}		10^{12}		Ω
Common-mode input resistance R_{ic}		10^{12}		Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.0		pF
Open-loop voltage gain A_o	25	200		V/mV
Common-mode rejection ratio CMRR	70	100		dB
Unity-gain bandwidth f_u	2.7	4.0		MHz
Slew rate SR	8.0	15		V/ μs
Power supply rejection ratio PSRR	70	100		dB

FIGURE 15.14

Simplified schematic for op-amp LF411
(Courtesy of National Semiconductor, Inc.)

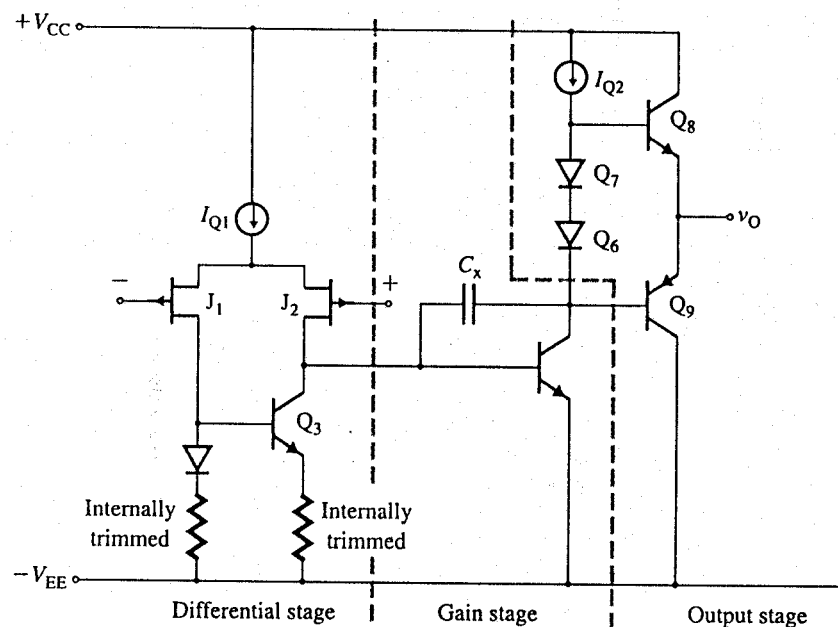
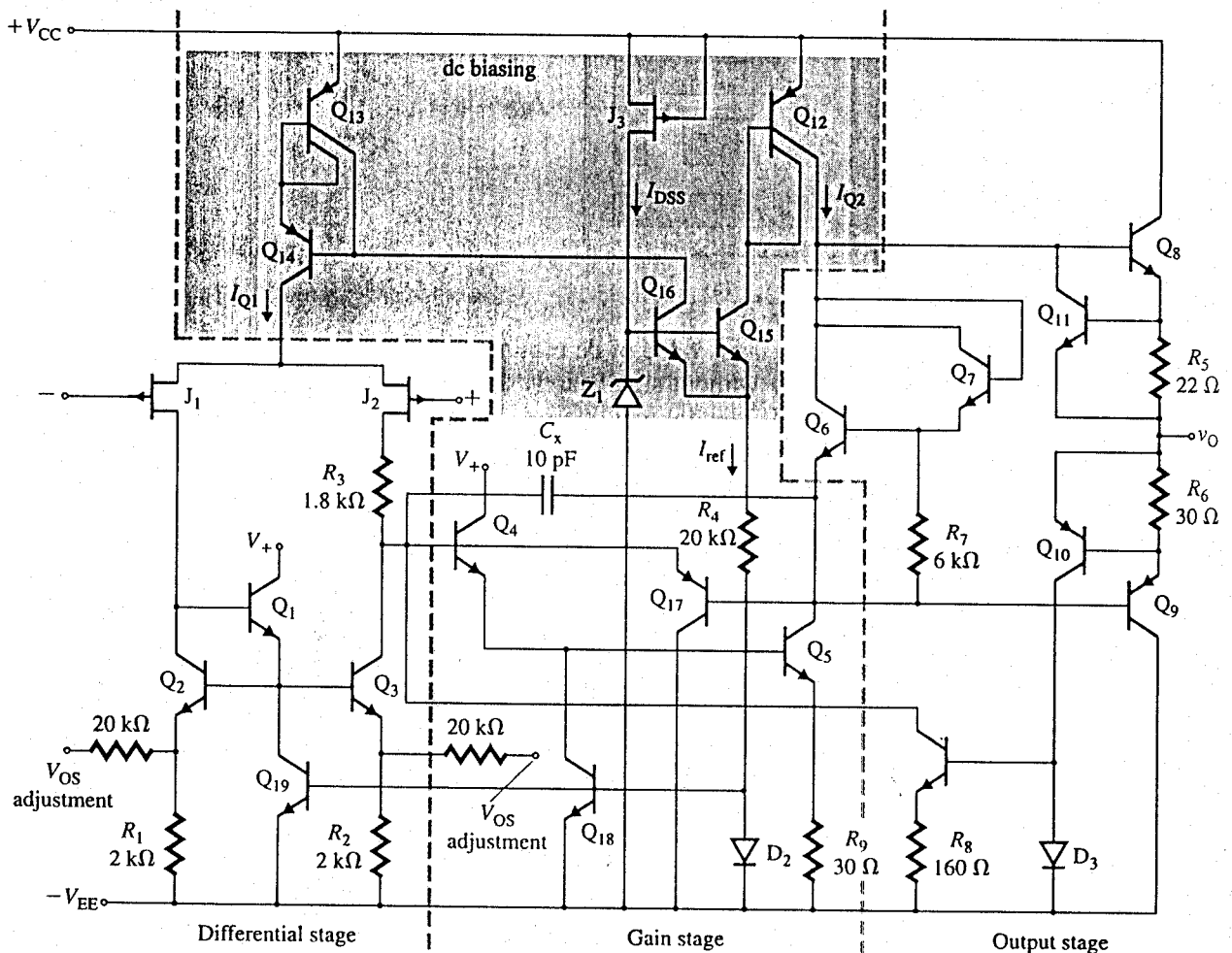


FIGURE 15.15 Schematic for op-amp LF411 (Courtesy of National Semiconductor, Inc.)

dc Biasing The zener diode Z_1 allows stable dc biasing with thermal compensation by diode D_2 and resistor R_4 . With JFET J_3 acting as a current-regulator diode (see Sec. 13.4), the current through zener diode Z_1 is kept constant at I_{DSS} . If V_Z is the zener voltage, then

$$I_{ref} = \frac{V_Z - V_{BE16} - V_{D2}}{R_4} \quad (15.56)$$

which in turn sets the dc biasing currents I_{Q1} and I_{Q2} .

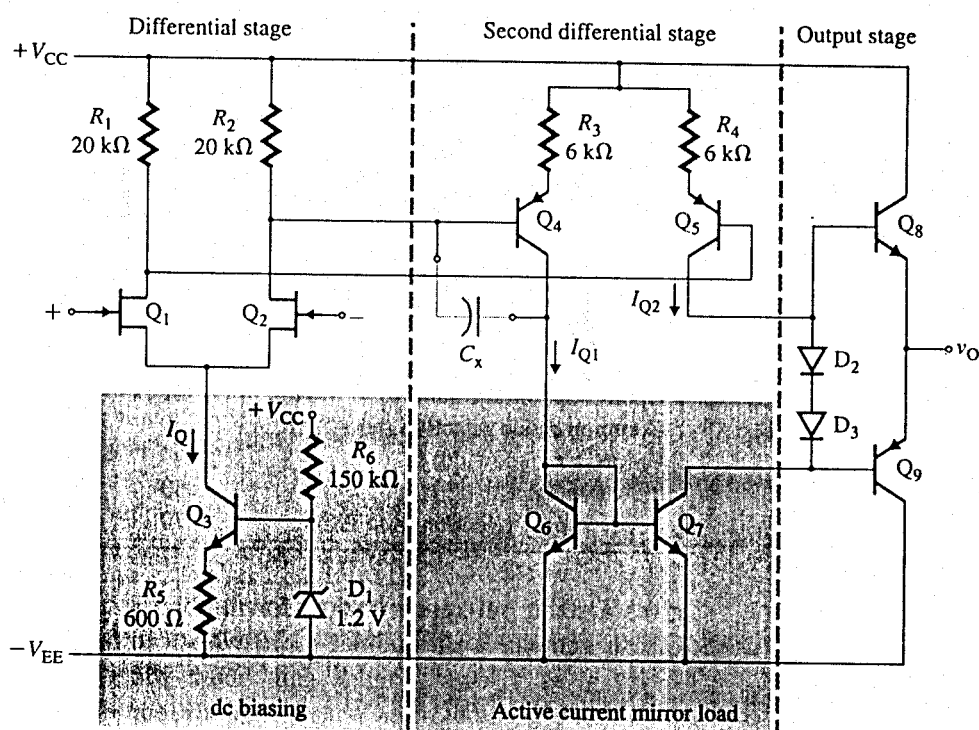
Thermal Protection Transistor Q_{19} is normally off. If the temperature rises, V_{BE16} will fall because of the negative temperature coefficient of Q_{16} , and the zener voltage V_Z will rise because of the positive temperature coefficient of zener diode Z_1 . As a result, the voltage at the emitter of Q_{16} will rise; thus, the voltage at the anode of D_2 will also rise. If the temperature rise is adequate, Q_{18} and Q_{19} will turn on and reduce the gain and the output voltage of the amplifier.

JFET Op-Amp LH0062

The simplified schematic of the LH0062 op-amp is shown in Fig. 15.16. The internal structure is similar to that of op-amp LH0022.

Differential Stage The differential input stage consists of n -channel transistors Q_1 and Q_2 with an active load. This is a normal source-coupled differential pair with a difference output, which gives a lower gain but a wider bandwidth. The input resistance is very high

FIGURE 15.16
Simplified schematic for
op-amp LH0062
(Courtesy of National
Semiconductor, Inc.)



for the JFET input stage. The dc biasing current I_Q is set by the current source consisting of transistor Q_3 and zener diode D_1 . Thus,

$$I_Q \equiv \frac{V_Z - V_{BE3}}{R_5} \quad (15.57)$$

$$= \frac{1.2 - 0.6}{600} = 1 \text{ mA}$$

Gain Stage The gain stage is a common-emitter coupled pair, which drives a current mirror load consisting of transistors Q_6 and Q_7 . The single-ended output gives a larger voltage gain. The biasing current I_{Q1} can be found from

$$I_{Q1}R_3 + V_{EB4} = \frac{R_2 I_Q}{2} \quad (15.58)$$

$$I_{Q1} = \frac{R_2 I_Q / 2 - V_{EB4}}{R_3}$$

$$= \frac{20 \text{ k} \times 0.5 \text{ mA} - 0.6}{6 \text{ k}} = 1.6 \text{ mA}$$

The collector current of Q_7 is the mirror of that of Q_6 . That is, I_{Q2} is the mirror of I_{Q1} , and $I_{Q2} = I_{Q1} = 1.6 \text{ mA}$, which is also the biasing current for the output stage. The high gain and wider bandwidth are obtained by cascading two differential stages. The slew rate is also high because of the higher dc biasing current. Some parameters of the LH0062 op-amp are listed in Table 15.3.

JFET Op-Amp LH0032

The LH0032 is an ultrafast op-amp. Its schematic is shown in Fig. 15.17. The internal structure is similar to that of op-amp LH0062, except that the second differential stage uses common-base cascode BJTs for a higher voltage gain. The zener diode D_{Z1}

TABLE 15.3
Parameters of op-amp
LH0062C

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 18	V
Input offset voltage V_{OS}		10	15	mV
Thermal drift D_v		10	35	$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		10	65	pA
Input offset current I_{OS}		1	5	pA
Differential input resistance R_{id}		10^{12}		Ω
Common-mode input resistance R_{ic}		10^{12}		Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.0		pF
Open-loop voltage gain A_o	25	160		V/mV
Common-mode rejection ratio CMRR	70	90		dB
Unity-gain bandwidth f_u		15		MHz
Slew rate SR	50	75		V/ μs
Power supply rejection ratio PSRR	70	90		dB

gives a stable reference voltage for the biasing circuit consisting of transistors Q_8 and Q_9 . In general, a differential stage with a difference output (i.e., the first differential stage) gives a lower voltage gain but a wider bandwidth. A differential pair with a single-ended output (i.e., the second differential stage) gives a higher voltage gain but a lower bandwidth. However, the common-base cascode connection gives a wider bandwidth.

The LH0032 op-amp has very high gain, a very large slew rate, and a very large bandwidth. Note that there is no compensation capacitor. As a result, the bandwidth is widened. Some parameters of the LH0032 op-amp are listed in Table 15.4.

FIGURE 15.17 Schematic for op-amp LH0032 (Courtesy of National Semiconductor, Inc.)

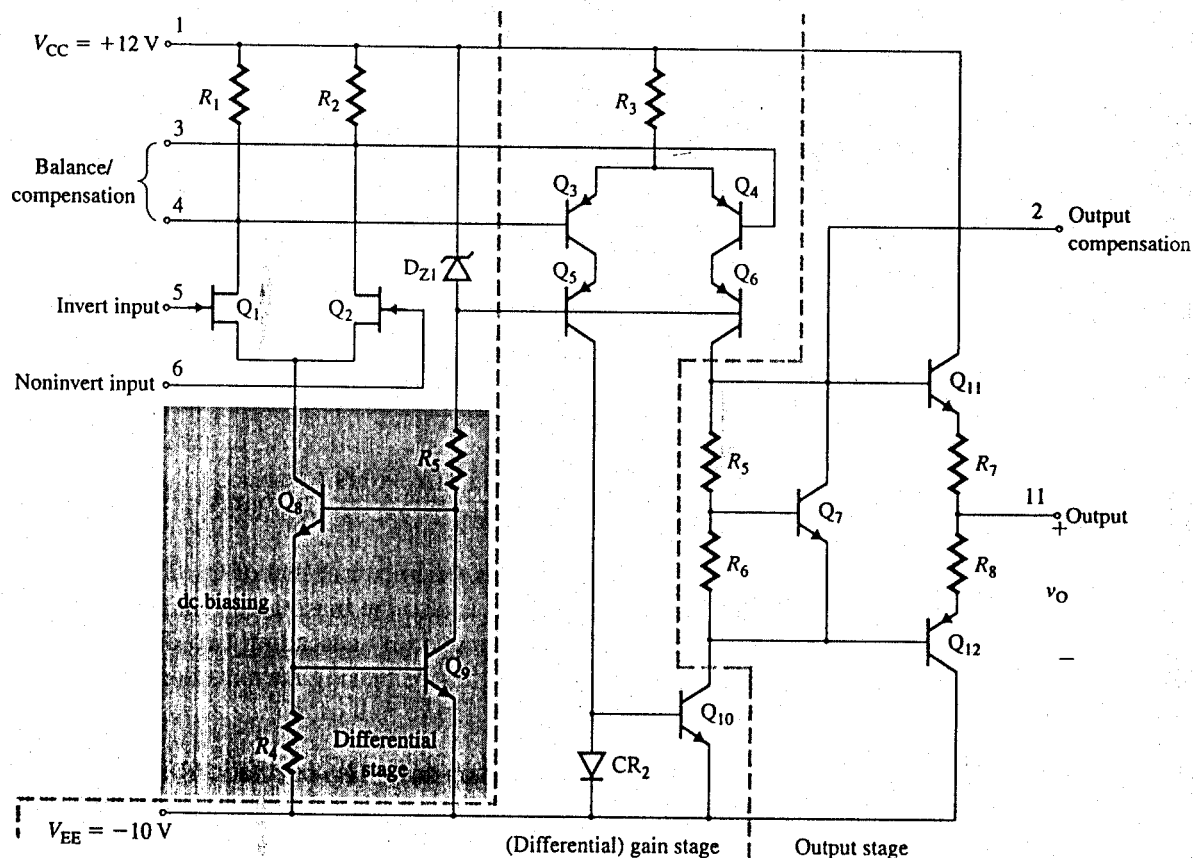


TABLE 15.4
Parameters of op-amp
LH0032A

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 18	V
Input offset voltage V_{OS}		1.0	2.0	mV
Thermal drift D_v		15	30	$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		50	150	pA
Input offset current I_{OS}		10	30	pA
Differential input resistance R_{id}		10^{12}		Ω
Common-mode input resistance R_{ic}		10^{12}		Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.0		pF
Open-loop voltage gain A_o	60	70		dB
Common-mode rejection ratio CMRR	50	60		dB
Unity-gain bandwidth f_u		70		MHz
Slew rate SR	350	500		V/ μs
Power supply rejection ratio PSRR	50	60		dB

KEY POINTS OF SECTION 15.4

- JFET op-amps are generally hybrid-type amplifiers, using a pair of JFET transistors for the input stage differential amplifier and bipolar transistors for the rest of the circuit. This arrangement gives a very high input resistance (on the order of $10^{12} \Omega$), a low input biasing current (in pA), and a large voltage gain (on the order of 100 dB).
- The difference output (70 MHz for the LH0032 op-amp), which gives a lower gain but wider bandwidth, is normally used for ultrafast op-amps. Compensation capacitance is avoided (see Fig. 15.17).

15.5 CMOS Op-Amps

CMOS Op-Amp MC14573

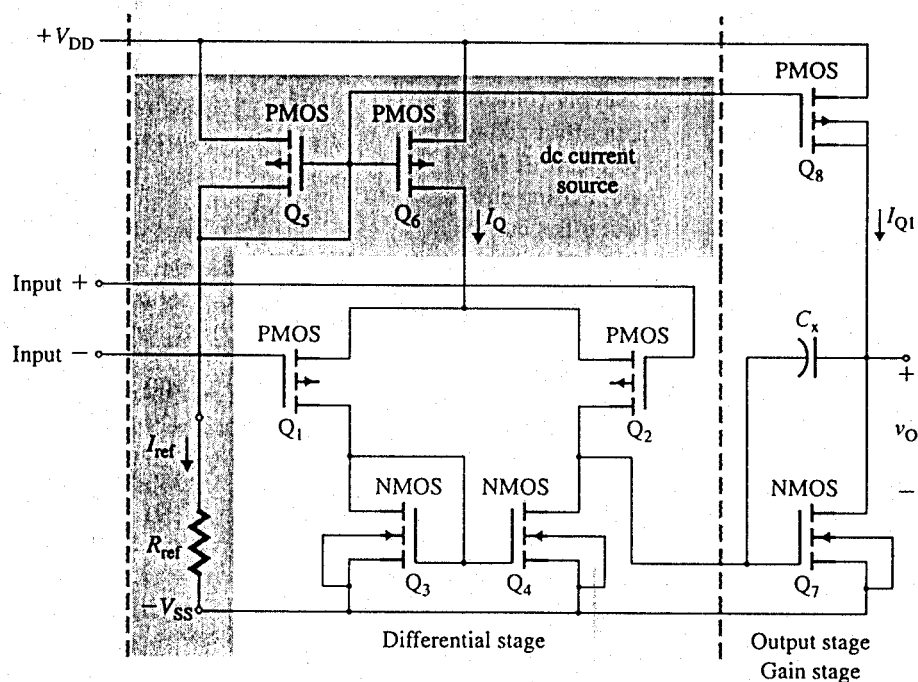
CMOS amplifiers can have either two or three stages. The gain and output stages are combined into a single stage. This type of amplifier has a very high input resistance, and the voltage gain is generally comparable to that of other types of amplifiers. In this section we will consider two CMOS amplifiers.

The simplified schematic of op-amp MC14573 is shown in Fig. 15.18. Its internal structure can be divided into a differential CMOS stage, a gain stage, and a biasing circuit. This op-amp has a very high input resistance, but the gain is lower than that of other op-amps, as expected. Some parameters of the MC14573 op-amp are listed in Table 15.5.

TABLE 15.5
Parameters of op-amp
MC14573

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 18	V
Input offset voltage V_{OS}		160	600	μV
Thermal drift D_v		1		$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B			1.0	nA
Input offset current I_{OS}			200	pA
Differential input resistance R_{id}		10^{12}		Ω
Common-mode input resistance R_{ic}		10^{12}		Ω
Output resistance R_o		50		Ω
Input capacitance C_i		1.0		pF
Open-loop voltage gain A_o		90		dB
Common-mode rejection ratio CMRR	75	95		dB
Unity-gain bandwidth f_u		70		MHz
Slew rate SR		2.5		V/ μs
Power supply rejection ratio PSRR	75	97		dB

FIGURE 15.18
Schematic for op-amp
MC14573 (Copyright of
Motorola. Used by
permission.)



Differential Stage The input stage is a PMOS differential amplifier consisting of transistors Q_1 and Q_2 . Its load is a current mirror consisting of NMOS transistors Q_3 and Q_4 .

Gain Stage The gain stage is also the output stage. It is a common-source amplifier with Q_8 as the active load. C_x is the compensation capacitor connected to Q_7 .

dc Biasing The differential stage is biased by transistors Q_5 and Q_6 as a current source. An external resistance R_{ref} sets the dc biasing current I_Q , which can be found approximately from

$$\begin{aligned} I_Q &= \frac{V_{DD} + V_{SS} - V_{SG}}{R_{ref}} \\ &= K_P(V_{GS} - V_t)^2 \end{aligned} \quad (15.59)$$

Transistor Q_8 serves as the load to the output stage. Since the gate voltages of Q_5 , Q_6 , and Q_8 are the same, the biasing current Q_8 equals $I_{Q1} = I_Q$.

EXAMPLE 15.2

D

Analyzing the CMOS op-amp MC14573 The CMOS amplifier in Fig. 15.18 is operated at a biasing current of $I_Q = 40 \mu\text{A}$. The parameters of the MOSFETs are $K_x = 10 \mu\text{A}/\text{V}^2$, $|V_{M(\text{NMOS})}| = V_{N(\text{PMOS})} = 70 \text{ V}$, $V_t = 0.5 \text{ V}$, and $W/L = 160 \mu\text{m}/10 \mu\text{m}$, except for Q_7 , for which $W/L = 320 \mu\text{m}/10 \mu\text{m}$. Assume $V_{DD} = -V_{SS} = 5 \text{ V}$.

- Find V_{GS} , g_m , and r_o for all MOSFETs.
- Find the low-frequency voltage gain of the amplifier A_{vo} .
- Find the value of the external resistance R_{ref} .
- Find the value of compensation capacitance C_x that gives a unity-gain bandwidth of 1 MHz and the corresponding slew rate.
- Find the value of resistance R_x to be connected in series with C_x in order to move the zero frequency to infinity.
- Find the common-mode input voltage range.
- Find the output voltage range.

SOLUTION

(a) K_P , V_{GS} , g_m , and r_o are calculated using the following equations:

$$K_P = \frac{K'_n W}{L} \quad (15.60)$$

$$V_{GS} = V_t + \sqrt{\frac{I_D}{K_P}} \quad (15.61)$$

$$g_m = 2K_P(V_{GS} - V_t) = 2\sqrt{K_P I_D} \quad (15.62)$$

$$r_o = \frac{|V_M|}{I_D} \quad (15.63)$$

Their values are shown in Table 15.6.

(b) The voltage gain of the first stage with the active load is given by

$$\begin{aligned} A_{v1} &= -g_{m4}(r_{o2} \parallel r_{o4}) \\ &= -113.1 \mu \times (3.5 \text{ M} \parallel 3.5 \text{ M}) = -198 \end{aligned} \quad (15.64)$$

The voltage gain of the second stage with the active load is given by

$$\begin{aligned} A_{v2} &= -g_{m7}(r_{o7} \parallel r_{o8}) \\ &= -226.3 \mu \times (1.75 \text{ M} \parallel 1.75 \text{ M}) = -198 \end{aligned} \quad (15.65)$$

Thus, the overall voltage gain is $A_{vo} = A_{v1}A_{v2} = 198 \times 198 = 39\,204$ (or 91.87 dB).

(c) From Eq. (15.59), we get the value of the external resistance R_{ref} as

$$R_{ref} = (V_{DD} + V_{SS} - V_{GS5})/I_Q = (5 + 5 - 1)/(40 \mu\text{A}) = 225 \text{ k}\Omega$$

(d) For $f_u = 1 \text{ MHz}$, Eq. (15.45) gives the value of compensation capacitance C_x as

$$C_x = G_{m1}/2\pi f_u = g_{m2}/2\pi f_u = 113.1 \mu/(2\pi \times 1 \text{ MHz}) = 18 \text{ pF}$$

From Eq. (15.52), we get the slew rate as

$$SR = I_Q/C_x = 40 \mu\text{A}/18 \text{ pF} = 2.22 \text{ V}/\mu\text{s}$$

(e) From Eq. (15.48), the value of resistance R_x is

$$R_x = 1/G_{m2} = 1/g_{m7} = 1/(226.3 \mu) = 4.42 \text{ M}\Omega$$

(f) Transistor Q_6 will leave saturation when the common-mode input voltage becomes

$$v_{ic(\max)} = V_{DD} - |V_{GS6}| + |V_t| - |V_{GS1}| = 5 - 1 + 0.5 - 0.854 = 3.646 \text{ V}$$

Transistors Q_1 and Q_2 will leave saturation when the common-mode input voltage falls below the voltage at the drain of Q_1 by $|V_t|$ —that is, when

$$v_{ic(\min)} = -V_{SS} + |V_{GS3}| - |V_t| = -5 + 1 - 0.5 = -4.5 \text{ V}$$

TABLE 15.6 Calculated values for Example 15.2

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L (in $\mu\text{m}/\mu\text{m}$)	160/10	160/10	160/10	160/10	160/10	160/10	320/10	160/10
K_P (in $\mu\text{A}/\text{V}^2$)	160	160	160	160	160	160	320	160
I_D (in μA)	20	20	20	20	40	40	40	40
V_{GS} (in V)	0.854	0.854	0.854	0.854	1	1	0.854	1
g_m (in $\mu\text{A}/\text{V}$)	113.1	113.1	113.1	113.1	160	160	226.3	160
r_o (in $\text{M}\Omega$)	3.5	3.5	3.5	3.5	1.75	1.75	1.75	1.75

Thus, the common-mode input voltage range is -4.5 V to 3.646 V .

(g) Transistor Q_8 will leave saturation when the output voltage becomes

$$v_{o(\max)} = V_{DD} - |V_{GS8}| + |V_t| = 5 - 1 + 0.5 = 4.5\text{ V}$$

Transistor Q_7 will leave saturation when the output voltage becomes

$$v_{o(\min)} = -V_{SS} + |V_{GS7}| - |V_t| = -5 + 0.854 - 0.5 = -4.646\text{ V}$$

Thus, the output voltage range is -4.646 V to 4.5 V .

CMOS Op-Amp TLC1078

The simplified schematic of the TLC1078 op-amp is shown in Fig. 15.19. Its structure is similar to that of op-amp MC14573. The internal structure can be divided into a differential CMOS stage, a gain stage, an output stage, and a biasing circuit. Some parameters of the TLC1078 op-amp are listed in Table 15.7.

Differential Stage The input stage is a PMOS differential amplifier consisting of transistors Q_1 and Q_5 . Its load is a current mirror consisting of NMOS transistors Q_2 and Q_4 , which have sources R_2 and R_3 to give high output resistances.

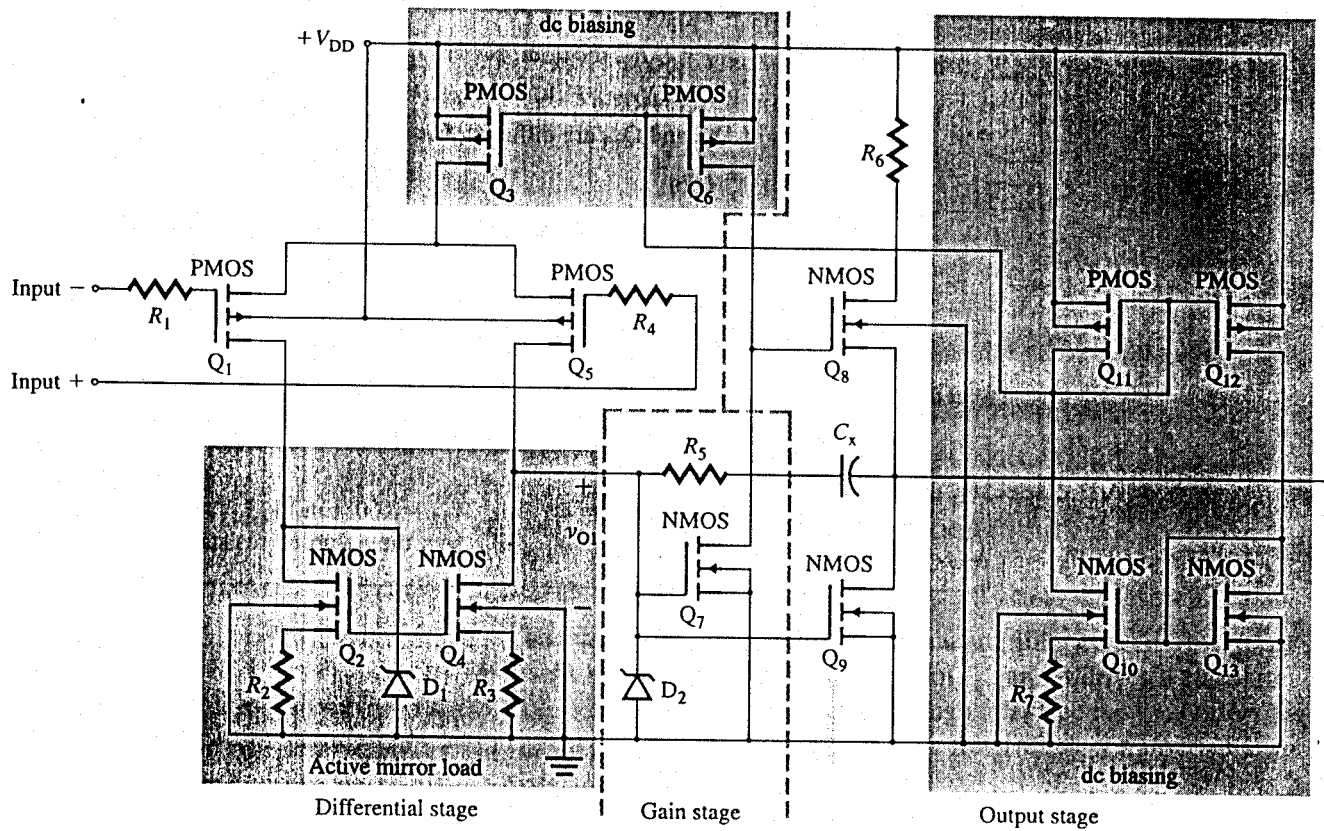
Gain Stage The gain stage uses NMOS Q_7 in a common-source configuration with PMOS Q_6 as the current source active load. The combination of C_x and R_5 is a pole-zero circuit, which can reduce the lowest pole or break frequency to a low value to ensure stability. Also, it can produce a zero to cancel out one of the second poles of the amplifier's open-loop frequency response.

Output Stage The output stage consists of a pair of NMOS transistors that operate in the class AB push-pull mode. Transistor Q_8 is the source follower, sourcing current to the load during the interval when the signal at the output of Q_7 goes up above the quiescent value. Transistor Q_9 acts as the common-source amplifier, sinking current from the load during the interval when the signal at the output of the differential stage goes down below the quiescent value.

A decreasing signal at the output of the differential stage will be amplified by Q_7 with a phase shift of 180° and then will appear through the source follower of Q_8 as an increasing signal to the load. However, an increasing signal will be amplified by the common-source amplifier of Q_9 with a phase shift of 180° and then will appear as a

TABLE 15.7
Parameters of op-amp
TLC1078

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			18	V
Input offset voltage V_{OS}		180	600	μV
Thermal drift D_v		1		$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		0.7		pA
Input offset current I_{OS}		0.1		pA
Differential input resistance R_{id}		1.5		T Ω
Common-mode input resistance R_{ic}		1.5		T Ω
Output resistance R_o		50		Ω
Input capacitance C_i		1.0		pF
Open-loop voltage gain A_o	110	120		dB
Common-mode rejection ratio CMRR	75	97		dB
Unity-gain bandwidth f_u		110		MHz
Slew rate SR		47		V/ms
Power supply rejection ratio PSRR	75	97		dB

FIGURE 15.19 Schematic for op-amp TLC1078 (Reprinted by permission of Texas Instruments)

decreasing signal to the load. Thus, the voltages applied to the gates of Q_8 and Q_9 will be phase shifted by 180° . The voltage gain through the two paths will be the same, however.

dc Biasing The differential amplifier is biased by transistors Q_3 and Q_6 as a current source whose gate voltage is set by the voltage divider circuit consisting of transistors Q_{11} through Q_{13} . All of the transistors are identical, except for Q_{10} and Q_{13} , whose channel widths differ from that of the others.

EXAMPLE 15.3**D**

Analyzing the CMOS op-amp TLC1078 The CMOS amplifier in Fig. 15.19 is operated at a biasing current of $I_Q = 40 \mu\text{A}$. The parameters of the MOSFETs are $K_x = 10 \mu\text{A}/\text{V}^2$, $|V_{M(\text{NMOS})}| = V_{N(\text{PMOS})} = 70 \text{ V}$, $V_t = 0.5 \text{ V}$, and $W/L = 160 \mu\text{m}/10 \mu\text{m}$, except for Q_{10} , for which $W/L = 40 \mu\text{m}/10 \mu\text{m}$. Find the value of the resistance R_7 . Assume $V_{DD} = -V_{SS} = 5 \text{ V}$.

SOLUTION

We have

$$K_P = K_x W/L = 10 \mu \times 160/10 = 160 \mu\text{A}/\text{V}^2 \quad \text{for all MOSFETs except } Q_{10}$$

$$K_{P10} = K_x W/L = 10 \mu \times 40/10 = 40 \mu\text{A}/\text{V}^2 \quad \text{for } Q_{10}$$

For $I_Q = 40 \mu\text{A}$ and $K_P = 160 \mu\text{A}/\text{V}^2$, Eq. (15.61) gives

$$V_{GS} = V_t + \sqrt{I_D/K_P} = 0.5 + \sqrt{40/160} = 1 \text{ V}$$

Thus,

$$V_{GS3} = V_{GS6} = V_{GS11} = V_{GS12} = 1 \text{ V}$$

Also,

$$I_{D3} = I_{D6} = I_{D1} = I_{D12} = I_{D10} = I_{D13} = I_Q$$

The drain current I_{D13} of Q_{13} is given by

$$I_{D13} = K_{P13}(V_{GS13} - V_t)^2 \quad (15.66)$$

Since $V_{GS10} = V_{GS13} - I_Q R_7$, the drain current I_{D10} of Q_{10} is given by

$$I_{D10} = K_{P10}(V_{GS10} - V_t)^2 = K_{P10}(V_{GS13} - I_Q R_7 - V_t)^2 \quad (15.67)$$

The V_{GS} values of Q_{10} and Q_{13} are different, but their drain currents are equal. That is,

$$I_{D13} = I_{D10}$$

and $K_{P13}(V_{GS13} - V_t)^2 = K_{P10}(V_{GS13} - I_Q R_7 - V_t)^2$

which relates R_7 to I_Q as follows:

$$R_7 = \frac{V_{GS13} - V_t}{I_Q} \left[1 - \left(\frac{K_{P13}}{K_{P10}} \right)^{1/2} \right] \quad (15.68)$$

Since K_p is proportional to the ratio W/L , Eq. (15.68) can be expressed as

$$R_7 = \frac{V_{GS13} - V_t}{I_Q} \left[1 - \left(\frac{W_{13}}{W_{10}} \right)^{1/2} \right] \quad (15.69)$$

which, for $I_Q = 40 \mu\text{A}$, $W_{10} = 40 \mu\text{m}$, $W_{13} = 160 \mu\text{m}$, $V_{GS13} = 1 \text{ V}$, and $V_t = 0.5 \text{ V}$, gives $R_7 = 7.3 \text{ k}\Omega$. Thus, the ratio $\sqrt{W_{13}/W_{10}}$ sets the value of resistance R_7 or I_Q .

KEY POINTS OF SECTION 15.5

- CMOS op-amps can have either two or three stages. The gain and output stages are often combined into a single stage. This type of amplifier has a very high input resistance, and the voltage gain is generally comparable to that of other types of amplifiers.
- Since MOSFETs have lower transconductance than other amplifiers, the gain stage often requires zero-pole compensation (see Fig. 15.19).

15.6

BiCMOS Op-Amps

BiCMOS Op-Amp CA3130

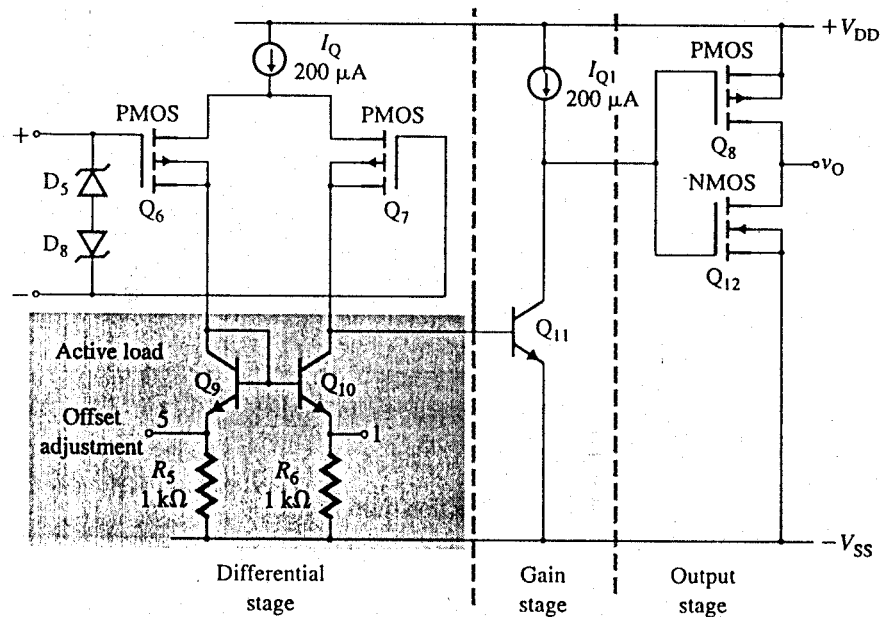
BiCMOS op-amps contain both CMOS and BJT transistors on the same chip. This arrangement incorporates the advantages of both BJTs and MOSFETs to achieve desirable characteristics such as high input resistance, low offset, large gain, and wide bandwidth.

The simplified schematic of the BiCMOS op-amp CA3130 is shown in Fig. 15.20. The internal structure can be divided into three stages: a differential MOS stage, a gain stage, and an output stage. Some parameters of the CA3130 op-amp are listed in Table 15.8.

TABLE 15.8
Parameters of op-amp
CA3130

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 18	V
Input offset voltage V_{OS}		8.0	15.0	mV
Thermal drift D_v		15	30	$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		5	50	pA
Input offset current I_{OS}		0.5	30	pA
Differential input resistance R_{id}		1.5		T Ω
Common-mode input resistance R_{ic}		1.5		T Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.3		pF
Open-loop voltage gain A_o	50	320		V/mV
Common-mode rejection ratio CMRR	70	90		dB
Unity-gain bandwidth f_u		15		MHz
Slew rate SR		10		V/ μs
Power supply rejection ratio PSRR	70	90		dB

FIGURE 15.20
Simplified schematic for
op-amp RCA-CA3130
(Courtesy of Harris
Corporation,
Semiconductor Sector)



Differential Stage The input stage is a PMOS differential amplifier consisting of transistors Q_6 and Q_7 . This stage is biased by a current source of I_Q , and it drives a current mirror load consisting of BJT transistors Q_9 and Q_{10} . Although a BJT active load offers high resistance, the voltage gain is only about 5 because of the relatively low transconductance of MOSFETs.

Resistors R_5 and R_6 allow offset voltage adjustment (in the range of $\pm R_5 I_Q / 2 = \pm 1 \text{ k} \times 100 \mu = \pm 100 \text{ mV}$) through an externally connected potentiometer (typically $10 \text{ k}\Omega$) across terminals 1 and 5. Also, resistor R_6 increases the output resistance of the active load and hence the voltage gain. Zener diodes D_5 and D_8 protect the thin gate-oxide of the MOSFETs from excessive voltage spikes and static discharge, which could cause breakdown of the oxide layer and hence damage the transistors.

Gain Stage The gain stage is a common-emitter amplifier consisting of transistor Q_{11} and has an active current load for a large voltage gain (about 6000). Note that the absence of a compensation capacitor gives a high bandwidth (15 MHz).

Output Stage The output stage is a CMOS push-pull stage consisting of PMOS Q_8 and NMOS Q_{12} . If the voltage at the collector of Q_{11} increases by a small amount above the quiescent level, then NMOS transistor Q_{12} turns on and PMOS transistor Q_8 remains off. On the other hand, if the voltage goes down by a small amount, then PMOS transistor Q_8 turns on and NMOS transistor Q_{12} remains off. The voltage gain of the output stage is about 30.

BiCMOS Op-Amp CA3140

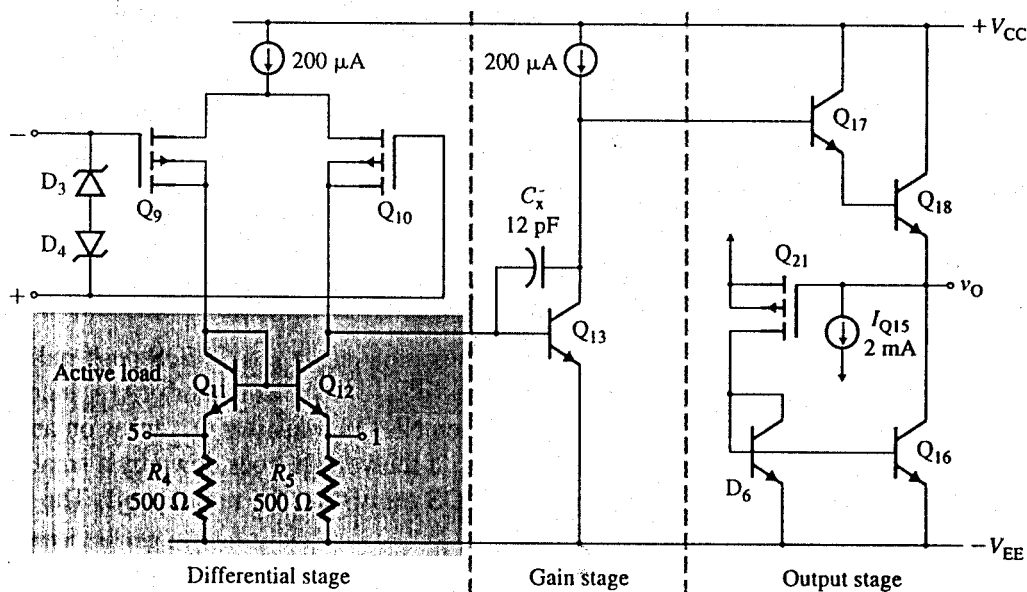
The simplified schematic of the BiCMOS op-amp CA3140 is shown in Fig. 15.21. Its internal structure is similar to that of op-amp CA3130, except for the output stage and the addition of a compensation capacitor C_x in the second stage. The voltage gain of the differential stage is about 10. The offset voltage adjustment is in the range of $\pm R_5 I_Q / 2 = \pm 500 \times 100 \mu = \pm 50 \text{ mV}$. C_x provides feedback stability, but it reduces the bandwidth. The Darlington *nnp* emitter follower in the output stage increases the effective load resistance seen by transistor Q_{13} in the gain stage and hence increases the voltage gain to about 10. The voltage gain of the gain stage is about 10,000. Some parameters of the CA3140 op-amp are listed in Table 15.9.

TABLE 15.9
Parameters of op-amp
CA3140

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 18	V
Input offset voltage V_{OS}		8.0	15.0	mV
Thermal drift D_v		10	30	$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		10	50	pA
Input offset current I_{OS}		0.5	30	pA
Differential input resistance R_{id}		1.5		T Ω
Common-mode input resistance R_{ic}		1.5		T Ω
Output resistance R_o		50		Ω
Input capacitance C_i		1		pF
Open-loop voltage gain A_o	20	100		V/mV
Common-mode rejection ratio CMRR	70	90		dB
Unity-gain bandwidth f_u		4.5		MHz
Slew rate SR		9		V/ μs
Power supply rejection ratio PSRR	76	80		dB

Output Stage The Darlington emitter follower offers a lower than average output resistance and a high resistance to the gain stage. If the voltage at the collector of transistor Q_{13} goes up in the positive direction above the quiescent value, transistor Q_{18} will drive the load and source current of I_{Q15} (2 mA). However, if the current of Q_{18} falls below the level of I_{Q15} (2 mA), the voltage across the load will go down below the quiescent level. Transistor Q_{18} will always remain on. This will cause MOSFET Q_{21} to turn on. Since the collector current of Q_{16} will be the mirror of the drain current of MOSFET Q_{21} , transistor Q_{16} will sink the load current.

FIGURE 15.21
Simplified schematic for
op-amp RCA-CA3140
(Courtesy of Harris
Corporation,
Semiconductor Sector)



KEY POINT OF SECTION 15.6

- BiCMOS op-amps contain both CMOS and BJT transistors on the same chip. The advantages of both BJTs and MOSFETs are utilized to achieve desirable characteristics such as high input resistance (1.5 T Ω), low input biasing current (10 pA), large gain (100 dB), and wide bandwidth (4.5 MHz).

15.7 BJT Op-Amps

Like FET op-amps, BJT amplifiers have three stages: a differential stage, a gain stage, and an output stage. They have the disadvantages of a lower input resistance and a higher input biasing current. However, BJTs provide higher voltage gain. In this section we will consider two popular op-amps.

BJT Op-Amp LM124

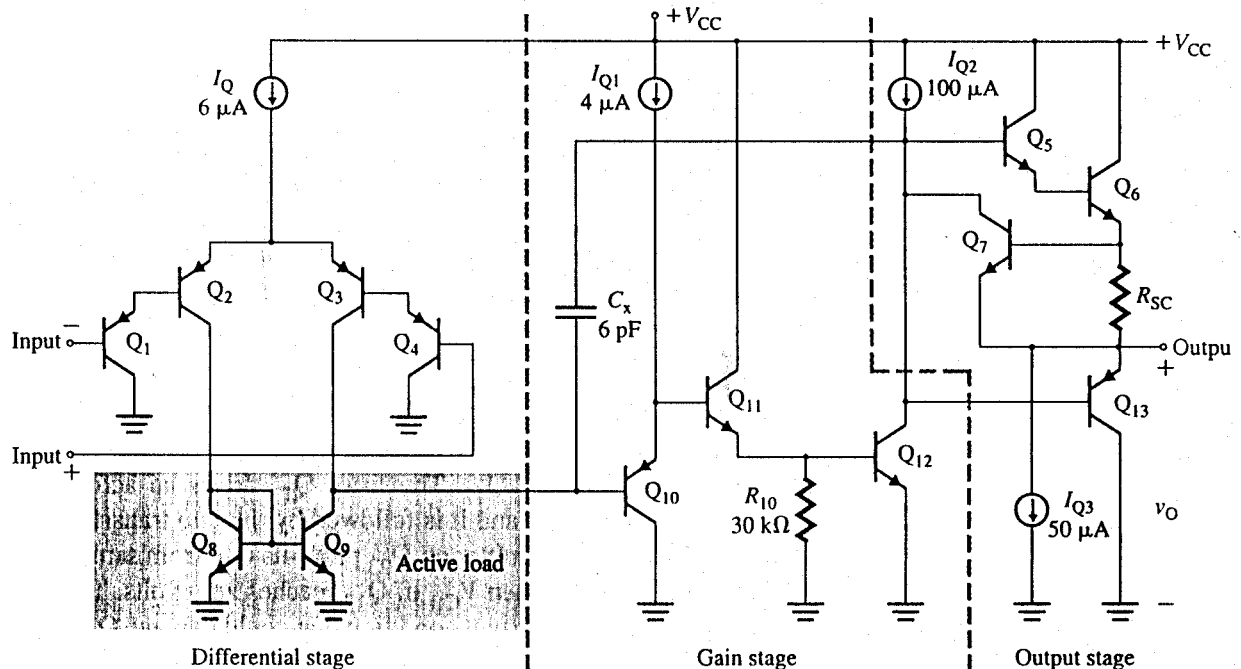
The LM124 op-amp is designed to operate from a power supply of ± 16 V, but it can operate from a single power supply as low as 5 V. The simplified schematic is shown in Fig. 15.22. Some of the parameters of LM124 op-amps are listed in Table 15.10.

TABLE 15.10
Parameters of op-amp
LM124

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 16	V
Input offset voltage V_{OS}		1.0	2.0	mV
Thermal drift D_v		100	200	$\mu\text{V}/^\circ\text{C}$
Input biasing current I_B		20	50	nA
Input offset current I_{OS}		2.0	10	nA
Differential input resistance R_{id}		2		M Ω
Common-mode input resistance R_{ic}		2		M Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.0		pF
Open-loop voltage gain A_o	50	100		V/mV
Common-mode rejection ratio CMRR	70	85		dB
Unity-gain bandwidth f_u		1.0		MHz
Slew rate SR		3.0		V/ μs
Power supply rejection ratio PSRR	650	100		dB

Differential Stage The differential input stage consists of bipolar transistors Q_1 through Q_4 . They are connected in Darlington pairs to give high input resistances and low input biasing currents. These BJTs drive the current mirror load consisting of transistors Q_8 and Q_9 for a high differential gain.

FIGURE 15.22 Simplified schematic for op-amp LM124 (Courtesy of National Semiconductor, Inc.)



Gain Stage The gain stage is a common-emitter amplifier consisting of *pnp* transistor Q_{10} (with an active load), which is followed by a Darlington pair consisting of transistors Q_{11} and Q_{12} . The beta of a *pnp* transistor is generally low. The Darlington pair offers a high load to transistor Q_{10} . This arrangement ensures a high voltage gain (100 dB). The number of poles in the op-amp increases with the number of transistor stages. C_x is used for feedback compensation.

Output Stage The Darlington emitter follower consisting of transistors Q_5 and Q_6 offers a lower than average output resistance and a high resistance to the gain stage. If the voltage at the collector of transistor Q_{12} goes up in the positive direction, transistor Q_6 will drive the load and source current of I_{Q3} (50 μ A). However, if the current of Q_6 falls below the level of I_{Q3} (50 μ A), transistor Q_6 will be off, and the voltage across the load will go down below the quiescent level. This will cause transistor Q_{13} to turn on and sink the load current. Transistor Q_7 , together with resistor R_{SC} , provides short-circuit protection by limiting the current through Q_6 . This is done by turning Q_7 on if the voltage across R_{SC} exceeds the base-emitter voltage V_{BE7} .

The LM741 op-amp is familiar to students because its characteristics are commonly used in illustrating the applications of op-amps. This op-amp was first introduced in 1966 by Fairchild Semiconductor, Inc. It is relatively simple. It has a large voltage gain and a large CMRR. The range of common-mode and differential input voltages is wide. The schematic is shown in Fig. 15.23. The op-amp circuit can be divided into five parts: a dc biasing circuit, an input stage, an amplifier stage, an output stage, and overload protection. Some of the parameters of the LM741 op-amp are listed in Table 15.11.

BJT Op-Amp LM741

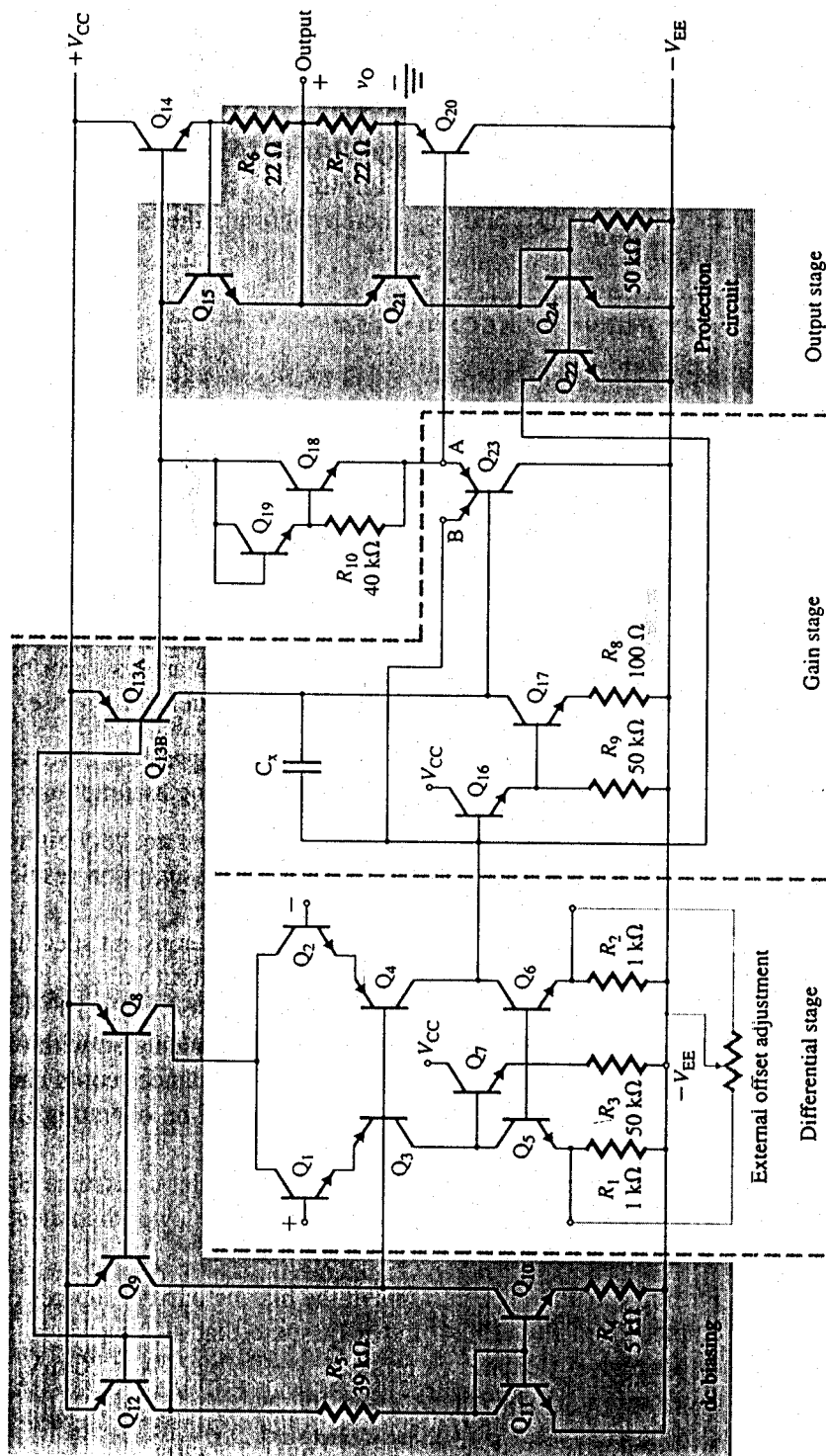
TABLE 15.11
Parameters of op-amp
LM741

Parameter	Minimum	Typical	Maximum	Units
dc supply voltages V_S			± 22	V
Input offset voltage V_{OS}		1.0	5.0	mV
Thermal drift D_v		15		μ V/ $^{\circ}$ C
Input biasing current I_B		80	550	nA
Input offset current I_{OS}		20	200	nA
Differential input resistance R_{id}	0.3	2		M Ω
Common-mode input resistance R_{ic}		2		M Ω
Output resistance R_o		75		Ω
Input capacitance C_i		4.0		pF
Open-loop voltage gain A_o	50	200		V/mV
Common-mode rejection ratio CMRR	70	90		dB
Unity-gain bandwidth f_u		1.0		MHz
Slew rate SR		0.5		V/ μ s
Power supply rejection ratio PSRR	70	90		dB

Differential Stage The differential input stage consists of bipolar transistors Q_1 through Q_4 . They form common-emitter and common-base configurations (see Fig. 13.33) for higher bandwidth and gain. This stage is biased by the current source consisting of Q_8 , and it drives the current mirror active load consisting of Q_5 , Q_6 , and Q_7 . The biasing feedback loop formed by Q_8 and Q_9 stabilizes the biasing currents in each of the input transistors at approximately one-half of the collector current of Q_{10} .

Gain Stage The gain stage consists of a common-emitter Darlington pair amplifier made up of transistors Q_{16} and Q_{17} . Transistor Q_{17} drives an active load consisting of transistor Q_{13B} for high gain, and it is followed by the *pnp* transistor Q_{23} in common-emitter configuration. The extra emitter on Q_{23} prevents Q_{17} from saturating by diverting the base drive current from Q_{16} when V_{CB} of Q_{17} reaches zero volts. This arrangement eliminates the possibility of a high current condition that could damage Q_{16} . Q_{23B} acts as the dc feedback so that $V_{B16} - V_{C17} = V_{EB23B}$. C_x is used for frequency compensation.

FIGURE 15.23 Schematic for op-amp LM741 (Courtesy of National Semiconductor, Inc.)



Output Stage The output stage is a push-pull output stage and operates in class AB mode to reduce crossover distortion. It is biased by a V_{BE} multiplier circuit (see Fig. 15.24) consisting of transistors Q_{18} and Q_{19} .

Protection Circuitry Resistors R_6 and R_7 provide short-circuit protection, turning on Q_{15} and Q_{21} to limit the currents through Q_{14} and Q_{20} , respectively. Turning on Q_{21} also turns on transistors Q_{22} and Q_{24} , thereby shorting the input signal to the base of Q_{16} in the gain stage.

KEY POINT OF SECTION 15.7

- BJT amplifiers usually have three stages: a differential stage, a gain stage, and an output stage. They have the disadvantages of a low input offset voltage (1 mV), a low input resistance (2 M Ω), and a high input biasing current (60 nA), but they provide large gain (100 dB) and wide bandwidth (1 MHz).

15.8

Analysis of the LM741 Op-Amp

dc Analysis

As an example, let us carry out a complete analysis of the LM741 op-amp shown in Fig. 15.23, finding the dc biasing currents, the small-signal gain, the input and output resistances, and the unity-gain bandwidth. The analysis can be divided into three sections: dc analysis, ac analysis, and analysis of frequency response.

The dc analysis to determine the quiescent operating currents and voltages of the transistors can be simplified by making the following assumptions:

1. The output resistances of the transistors are very high and do not affect the currents flowing in the circuit. Usually, this assumption results in a 10 to 20% error in the calculated currents.
2. The output voltage is maintained at a constant specified value by the internal feedback loop. Let us assume that the output voltage is zero. This assumption is necessary because of the very high gain, typically 10^5 , which results in a very low input voltage. If the output voltage is calculated with two input terminals grounded, any change in the beta or output resistances could cause a large change in the output voltage and the transistors could be operating in the saturation region rather than in the active region as expected.
3. The *nnp* transistors have large betas; let us assume $\beta_{F(npn)} = 250$.
4. The betas of *pnp* transistors are much lower than those of *nnp* transistors; let us assume $\beta_{F(pnp)} = 50$.

Biasing Circuit The currents in the biasing current sources of Q_{10} and Q_{13AB} can be calculated from Fig. 15.24. Let us assume that all transistors are operating in the forward active region, the base currents are negligible, $V_T = 26$ mV, and $V_{BE} = 0.7$ V. The reference current can be calculated as follows:

$$I_{ref} = \frac{V_{CC} - V_{EE} - V_{BE11} - V_{EB12}}{R_5} \quad (15.70)$$

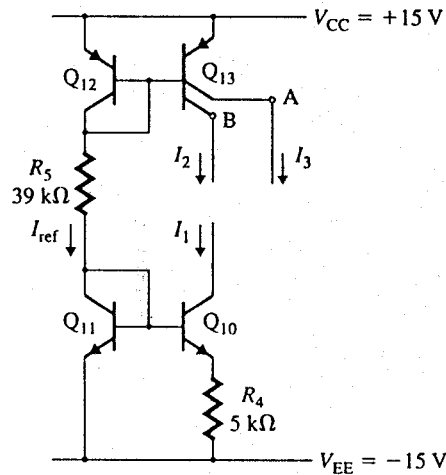
$$= \frac{15 + 15 - 2 \times 0.7}{39 \text{ k}\Omega} = 0.73 \text{ mA}$$

The transistors Q_{10} and Q_{11} form a Widlar current source. Using Eq. (13.16), we can find the output current I_1 from

$$V_T \ln \frac{I_{ref}}{I_1} = R_4 I_1 \quad (15.71)$$

$$V_T \ln \frac{0.73 \text{ mA}}{I_1} = 5 \text{ k}\Omega \times I_1$$

FIGURE 15.24
Biasing circuit for the
LM741 op-amp



which, by trial and error, gives $I_1 = 19 \mu\text{A}$.

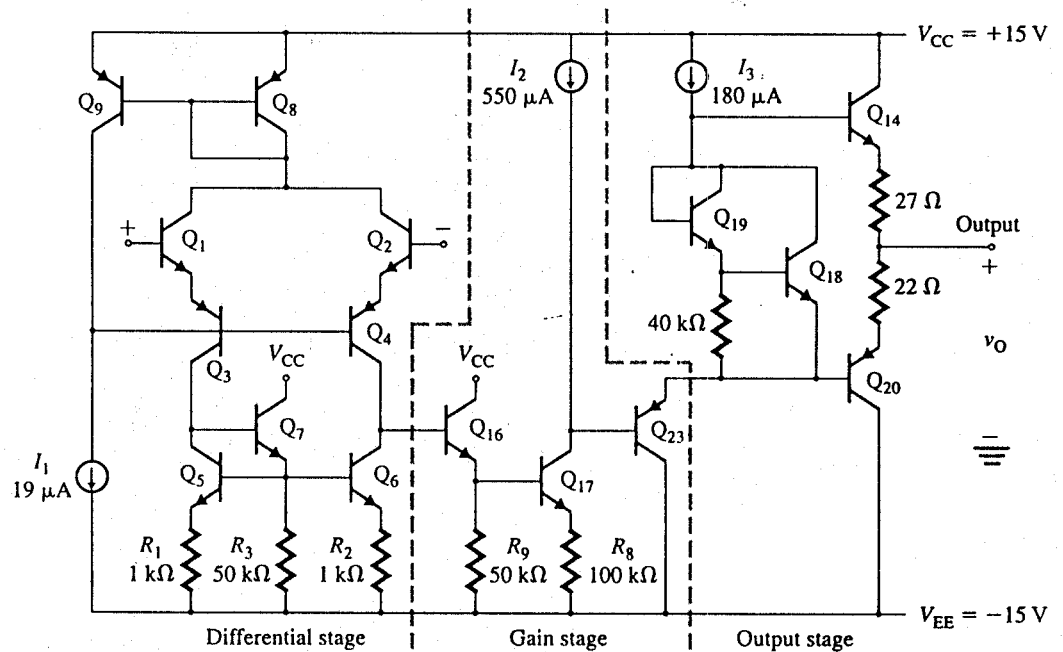
Transistor Q_{13} is a multicollector lateral *pnp* device. Thus, currents I_2 and I_3 are three-fourths and one-fourth of the reference current I_{ref} , respectively:

$$I_2 = (3/4) \times 0.73 \text{ mA} = 0.55 \text{ mA}$$

$$I_3 = (1/4) \times 0.73 \text{ mA} = 0.18 \text{ mA}$$

If we replace the biasing circuit in Fig. 15.24 by the equivalent current sources of I_1 , I_2 , and I_3 , the circuit in Fig. 15.23 can be simplified to that in Fig. 15.25.

FIGURE 15.25
The LM741 op-amp with
biasing current sources



Input Stage The input stage provides a high input resistance for differential and common-mode input signals, the differential-to-single output, and some voltage gain. The input stage of the LM741 with biasing current sources is shown in Fig. 15.26. Since the *nnp* transistors have large values of beta, the base currents are negligible compared to the collector currents. For identical transistors, $I_{C9} = I_{C8}$.

The current I_T , which is the sum of I_{C8} plus the base currents of Q_8 and Q_9 , can be found from

$$I_T = I_{C8} + I_{B8} + I_{B9} = I_{C9} \left(1 + \frac{2}{\beta_{F(\text{pnp})}} \right) \quad (15.72)$$

The emitter current of Q_7 is the sum of the base currents of Q_5 and Q_6 plus the current into resistor R_3 :

$$I_{E7} = I_{B5} + I_{B6} + I_{R3} \approx I_{R3}$$

Assuming $I_{E5} \approx I_{C5}$ and $I_{E6} \approx I_{C6}$, the voltage across R_3 is

$$\begin{aligned} V_{R3} &= V_{BE5} + R_1 I_{E5} = V_{BE6} + R_2 I_{E6} \\ &= V_T \ln \left(\frac{I_{C5}}{I_S} \right) + R_1 I_{E5} \\ &= 26 \text{ mV} \times \ln \left(\frac{9.5 \text{ } \mu\text{A}}{10^{-14}} \right) + 1 \text{ k}\Omega \times 9.5 \text{ } \mu\text{A} = 537.5 \text{ mV} + 9.5 \text{ mV} = 547 \text{ mV} \end{aligned} \quad (15.76)$$

The collector current of Q_7 is

$$I_{C7} \approx I_{E7} = V_{R3}/R_3 = 547 \text{ mV}/50 \text{ k}\Omega = 10.9 \text{ } \mu\text{A}$$

Gain Stage The gain stage provides a high voltage gain with a very high input and output resistance. The amplifier stage is shown in Fig. 15.27. Since it is assumed that the output voltage of the amplifier is zero, the base current of Q_{23} is zero and the collector current of Q_{17} is $I_{C17} = I_2 = 550 \text{ } \mu\text{A}$. The voltage at the base of Q_{17} is equal to the base-emitter voltage of Q_{17} plus the voltage drop across resistor R_8 . Assuming $I_{E17} = I_{C17}$, the voltage at the base of Q_{17} with respect to $-V_{EE}$ is

$$\begin{aligned} V_{B17} &= V_{BE17} + R_8 I_{E17} \\ &= V_T \ln \left(\frac{I_{C17}}{I_S} \right) + R_8 I_{E17} \\ &= V_T \ln \left(\frac{550 \text{ } \mu\text{A}}{10^{-14}} \right) + 100 \times 550 \text{ } \mu\text{A} = 642 \text{ mV} + 55 \text{ mV} = 697 \text{ mV} \end{aligned} \quad (15.77)$$

The current through R_9 is

$$I_{R9} = \frac{V_{B17}}{R_9} = \frac{697 \text{ mV}}{50 \text{ k}\Omega} = 13.94 \text{ } \mu\text{A}$$

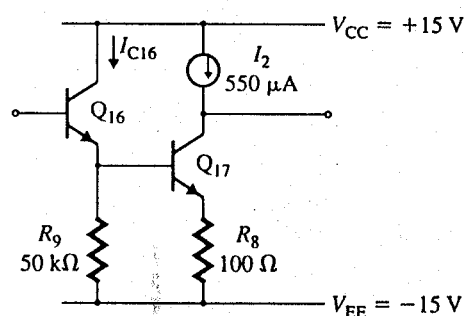
The base current of Q_{B17} is

$$I_{B17} = \frac{I_{C17}}{\beta_{F(\text{npn})}} = \frac{550 \text{ } \mu\text{A}}{250} = 2.2 \text{ } \mu\text{A}$$

The collector current of Q_{16} is

$$I_{C16} \approx I_{E16} = I_{B17} + I_{R9} = 2.2 \text{ } \mu\text{A} + 13.94 \text{ } \mu\text{A} = 16.14 \text{ } \mu\text{A}$$

FIGURE 15.27
Gain stage



which can be written as

$$V_T \ln \left(\frac{I_{C18}}{I_{S18}} \right) + V_T \ln \left(\frac{I_{C19}}{I_{S19}} \right) = V_T \ln \left(\frac{I_{C14}}{I_{S14}} \right) + V_T \ln \left| \frac{I_{C20}}{I_{S20}} \right| \quad (15.79)$$

For an output voltage of $v_O = 0$ and $\beta_{F(\text{nnpn})} \gg 1$,

$$|I_{C14}| = |I_{C20}| \quad (15.80)$$

and Eq. (15.79) can be simplified to

$$\frac{I_{C18} I_{C19}}{I_{S18} I_{S19}} = \frac{I_{C14}^2}{I_{S14} I_{S20}} \quad (15.81)$$

from which we get

$$I_{C14} = I_{C20} = \sqrt{I_{C18} I_{C19}} \sqrt{\frac{I_{S14} I_{S20}}{I_{S18} I_{S19}}} \quad (15.82)$$

Thus, the collector currents depend on the I_S values, which depend on the physical geometry of the transistors. Q_{14} and Q_{20} are normally designed to carry much larger current than other transistors. The specific geometries used by different manufacturers may be different, but the I_S value of Q_{14} and Q_{20} is typically three times that of Q_{18} and Q_{19} . Thus,

$$I_{S14} = I_{S20} \approx 3I_{S18} = 3I_{S19} \quad (15.83)$$

Substituting I_{S14} from Eq. (15.83) into Eq. (15.82) yields

$$\begin{aligned} I_{C14} = I_{C20} &= 3\sqrt{I_{C18} I_{C19}} \\ &= 3 \times \sqrt{(164.4 \mu\text{A})(15.6 \mu\text{A})} = 151.9 \mu\text{A} \end{aligned} \quad (15.84)$$

Overload Protection Transistor Q_{15} (in Fig. 15.23) turns on only when the voltage across R_6 exceeds 550 mV at an output sourcing current of $550 \text{ mV}/R_6 = 550 \text{ mV}/27 = 20 \text{ mA}$. When Q_{15} turns on, it limits the current to the base of Q_{14} and the output current cannot increase further. Thus, Q_{15} provides short-circuit protection, preventing damage to the op-amp due to excess current flow and power dissipation. These problems can occur if the output is shorted to a negative power supply. Similarly, transistors Q_{21} , Q_{22} , and Q_{24} protect transistor Q_{20} in the case of sinking current. When Q_{21} turns on, it protects Q_{20} by limiting the current to the base of Q_{20} , thereby turning on Q_{22} and Q_{24} .

If the inverting terminal were overdriven such that its voltage became more positive than that of the noninverting terminal, Q_1 would turn off. As a result, Q_6 would also be off and the current into the base of Q_{16} would be $I_T = 19.4 \mu\text{A}$. This current would be amplified by the beta of Q_{16} , which could be as high as 1000, giving a collector current of $I_{C16} = 1000 \times 19.4 \mu\text{A} \approx 19.4 \text{ mA}$ that would flow into the base of Q_{17} . Q_{17} would thus become saturated. Saturation would result in a power dissipation in Q_{16} of

$$I_{C6}(V_{CC} + V_{EE}) = 19.4 \text{ mA} \times 30 \text{ V} \approx 580 \text{ mW}$$

The extra emitter on Q_{23} prevents Q_{17} from developing a high current condition that could damage Q_{16} .

Small-signal analysis is performed to determine the input resistance, the output resistance, the transconductance, and the voltage gain. The op-amp circuit may be broken up into three stages: the input stage, the gain stage, and the output stage. Since the op-amp may be considered as three cascaded stages, we shall represent the input and gain stages by their transconductance equivalents to simplify the analysis to determine the overall gain.

Notice from Eq. (15.24) that the CMRR is the change in the common-mode voltage per unit change in the input offset voltage ΔV_{OS} , which can be determined from Eq. (15.23) if A_d is known. Thus, we need to determine only A_d . The small-signal parameters of the transistors are

$$r_{\pi 16} = \frac{\beta_{F16} V_T}{I_{C16}} = \frac{250 \times 26 \text{ mV}}{16.1 \mu\text{A}} = 403.7 \text{ k}\Omega$$

$$r_{\pi 17} = \frac{\beta_{F17} V_T}{I_{C17}} = \frac{250 \times 26 \text{ mV}}{550 \mu\text{A}} = 11.82 \text{ k}\Omega$$

$$r_{\pi 23} = \frac{\beta_{F23} V_T}{I_{C23}} = \frac{250 \times 26 \text{ mV}}{180 \mu\text{A}} = 36.1 \text{ k}\Omega$$

$$g_{m3} = g_{m4} = g_{m5} = g_{m6} = \frac{I_{C3}}{V_T} = \frac{I_{C4}}{V_T} = \frac{I_{C6}}{V_T} = \frac{9.5 \mu\text{A}}{26 \text{ mV}} = 365.4 \mu\text{A/V}$$

$$g_{m13A} = g_{m23} = \frac{I_{C13A}}{V_T} = \frac{180 \mu\text{A}}{26 \text{ mV}} = 6.92 \text{ mA/V}$$

$$g_{m13B} = g_{m17} = \frac{I_{C17}}{V_T} = \frac{550 \mu\text{A}}{26 \text{ mV}} = 21.15 \text{ mA/V}$$

The output resistance r_o is given by

$$r_o = \frac{V_A}{I_C} = \frac{V_A}{V_T g_m} = \frac{1}{\eta_n g_m} \quad (15.85)$$

where $\eta_n = V_T/V_A$ is a transistor constant. Assuming $\eta_n = 5 \times 10^{-4}$ for *pnp* transistors, Eq. (15.85) gives

$$r_{o4} = \frac{1}{\eta_n g_{m4}} = \frac{1}{5 \times 10^{-4} \times 365.4 \mu\text{A/V}} = 5.47 \text{ M}\Omega$$

$$r_{o13A} = r_{o23} = \frac{1}{\eta_n g_{m13A}} = \frac{1}{5 \times 10^{-4} \times 6.92 \text{ mA/V}} = 289 \text{ k}\Omega$$

$$r_{o13B} = \frac{1}{\eta_n g_{m13B}} = \frac{1}{5 \times 10^{-4} \times 21.15 \text{ mA/V}} = 94.56 \text{ k}\Omega$$

Assuming $\eta_n = 2 \times 10^{-4}$ for *nnp* transistors, Eq. (15.85) gives

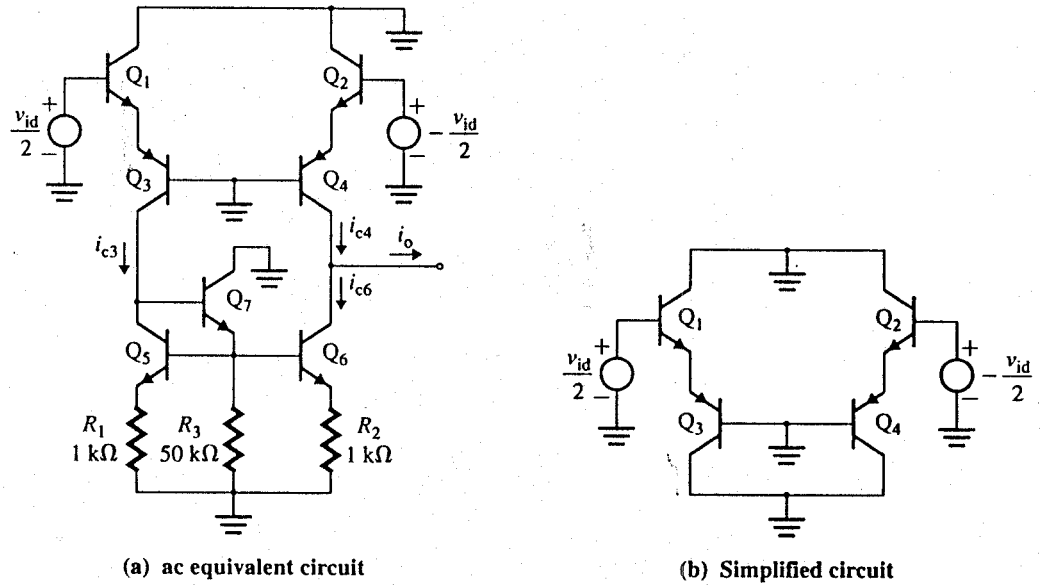
$$r_{o6} = \frac{1}{\eta_n g_{m6}} = \frac{1}{2 \times 10^{-4} \times 365.4 \mu\text{A/V}} = 13.68 \text{ M}\Omega$$

$$r_{o17} = \frac{1}{\eta_n g_{m17}} = \frac{1}{2 \times 10^{-4} \times 21.15 \text{ mA/V}} = 236.4 \text{ k}\Omega$$

Input Stage Let us assume that $v_{ic} = 0$ and only $v_{id}/2$ is applied. The ac equivalent circuit for the differential-mode signal is shown in Fig. 15.29(a). The input voltage to transistor Q_1 is $+v_{id}/2$, and that to transistor Q_2 is $-v_{id}/2$. Assuming that the transistors are identical and the circuit is balanced, an increase in voltage at the base junction of Q_3 and Q_4 due to $+v_{id}/2$ will be compensated by an equal decrease in voltage due to $-v_{id}/2$. The voltage at the base terminals of *pnp* transistors Q_3 and Q_4 will not vary at all. As a result, the bases of Q_3 and Q_4 are effectively at ground potential.

The transconductance of the input stage can be found by shorting the output to the ground and calculating the resulting current. Since $i_{c3} = i_{c5}$ and i_{c6} is the current mirror of

FIGURE 15.29
ac equivalent of input
stage with differential
input



i_{c5} , the current in the active load circuit (i_{c6}) will be equal in magnitude to the collector current of Q_3 (i_{c3}). That is,

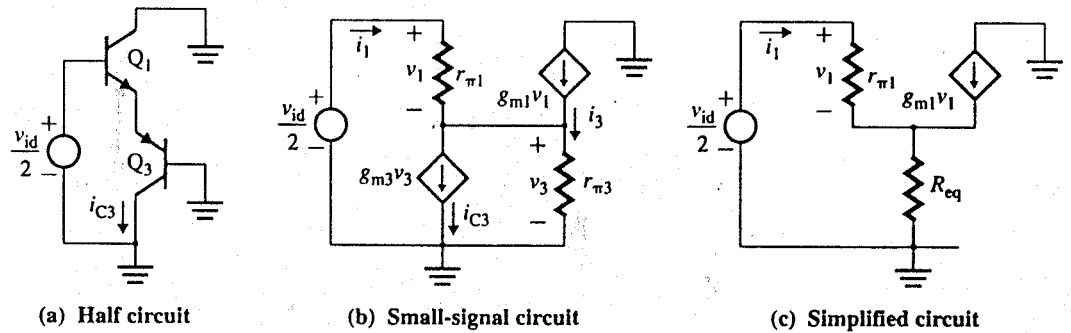
$$i_{c6} = i_{c3} \quad (15.86)$$

Thus, the output current under short-circuit conditions is

$$i_o = i_{c4} - i_{c6} = i_{c4} - i_{c3} \quad (15.87)$$

Under these conditions, Fig. 15.29(a) can be reduced to Fig. 15.29(b), which has two identical sides. The half-circuit ac equivalent is shown in Fig. 15.30(a), and its small-signal equivalent circuit is shown in Fig. 15.30(b), which can be simplified to Fig. 15.30(c).

FIGURE 15.30
Half-circuit ac equivalent
for differential input



From Fig. 15.30(b),

$$\frac{v_{id}}{2} = v_1 + v_3 \quad (15.88)$$

Summing the currents at the emitter junction, we get

$$g_{m1}v_1 + i_1 = g_{m3}v_3 + i_3 \quad (15.89)$$

Substituting for i_1 and i_3 , we get

$$g_{m1}v_1 + \frac{g_{m1}v_1}{\beta_{F1}} = g_{m3}v_3 + \frac{g_{m3}v_3}{\beta_{F3}}$$

$$\text{or} \quad g_{m1}v_1 \left[1 + \frac{1}{\beta_{F1}} \right] = g_{m3}v_3 \left[1 + \frac{1}{\beta_{F3}} \right] \quad (15.90)$$

where β_{Fi} is the small-signal current gain of the i th transistor. Since $|I_{C1}| = |I_{C3}|$, $g_{m1} \approx g_{m3}$. Assuming that $\beta_{F1} \gg 1$ and $\beta_{F3} \gg 1$, Eq. (15.90) is reduced to

$$v_1 = v_3 \quad (15.91)$$

and Eq. (15.88) becomes

$$\frac{v_{id}}{2} = v_1 + v_3 = v_3 + v_3 = 2v_3$$

$$\text{or} \quad v_3 = \frac{v_{id}}{4} \quad (15.92)$$

Using Eq. (15.92), we can find the collector current of Q_3 :

$$i_{c3} = g_{m3}v_3 = \frac{g_{m3}v_{id}}{4} \quad (15.93)$$

From the symmetry of the circuit in Fig. 15.29(a), we get

$$i_{c4} = -i_{c3} = \frac{g_{m3}v_{id}}{4} \quad (15.94)$$

Substituting i_{c3} from Eq. (15.93) and i_{c4} from Eq. (15.94) into Eq. (15.87), we get the output current as

$$i_o = \frac{g_{m3}v_{id}}{4} + \frac{g_{m3}v_{id}}{4} = \frac{g_{m3}v_{id}}{2} \quad (15.95)$$

which gives the transconductance of the input stage as

$$\begin{aligned} G_{m1} &= \frac{i_o}{v_{id}} = \frac{g_{m3}}{2} \\ &= \frac{I_{C3}}{2V_T} = \frac{9.5 \mu\text{A}}{2 \times 26 \text{ mV}} = \frac{1}{5.47 \text{ k}\Omega} = 182.7 \mu\text{A/V} \end{aligned} \quad (15.96)$$

Q_3 can be replaced by the equivalent resistance R_{eq} seen looking from the emitter of Q_3 , as shown in Fig. 15.30(c). R_{eq} can be found from

$$R_{eq} = \frac{v_3}{g_{m3}v_3 + v_3/r_{\pi3}} = \frac{1}{g_{m3} + 1/r_{\pi3}} = \frac{1}{g_{m3}(1 + 1/\beta_{F3})} \quad (15.97)$$

$$\approx \frac{1}{g_{m3}} = \frac{r_{\pi3}}{\beta_{F3}} = \frac{r_{\pi1}}{\beta_{F1}} \quad (15.98)$$

Using Eq. (5.28), we can relate v_{id} to i_1 as follows:

$$\frac{v_{id}/2}{i_1} = r_{\pi1} + R_{eq}(1 + \beta_{F1}) \quad (15.99)$$

Substituting $R_{eq} = r_{\pi1}/\beta_{F1}$ from Eq. (15.98) into Eq. (15.99) gives the input resistance as

$$\begin{aligned} R_{id} &= \frac{v_{id}}{i_1} = 2 \left[r_{\pi1} + \frac{r_{\pi1}}{\beta_{F1}} (1 + \beta_{F1}) \right] \\ &\approx 4r_{\pi1} \\ &= 4 \frac{\beta_{F1} V_T}{I_{C1}} = 4 \times \frac{250 \times 26 \text{ mV}}{9.69 \mu\text{A}} = 2.68 \text{ M}\Omega \end{aligned} \quad (15.100)$$

Notice from Eq. (15.100) that the input resistance is four times the input resistance of the input transistors. Also note that when v_{id} changes, the output voltage changes and produces feedback to the input through the output resistance of Q_4 . As a result, the input resistances seen from the two input terminals will not be exactly the same. This effect is neglected in the derivation of R_{id} .

The output resistance R_{o1} can be determined by setting the input voltage to zero and applying a test voltage v_x , as shown in Fig. 15.31(a). The analysis can be simplified by making the following assumptions:

1. Thevenin's equivalent resistance R_{th6} at the base of Q_6 is very small compared to r_{π} of Q_6 , so the base of Q_6 is grounded. In reality, the voltage at this point is very small, and this point may be considered a virtual ground without greatly affecting the results. That is, $v_{B6} \approx 0$. Figure 15.31(a) can be viewed as shown in Fig. 15.31(b).
2. The output resistance of Q_2 is large and does not affect the results.

Figure 15.31(b) can be further simplified to the half circuit shown in Fig. 15.31(c). If Q_2 is replaced by $1/g_{m2}$, Fig. 15.31(c) can be represented by the equivalent circuit in Fig. 15.32(a). If R_{Q4} and R_{Q6} are the effective resistances seen from the collectors of Q_4 and Q_6 , respectively, Fig. 15.32(a) can be represented by Fig. 15.32(b). Using Eq. (13.31), we get

$$R_{Q4} = r_{o4} \left[\frac{1 + g_{m4}(1/g_{m4})}{1 + g_{m4}/\beta_{F4}g_{m2}} \right] \quad (15.101)$$

$$\approx 2r_{o4}$$

$$= 2 \times 5.47 \text{ M}\Omega = 10.94 \text{ M}\Omega$$

$$\text{and} \quad R_{Q6} = r_{o6} \left[\frac{1 + g_{m6}R_2}{1 + g_{m6}R_2/\beta_{F6}} \right] \quad (15.102)$$

$$= r_{o6} \left[\frac{1 + 365.4 \mu\text{A/V} \times 1 \text{ k}\Omega}{1 + 365.4 \mu\text{A/V} \times 1 \text{ k}\Omega/250} \right] = 1.36r_{o6}$$

$$= 1.36 \times 13.68 \text{ M}\Omega = 18.65 \text{ M}\Omega$$

FIGURE 15.31 Test circuit for calculation of R_{o1}

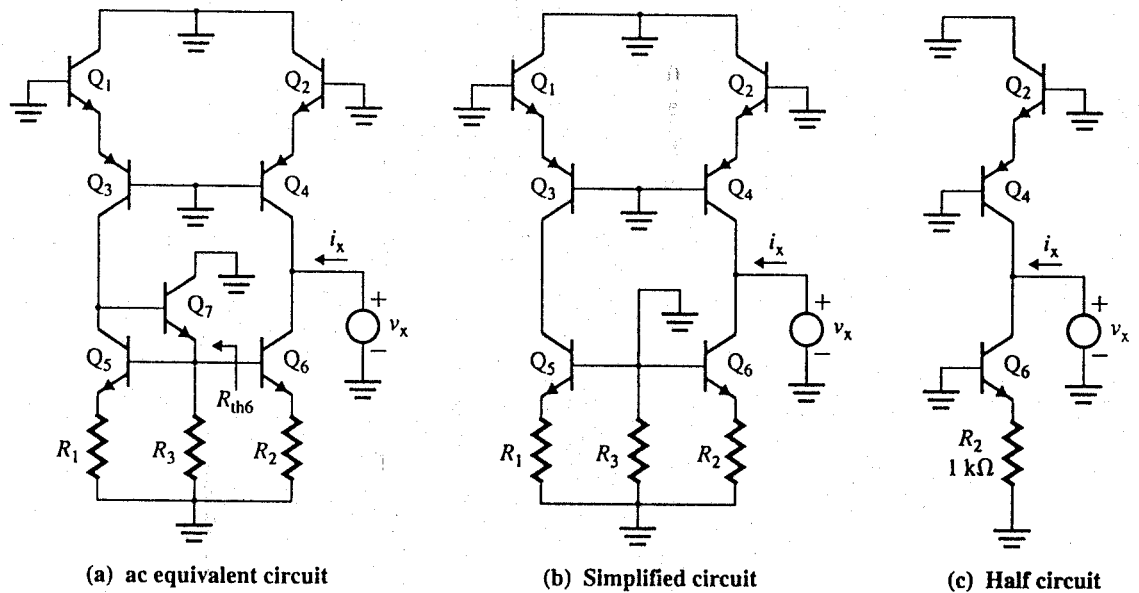
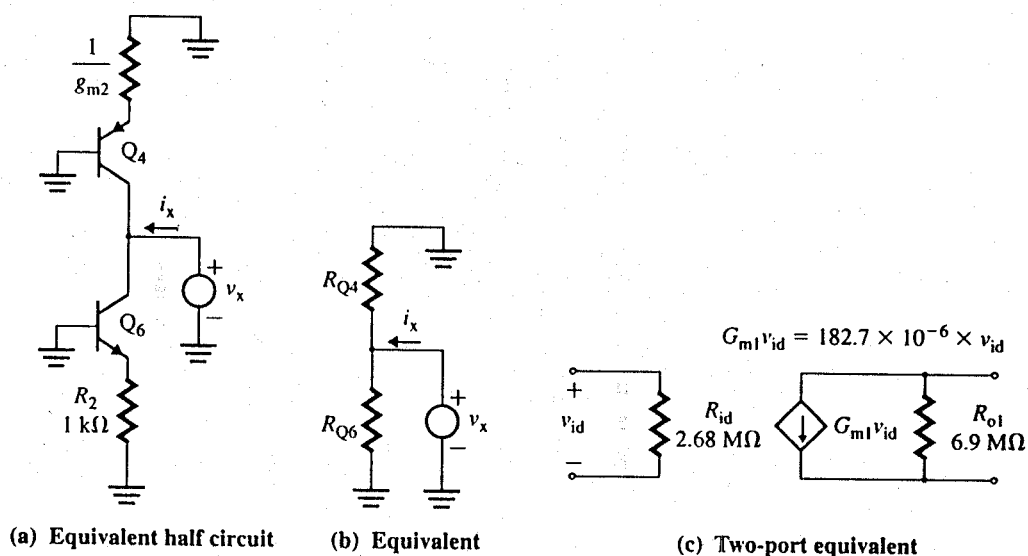


FIGURE 15.32
Two-port equivalent of
the input stage



The output resistance of the input stage is

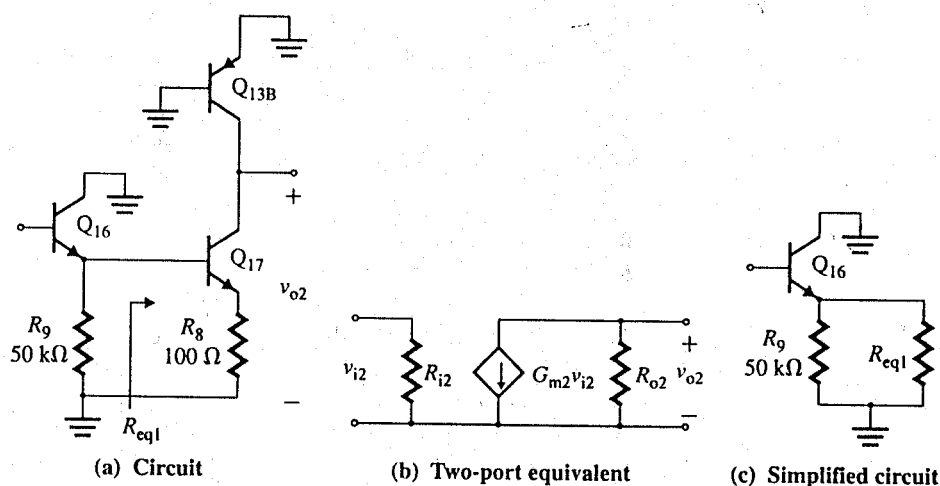
$$R_{o1} = R_{Q4} \parallel R_{Q6} = 10.94 \text{ M}\Omega \parallel 18.65 \text{ M}\Omega = 6.9 \text{ M}\Omega$$

The two-port equivalent circuit of the input stage is shown in Fig. 15.32(c).

Gain Stage The ac equivalent for the gain stage, shown in Fig. 15.33(a), can be represented by the equivalent circuit shown in Fig. 15.33(b). If R_{eq1} is Thevenin's equivalent resistance seen looking into the base of transistor Q_{17} , Fig. 15.33(a) can be reduced to the form shown in Fig. 15.33(c). From Eq. (5.28), we can find the input resistance of a common-emitter amplifier with a resistance in the emitter as follows:

$$\begin{aligned} R_{eq1} &= r_{\pi 17} + (1 + \beta_{F17})R_8 \\ &= 11.82 \text{ k}\Omega + (1 + 250) \times 100 = 36.9 \text{ k}\Omega \end{aligned} \quad (15.103)$$

FIGURE 15.33
Small-signal ac equivalent
circuit for the gain stage



The input resistance of the stage is

$$\begin{aligned} R_{i2} &= r_{\pi 16} + (1 + \beta_{F16})(R_{eq1} \parallel R_9) \\ &= 403.7 \text{ k}\Omega + (1 + 250)(36.9 \text{ k}\Omega \parallel 50 \text{ k}\Omega) = 5.73 \text{ M}\Omega \end{aligned} \quad (15.104)$$

Assuming that the voltage gain of the emitter follower Q_{16} is unity, the transconductance G_{m2} of this stage is that of the common-emitter amplifier of Q_{17} with resistance in the emitter:

$$\begin{aligned} G_{m2} &= \frac{g_{m17}}{1 + g_{m17}R_8} \\ &= \frac{21.15 \text{ mA/V}}{1 + 21.15 \text{ mA/V} \times 100} = \frac{1}{147 \Omega} \approx 6.79 \text{ mA/V} \end{aligned} \quad (15.105)$$

The circuit for determining the output resistance is shown in Fig. 15.34(a). The small-signal ac equivalent is shown in Fig. 15.34(b). If R_{Q13B} and R_{Q17} are the effective resistances seen from the collectors of Q_{13B} and Q_{17} , respectively, Fig. 15.34(b) can be represented by the equivalent circuit in Fig. 15.34(c) and

$$R_{Q13B} = r_{o13B} = 94.56 \text{ k}\Omega$$

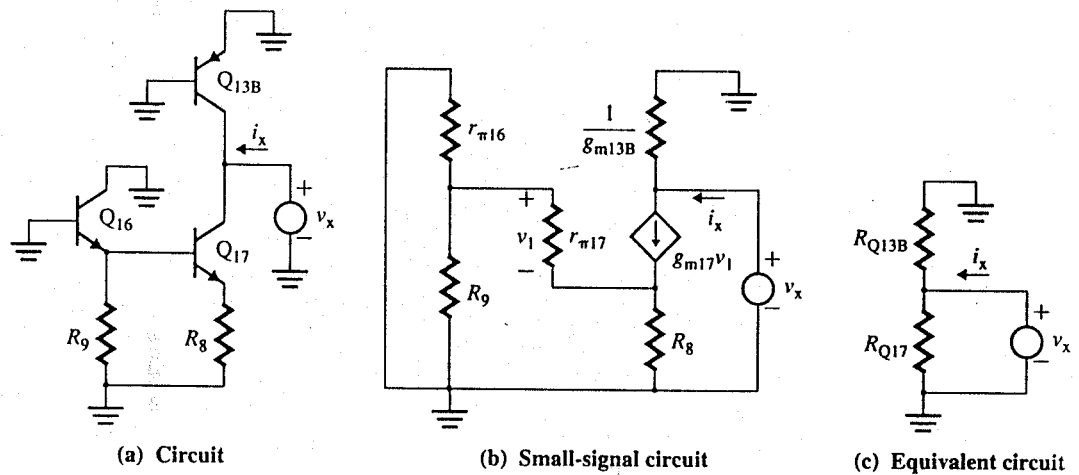
Using Eq. (13.31), we get

$$\begin{aligned} R_{Q17} &\approx r_{o17} \left[\frac{1 + g_{m17}R_8}{1 + g_{m17}R_8/\beta_{F17}} \right] \\ &\approx r_{o17} \left[\frac{1 + 21.15 \text{ mA/V} \times 100}{1 + 21.15 \text{ mA/V} \times 100/250} \right] = 3.09 r_{o17} \\ &= 3.09 \times 236.4 \text{ k}\Omega = 730.5 \text{ k}\Omega \end{aligned} \quad (15.106)$$

The output resistance of the gain stage is

$$R_{o2} = R_{Q13B} \parallel R_{Q17} = 94.56 \text{ k}\Omega \parallel 730.5 \text{ k}\Omega = 83.72 \text{ k}\Omega$$

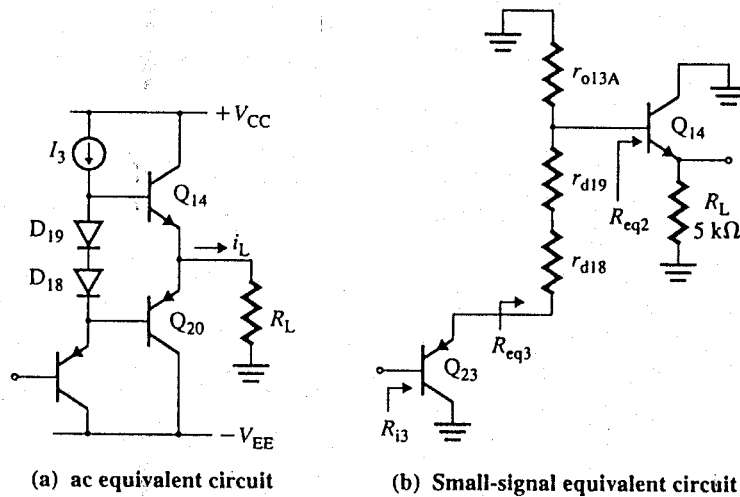
FIGURE 15.34
ac equivalent circuit for
calculation of R_{o2}



Output Stage Since V_{CE} of transistor Q_{18} is the sum of the V_{BE} voltages of Q_{18} and Q_{19} , transistors Q_{18} and Q_{19} can be replaced by diodes, as shown in Fig. 15.35(a). The output could be either sourcing or sinking, depending on the output voltage and the load. As a result, the input and resistances of this stage greatly depend on the particular values of output voltage and current. We will make the following assumptions:

1. The output is sourcing—that is, the output current is flowing out of the output stage.
2. The load current is $i_L = 2 \text{ mA}$ at $R_L = 5 \text{ k}\Omega$.

FIGURE 15.35
ac equivalent circuit for
the output stage



3. Transistor Q_{14} is in the active region.

4. Transistor Q_{20} is conducting a very small amount of current and is considered to be off.

The small-signal ac equivalent of Fig. 15.35(a) is shown in Fig. 15.35(b). Notice that the circuit consists of two emitter followers in series and that the voltage gain is approximately unity. Thus,

$$A_3 \approx 1 \quad (15.107)$$

Since Q_{14} carries the load current i_L and a no-load dc biasing current of $151.4 \mu\text{A}$,

$$I_{C14} = 2 \text{ mA} + 151.4 \mu\text{A} = 2.15 \text{ mA}$$

Thus,

$$r_{\pi 14} = \frac{\beta_{F14} V_T}{I_{C14}} = \frac{250 \times 26 \text{ mV}}{2.15 \text{ mA}} = 3.02 \text{ k}\Omega$$

Since Q_{23} and diodes D_{18} and D_{19} operate at a current of $180 \mu\text{A}$,

$$r_{d18} = r_{d19} = \frac{V_T}{I_{d18}} = \frac{26 \text{ mV}}{180 \mu\text{A}} = 144 \Omega$$

If R_{eq2} is the resistance seen looking at the base of Q_{14} , we can use Eq. (5.28) to find R_{eq2} :

$$\begin{aligned} R_{eq2} &= r_{\pi 14} + (1 + \beta_{F14})R_L \\ &= 3.02 \text{ k}\Omega + (1 + 250) \times 5 \text{ k}\Omega = 1258 \text{ k}\Omega \end{aligned} \quad (15.108)$$

Thevenin's equivalent resistance seen looking from the emitter of Q_{23} can be found from

$$\begin{aligned} R_{eq3} &= r_{d18} + r_{d19} + r_{o13A} \parallel R_{eq2} \\ &= 144 \Omega + 144 \Omega + (289 \text{ k}\Omega \parallel 1258 \text{ k}\Omega) = 235.3 \text{ k}\Omega \end{aligned} \quad (15.109)$$

Using Eq. (5.28), we can find the input resistance of the stage:

$$\begin{aligned} R_{i3} &= r_{\pi 23} + (1 + \beta_{F23})R_{eq3} \\ &= 36.1 \text{ k}\Omega + (1 + 50) \times 235.3 \text{ k}\Omega = 12.04 \text{ M}\Omega \end{aligned} \quad (15.110)$$

Notice that the input resistance of the output stage ($12.04 \text{ M}\Omega$) is much larger than the output resistance of the preceding stage ($83.72 \text{ k}\Omega$). As a result, the overall gain of the amplifier is not affected by the variations in external load resistance.

The output resistance of the output stage can be determined from the ac equivalent circuit shown in Fig. 15.36(a), which includes the output resistance R_{o2} of the preceding stage. Converting R_{o2} at the base of Q_{23} to its emitter gives the equivalent resistance seen looking from the base of Q_{14} toward Q_{23} :

$$\begin{aligned} R_{eq4} &= r_{d18} + r_{d19} + \frac{R_{o2} + r_{\pi23}}{1 + \beta_{F23}} \\ &= 144 + 144 + \frac{83.72 \text{ k}\Omega + 36.1 \text{ k}\Omega}{1 + 50} = 2.64 \text{ k}\Omega \end{aligned} \quad (15.111)$$

The resistance seen looking from the base of Q_{14} to the left is

$$\begin{aligned} R_{eq5} &= r_{o13A} \parallel R_{eq4} \\ &= 289 \text{ k}\Omega \parallel 2.64 \text{ k}\Omega = 2.62 \text{ k}\Omega \end{aligned} \quad (15.112)$$

The resistance seen looking into the output terminal is

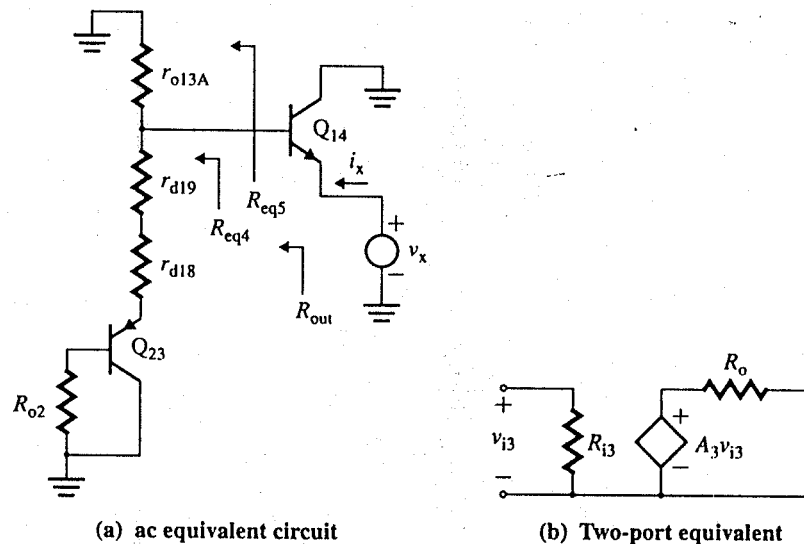
$$\begin{aligned} R_{out} &= \frac{R_{eq5} + r_{\pi14}}{1 + \beta_{F14}} \\ &= \frac{2.62 \text{ k}\Omega + 3.02 \text{ k}\Omega}{1 + 250} = 22.5 \Omega \end{aligned} \quad (15.113)$$

The current-limiting resistance R_6 must be added to R_{out} to find the actual output resistance of the op-amp:

$$\begin{aligned} R_o &= R_{out} + R_6 \\ &= 22.5 + 27 = 49.5 \Omega \end{aligned} \quad (15.114)$$

The two-port equivalent circuit of the output stage is shown in Fig. 15.36(b).

FIGURE 15.36
ac equivalent circuit for
calculation of R_o



Analysis of Frequency Response

For $G_{m1} = 182.7$ and $C_x = 30$ pF, Eq. (15.45) gives the unity-gain frequency (or bandwidth) as

$$f_u = \frac{G_{m1}}{2\pi C_x} = \frac{182.7 \mu}{2\pi \times 30 \text{ pF}} = 969.2 \text{ kHz}$$

From Eq. (15.53), the slew rate is

$$SR = 4\pi V_T f_u = 4\pi \times 25.8 \text{ m} \times 969.3 \text{ k} = 0.314 \text{ V}/\mu\text{s}$$

Small-Signal Equivalent Circuit

The manufacturer-specified values are $f_u = 1$ MHz and $SR = 0.5$ V/ μ s. The discrepancy between the calculated values and the manufacturer-specified values is caused by the fact that Eq. (15.53) gives an approximate value of SR and does not take into account the input and output resistances of preceding and subsequent amplifier stages.

The small-signal equivalent of the complete circuit is shown in Fig. 15.37. The voltage gain is

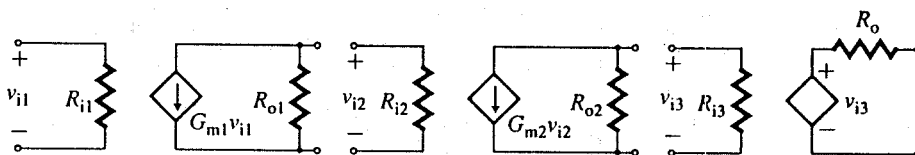
$$\begin{aligned} A_v &= G_{m1}(R_{o1} \parallel R_{i2})G_{m2}(R_{o2} \parallel R_{i3}) \\ &= 182.7 \mu\text{A/V} \times (6.89 \text{ M}\Omega \parallel 5.73 \text{ M}\Omega) \times 6.79 \text{ mA/V} \times (83.72 \text{ k}\Omega \parallel 12.4 \text{ M}\Omega) \\ &= 571.5 \times 564.6 = 323\,000 \end{aligned} \quad (15.115)$$

Resistances are

$$R_{id} = 2.68 \text{ M}\Omega$$

$$R_o = 49.5 \Omega$$

FIGURE 15.37
Small-signal equivalent
circuit for the LM741
op-amp



► NOTES:

1. The input stage and the gain stage contribute about the same gain: 571.5 and 564.6, respectively. The gain stage loads the input stage and reduces its gain by about half. This loading makes the op-amp beta-dependent, causing the gain to vary with temperature and fabrication-process tolerances.
2. The output stage does not significantly load the gain stage, and the voltage gain is almost independent of the external load resistance.
3. Although the results of the analysis are approximate, they give insight into the operation and performance of the op-amp.
4. The output resistances of transistors were neglected in the dc analysis. If these were taken into consideration, the biasing currents would change, thereby changing the small-signal output resistance and the results.
5. The variation in the transistor beta was neglected. But the transistor current gain falls at low collector current levels because of recombination in the emitter-base space charge layer.

KEY POINTS OF SECTION 15.8

- This section illustrated a three-part analysis of a complete op-amp circuit, the LM741: dc analysis to find the dc biasing currents, small-signal analysis to find the voltage gain, and analysis of the frequency response to find the unity-gain bandwidth for all stages of the op-amp.
- The values obtained from hand calculations correspond well to the values specified in the manufacturer's data sheet. That is, $A_v = 323\,000$ (compared to 200 000), $R_{id} = 2.68 \text{ M}\Omega$ (compared to 2 M Ω), $R_o = 50 \Omega$ (compared to 75 Ω), $f_u = 969.2 \text{ kHz}$ (compared to 1 MHz), and $SR = 0.314 \text{ V}/\mu\text{s}$ (compared to 0.5 V/ μ s).

15.9 Design of Op-Amps

An operational amplifier is a complete integrated circuit that is expected to meet certain specifications with respect to input resistance, output resistance, gain, CMRR, and bandwidth. An op-amp is designed at the system level. The process involves designing the amplifying stages and protection circuitry and requires the following steps:

- Step 1.** Identify the important specifications: the voltage gain A_d , the CMRR, the input resistance R_{id} , the output resistance R_o , the unity-gain bandwidth, and the dc supply voltages V_{CC} and V_{EE} (or V_{DD} and V_{SS}).
- Step 2.** Select the type of op-amp (bipolar, BiFET, CMOS, or BiCMOS).
- Step 3.** Choose the circuit configurations and stages.
- Step 4.** Determine the biasing current requirement I_Q for the desired specifications.
- Step 5.** Choose the type of current source (BJT or MOSFET), and determine its component ratings.
- Step 6.** Choose the active load with a current mirror (BJT or MOSFET) in order to obtain the desired voltage gain, and determine its component ratings.
- Step 7.** Choose the type of gain stage (BJT or MOSFET), and determine its component ratings.
- Step 8.** Choose the type of output stage (BJT or MOSFET), and determine its component ratings.
- Step 9.** Choose the type of frequency compensation (pole or pole-zero circuit), and determine its component ratings.
- Step 10.** Determine the voltage, current, and power ratings of active and passive components.
- Step 11.** Analyze and evaluate the complete differential amplifier to see that it meets the desired specifications.
- Step 12.** Use PSpice/SPICE to simulate and verify your design. If it would be implemented with discrete devices, use standard values of components, with tolerances of, say, 5%.

Summary

The internal structure of an op-amp usually consists of differential, gain, and output stages. There are many possible combinations of op-amp stages, depending on whether the amplifier is a bipolar, JFET, or CMOS op-amp. In general, an FET op-amp gives a very high input resistance but less gain, whereas a bipolar op-amp gives a higher gain but lower input resistance. A Darlington BJT pair is commonly used for high current gain and input resistance. A difference output of a differential stage gives less gain but yields wider bandwidth.

Op-amps exhibit offset voltages and currents, which can be minimized by appropriate internal design. The input offset voltage is dependent on the CMRR and the common-mode signal. A pole or pole-zero compensation circuit is commonly used for frequency compensation, but the compensation comes at the expense of unity-gain bandwidth.

The small-signal voltage gain and the input and output resistances of the LM741 op-amp can be determined for various load conditions. Since the voltage gain is very high, the amplifier offers offset voltages and currents because of variations in the transistor parameters and circuit resistances. Although the analysis required to derive equations describing the characteristics of current sources and differential amplifiers can be simplified with some assumptions, computer-aided analysis is generally required to evaluate the actual performance of an op-amp at the final design stage. The analysis of other op-amps would be similar to the analysis of the LM741 op-amp in this chapter.

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Review Questions

1. What are the main stages of an op-amp?
2. What is the input biasing current of an op-amp?
3. What is the input offset current of an op-amp and what factors influence its value?
4. What is the input offset voltage of an op-amp and what factors influence its value?
5. What is the CMRR of an op-amp?
6. What factors influence the unity-gain bandwidth of an op-amp?
7. What factors influence the slew rate of an op-amp?
8. What is the relation between slew rate and unity-gain bandwidth?
9. What is pole-zero compensation of an op-amp?
10. What circuit configurations are used for ultrafast op-amps?
11. What are the advantages and disadvantages of JFET op-amps?
12. What are the advantages and disadvantages of bipolar op-amps?
13. What are the advantages and disadvantages of CMOS op-amps?
14. What are the advantages and disadvantages of BiCMOS op-amps?
15. What is the function of short-circuit protection in op-amps?
16. What are the typical values of input resistance, output resistance, and voltage gain for the LM741 op-amp?

Problems

The symbol **D** indicates that a problem is a design problem. The symbol **P** indicates that you can check the solution to a problem using PSpice/SPICE or Electronics Workbench.

► 15.3 Op-Amp Parameters

- 15.1 The Darlington pair shown in Fig. 15.4 is biased in such a way that the collector biasing current I_{C2} of Q_2 is $400\ \mu\text{A}$. The current gains of the two transistors are the same, $\beta_{F1} = \beta_{F2} = 80$, and the Early voltage is $V_A = 50\ \text{V}$. Calculate (a) the effective input resistance r_π , (b) the effective transconductance g_m , (c) the effective current gain $\beta_{F(\text{eff})}$, and (d) the effective output resistance r_o .

► 15.4 JFET Op-Amps

- 15.2 The JFETs of the op-amp in Fig. 15.11 have $I_{\text{DDs}} = 500\ \mu\text{A}$ and $V_p = -4\ \text{V}$. The biasing current is $I_Q = 200\ \mu\text{A}$.
- (a) If the input biasing current is $I_B = 1.0\ \text{nA}$ at 25°C and doubles for every 10°C temperature rise, find the input biasing current I_B at 75°C , 100°C , and 125°C .
 - (b) If I_{DDs} changes by 2%, find the input offset voltage V_{OS} and the thermal drift D_v .
- 15.3 The biasing current for the JFET op-amp in Fig. 15.11 is $I_Q = 200\ \mu\text{A}$, and the compensation capacitance is $C_x = 30\ \text{pF}$. Find (a) the slew rate SR and (b) the unity-gain bandwidth f_u .

► 15.5 CMOS Op-Amps

- 15.4 The CMOS of the op-amp in Fig. 15.18 has $K_x = 10\ \mu\text{A}/\text{V}^2$, $W/L = 160\ \mu\text{m}/10\ \mu\text{m}$, and $V_t = 0.5\ \text{V}$. The biasing current is $I_Q = 40\ \mu\text{A}$. If V_t changes by 2% and W/L by 1%, find the input offset voltage V_{OS} .
- D** 15.5 The CMOS amplifier in Fig. 15.18 is operated at a biasing current of $I_Q = 50\ \mu\text{A}$. The parameters of the MOSFETs are $K_x = 10\ \mu\text{A}/\text{V}^2$, $|V_{M(\text{NMOS})}| = V_{N(\text{PMOS})} = 60\ \text{V}$, $V_t = 1\ \text{V}$, and

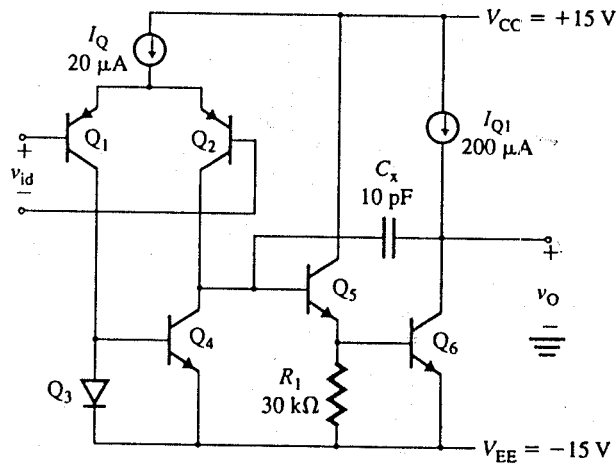
$W/L = 80 \mu\text{m}/10 \mu\text{m}$, except for Q_7 , for which $W/L = 160 \mu\text{m}/10 \mu\text{m}$. Assume $V_{DD} = -V_{SS} = 5 \text{ V}$.

- Find V_{GS} , g_m , and r_o for all MOSFETs.
- Find the low-frequency voltage gain of the amplifier A_{vo} .
- Find the value of the external resistance R_{ref} .
- Find the value of compensation capacitance C_x that gives a unity-gain bandwidth of 1 MHz and the corresponding slew rate.
- Find the value of resistance R_x to be connected in series with C_x in order to move the zero frequency to infinity.
- Find the common-mode input voltage range.
- Find the output voltage range.

► **15.7 BJT Op-Amps**

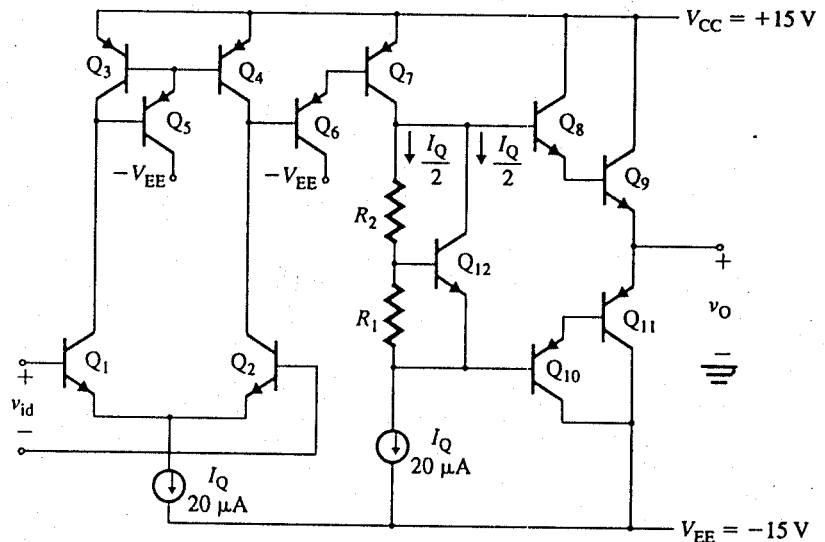
- 15.6** The BJTs for the op-amp shown in Fig. P15.6 have $\beta_{F(\text{nnp})} = 100$, $\beta_{F(\text{pnp})} = 50$, $V_{A(\text{pnp})} = V_{A(\text{nnp})} = 80 \text{ V}$, $V_{BE} = 0.6 \text{ V}$, and $I_S = 10^{-14} \text{ A}$. Find (a) the input biasing current I_B , (b) the input resistance R_i , (c) the unity-gain bandwidth f_u and the slew rate, and (d) the overall low-frequency voltage gain A_{vo} . Assume $V_{CC} = -V_{EE} = 15 \text{ V}$.

FIGURE P15.6



- 15.7** The BJTs for the op-amp shown in Fig. P15.7 have $\beta_{F(\text{nnp})} = 100$, $\beta_{F(\text{pnp})} = 50$, $V_{A(\text{pnp})} = V_{A(\text{nnp})} = 80 \text{ V}$, $V_{BE} = 0.6 \text{ V}$, and $I_S = 10^{-14} \text{ A}$. Find (a) the input biasing current I_B , (b) the input resistance R_i , and (c) the overall low-frequency voltage gain A_{vo} . Assume $V_{CC} = -V_{EE} = 15 \text{ V}$.

FIGURE P15.7



- 15.8** The BJTs for the LM124 op-amp shown in Fig. 15.22 have $\beta_{F(\text{nnp})} = 100$, $\beta_{F(\text{pnp})} = 50$, $V_{A(\text{pnp})} = V_{A(\text{nnp})} = 80 \text{ V}$, $V_{BE} = 0.6 \text{ V}$, and $I_S = 10^{-14} \text{ A}$. Assume $V_{CC} = 12 \text{ V}$. Find (a) the input biasing current I_B , (b) the input resistance R_i , (c) the unity-gain bandwidth f_u and the slew rate, (d) the overall low-frequency voltage gain A_{vo} , and (e) the value of R_{SC} for a short-circuit current limit of 25 mA.

► **15.8** *Analysis of the LM741 Op-Amp*

- 15.9** Calculate the gain of the LM741 op-amp in Fig. 15.23 if R_g is reduced from 100Ω to 0.
- 15.10** Calculate the gain of the LM741 op-amp in Fig. 15.23 if the current gain for *nnp* transistors is changed from $\beta_F = 250$ to $1.1 \times 250 = 275.0$ and the saturation current is changed from $I_S = 10^{-14} \text{ A}$ to $1.05 \times 10^{-14} \text{ A}$.
- 15.11** Calculate the gain of the LM741 op-amp in Fig. 15.23 if all resistances are increased by 1%.
- 15.12** Calculate the gain of the LM741 op-amp in Fig. 15.23 if all resistances are decreased by 1%.