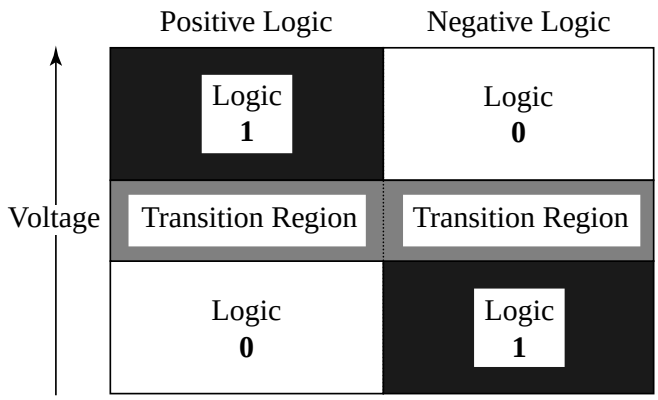
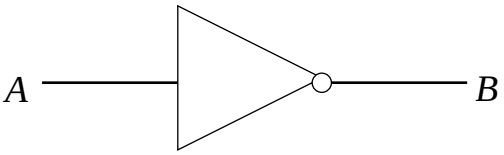
Digital Electronics

- Assign “1” and “0” to a range of voltage (or current), with a separation that minimizes a transition region



We will use positive logic (usually the case)

Simplest binary function: inversion



A	B
0	1
1	0

Circuit must take the “1” voltage range at the input and deliver the “0” voltage range at the output.

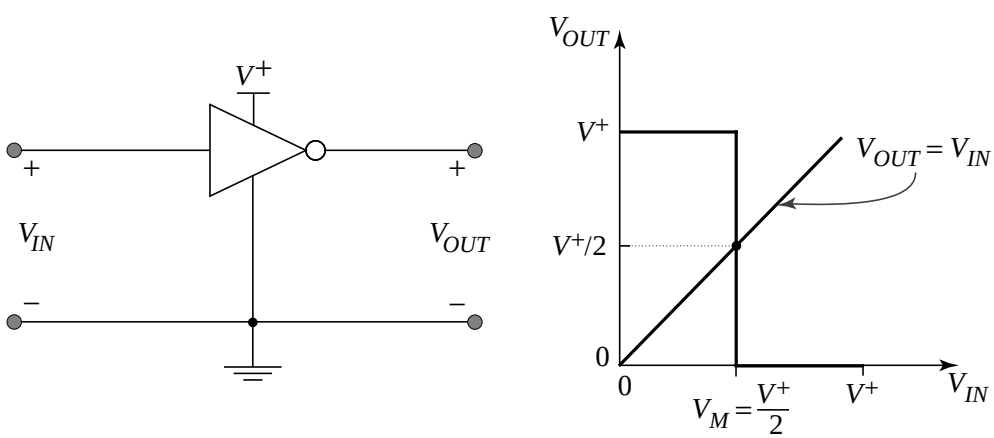
An Ideal Inverter

- Voltage transfer curve for an inverter -- it should yield 0 V when a high voltage is input and the high voltage, V^+, when a low voltage is input. An ideal inverter would be very forgiving of imperfect input voltages ...

$$V_{IN} > V_M = V^+ / 2 \text{ --> } V_{OUT} = 0 \text{ V}$$

$$V_{IN} < V_M = V^+ / 2 \text{ --> } V_{OUT} = V^+$$

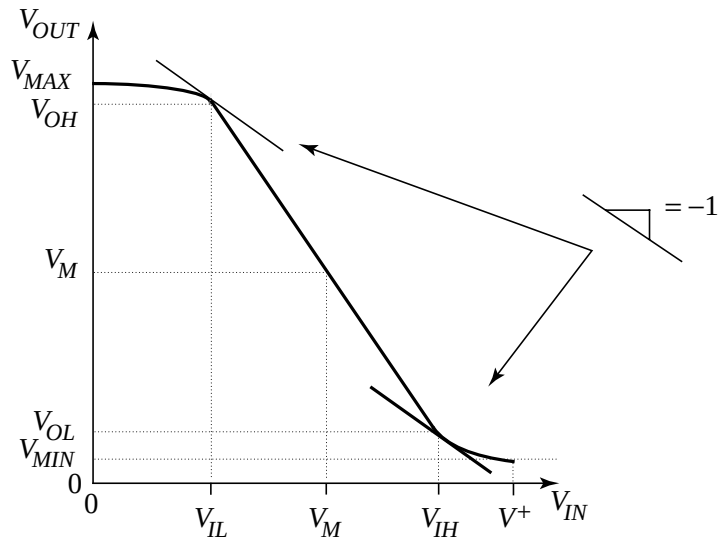
Note that the ideal inverter returns correct logical outputs (0 V or V^+) even when the input voltage is corrupted by noise, voltage spikes, etc. that are nearly half the supply voltage!



(a) (b)

Real Inverters

The inverters which we can build are approximations to the ideal inverter. A typical inverter characteristic is:



On the output and input axes, several voltages are defined:

V_M = voltage midpoint where $V_{OUT} = V_{IN} = V_M$.

V_{OL} = “voltage output low” = max. output voltage for a valid “0”

V_{OH} = “voltage output high” = min. output voltage for a valid “1”

V_{IL} = “voltage input low” = smaller input voltage where slope equals -1

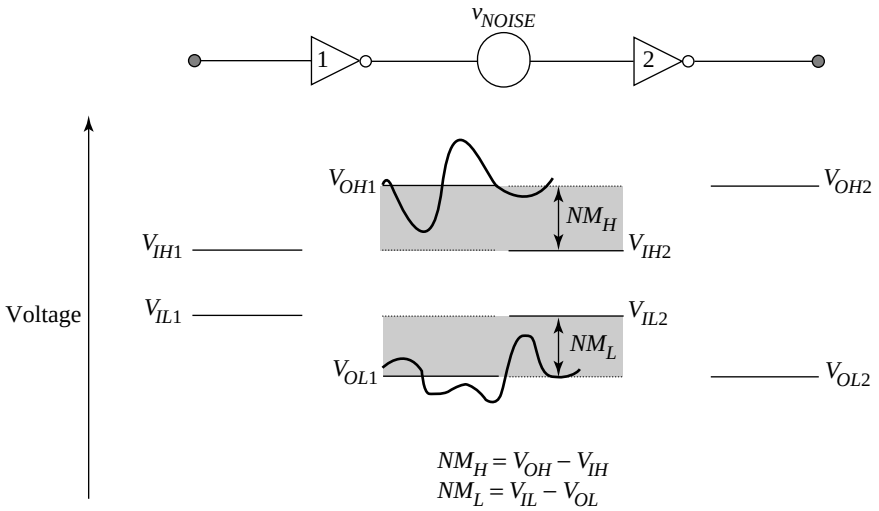
V_{IH} = “voltage input high” = larger input voltage where slope equals -1

$V_{MAX} = V_{OUT}$ for V_{IN} = 0 V; usually, $V_{MAX} = V^+$, the supply voltage

$V_{MIN} = V_{OUT}$ for $V_{IN} = V^+$ and is the minimum output voltage

Noise Margins

- Digital electronic circuits consist of series of logic gates; the voltage signals are contaminated by “noise” -- actually, mostly generated by capacitive coupling from other parts of the circuit



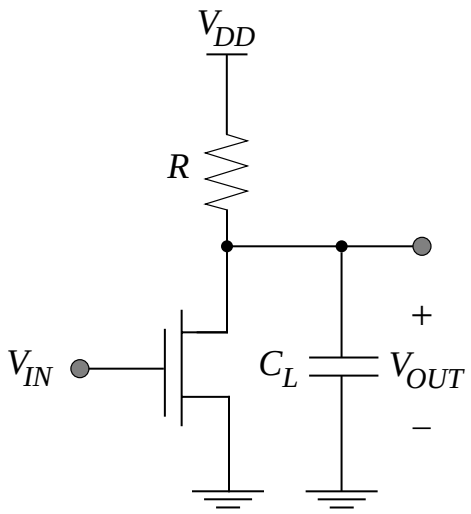
- Output of inverter #1 is at least V_{OH1} (assuming it had a valid low input $V_{IN1} < V_{IL1}$); therefore, there’s a margin of V_{OH1} - V_{IH2} to spare before the input to inverter #2 has an invalid high input.
- For the case of cascaded identical inverters, we define **noise margins**

$$NM_H = V_{OH} - V_{IH} = \text{noise margin (high)}$$

$$NM_L = V_{IL} - V_{OL} = \text{noise margin (low)}$$

Inverter Circuits: NMOS-Resistor Pull-Up

- First example: motivate the concept of a MOSFET switch enabling an approximation to the inverter.



V_{DD} = 5 V (typically)

C_L = load capacitance (from interconnections and from other inverters connected to the output

V_{BS} = 0 V -- bulk-to-source short-circuit is assumed to be present unless indicated otherwise

Finding the Voltage Transfer Curve

- *Approach 1*: start with $V_{IN} = 0$ and increase it; figure out the operating regions for the MOSFET and substitute $I_D = I_D\,(V_{GS}, V_{DS}) = I_D(V_{IN}, V_{OUT})$ and find

$$V_{OUT} = V_{DD} - I_D R$$

- *Approach 2*: use a graphical technique

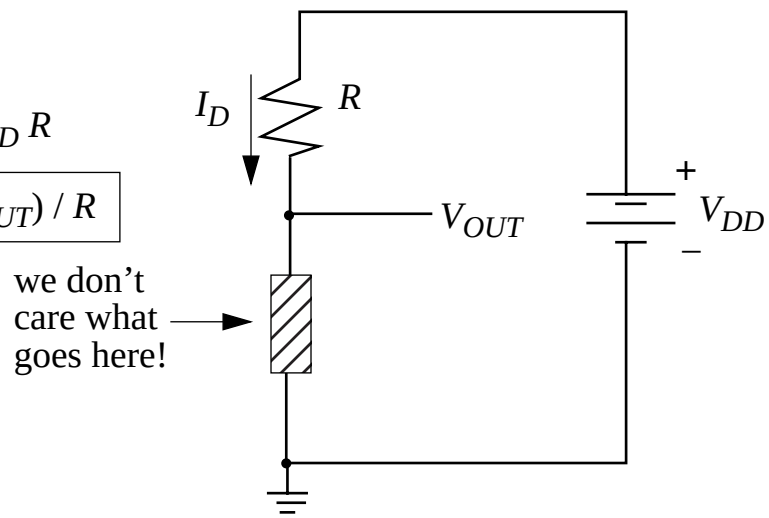
  >> we know $I_D(V_{IN}, V_{OUT})$ from the MOSFET's drain characteristics

  >> we can find *another equation* relating I_D and V_{OUT} from KVL --

$V_{OUT} = V_{DD} - I_D R$

$\boxed{I_D = (V_{DD} - V_{OUT}) / R}$

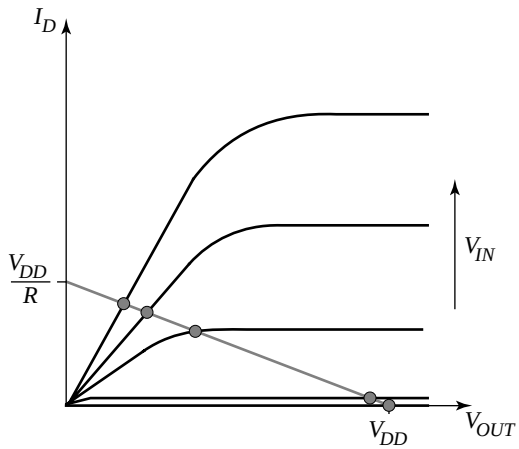
load line



- Intersections between the family of drain characteristics and the *load line* yield V_{OUT} as a function of V_{IN}

Voltage Transfer Curve using Load Line Technique

- Graphical intersection of I_D versus V_{OUT} characteristics with load line



* Given $\mu_n C_{ox}$ = 50 μA/V^2, (W/L) = 4.5/1.5 = 3, V_{Tn} = 1.0 V, and λ_n = 0

Improved Inverters

- *First try*: quantify how increasing the resistor R affects the slope of the voltage transfer curve at the midpoint (a measure of the steepness of the transition region)

$$\left.\frac{dv_{OUT}}{dv_{IN}}\right|_{V_M} = A_v$$

From our small-signal modelling concepts, this slope is equal to the ratio of the small-signal voltages v_{out} and v_{in}

$$\frac{v_{out}}{v_{in}} = A_v$$

How to find v_{out} / v_{in}? Use the small-signal model!

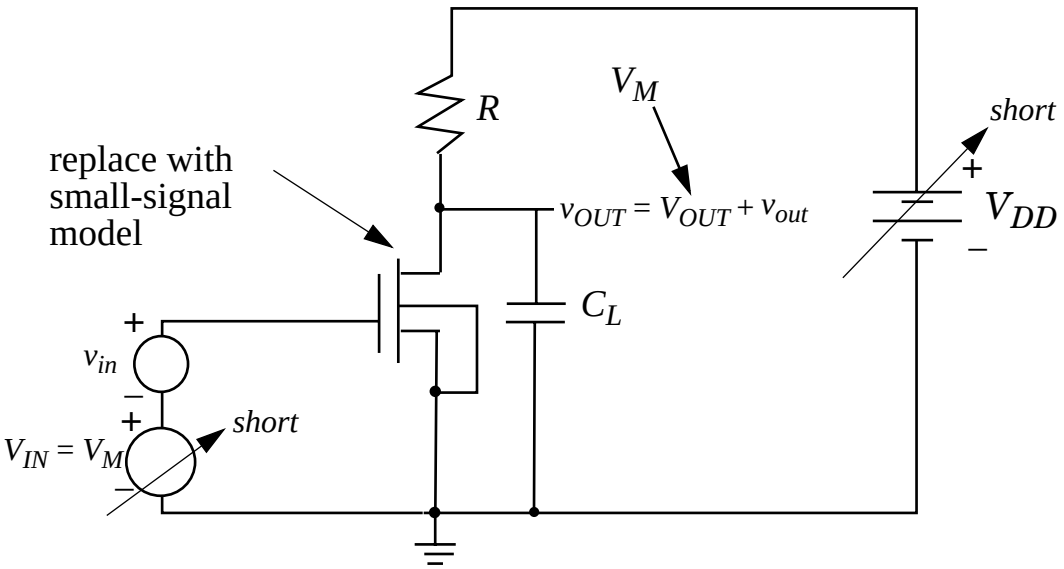
Small-signal model of the battery V_{DD} --> a short circuit!

Why? $v_{DD} = V_{DD} + v_{dd}$ ... by definition, an ideal battery has

$v_{DD} = V_{DD}$ which implies that $v_{dd} = 0$.

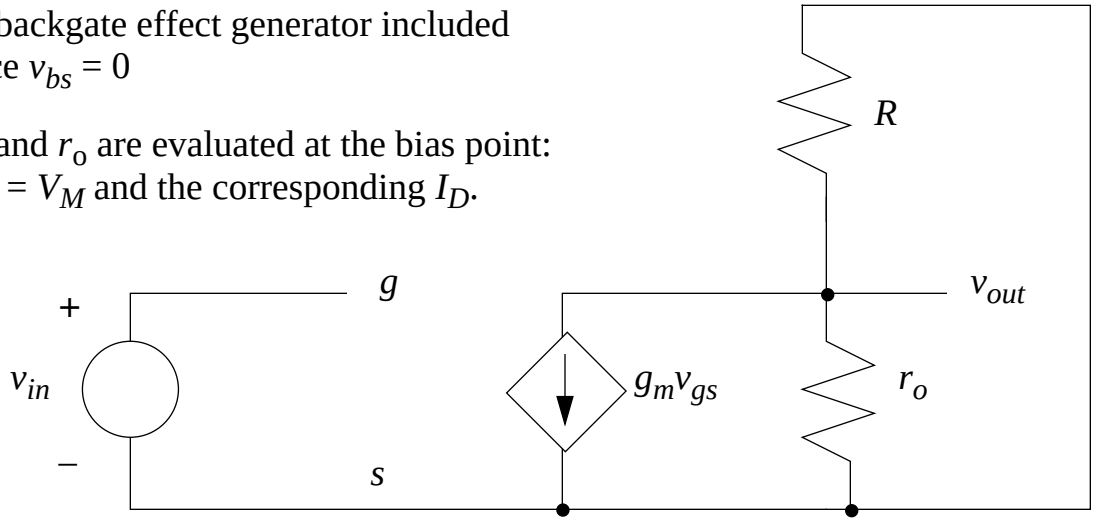
Small-Signal Model of Inverter

*Finding the small-signal circuit, neglecting capacitors:



* No backgate effect generator included since $v_{bs} = 0$

* g_m and r_o are evaluated at the bias point: $V_{GS} = V_M$ and the corresponding I_D.



Small-Signal Analysis

- Solving for the small-signal voltage gain -- the slope of the transfer curve at $V_{IN} = V_M$:

$$\frac{v_{out}}{v_{in}} = -g_m(R||r_o) \cong -g_m R = A_v$$

  where we have assumed that $R << r_o$, which is reasonable for small λ_n

- The transconductance is a function of the DC drain current, which is in turn a function of R through the load line equation:

$$g_m \cong \sqrt{2\mu_n C_{ox}(W/L)I_D} = \sqrt{2\mu_n C_{ox}(W/L)\left(\frac{V_{DD} - V_M}{R}\right)}$$

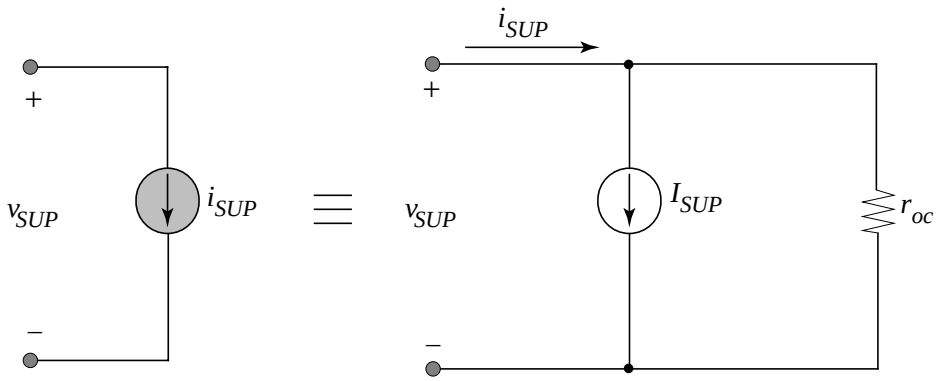
so that $A_v \propto \sqrt{R}$

- Why not increase R to say 500 kΩ? The answer lies in the dynamic response of the inverter. Tiny DC drain currents --> very *slow* transitions

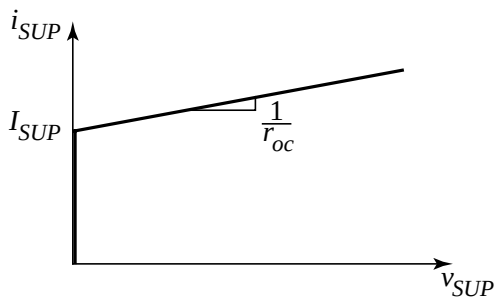
  Therefore, we want to have a large A_v with a large I_D ...

Current-Source Pull-Up

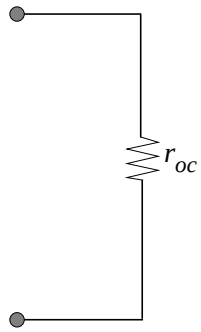
- What else could be connected between the drain and V_{DD}?



(a)



(b)



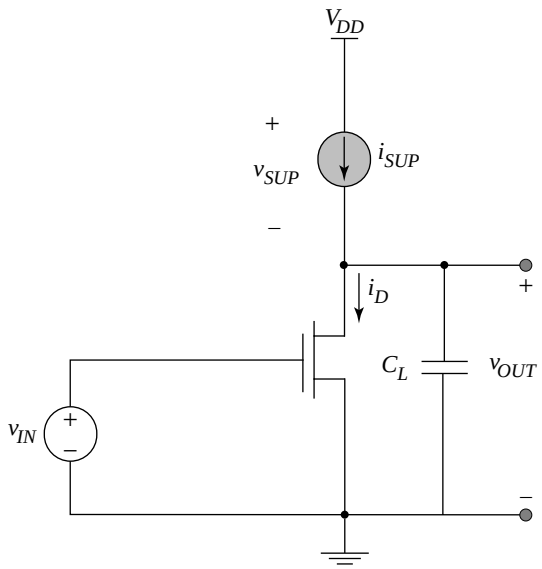
(c)

Resistor can be quite large --> can get high small-signal gain (and therefore, a narrow transition region)

DC Current is large --> fast transitions

MOS Inverter with Current-Source Pull-Up

- Replace resistor with current source



- Find the voltage transfer curve graphically by superimposing i_{SUP} vs. v_{OUT} (load line) on top of the drain characteristics

  we have a plot of i_{SUP} vs. v_{SUP} and we know that $v_{OUT} = V_{DD} - v_{SUP}$

  therefore, the current source i_{SUP} vs. v_{OUT} is a “mirrored” version of the plot of i_{SUP} vs. v_{SUP}

Load-Line Analysis of Improved Inverter

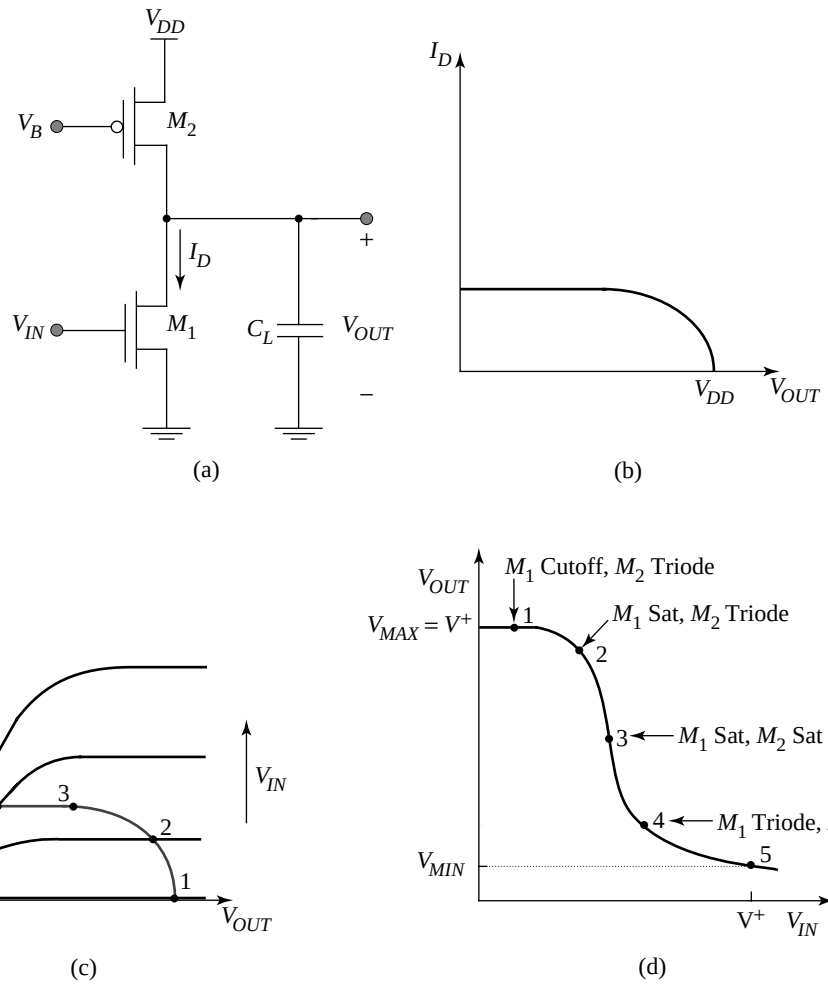
- Voltage transfer curve with idealized current-source pull-up is much closer to that of the ideal inverter

- Question: how to implement the current source using transistors?

p-channel MOSFET as a Current-Source Pull-Up

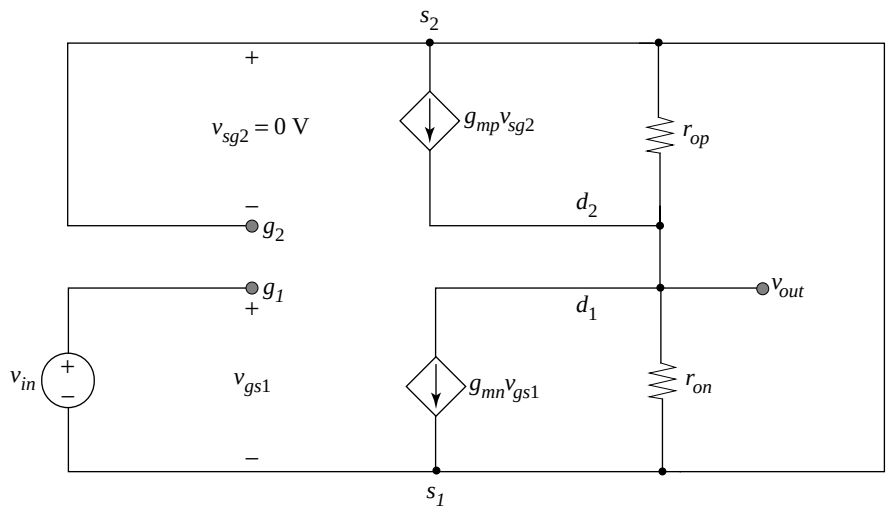
- Use p-channel MOSFET M_2 (with well connected to the source to make $V_{SB} = 0$ and source connected to the supply voltage)

  connect the gate to a battery V_B that results in an "appropriate" value of DC current $-I_{D2} = I_{D1}$.



Voltage Transfer Curve

- In order to find the slope at $V_{IN} = V_M$, we note that both transistors are saturated there (near point 3) and that the small-signal models from Chapter 4 are valid



- Slope of transfer curve at $V_{IN} = V_M$:

$$\left.\frac{dv_{OUT}}{dv_{IN}}\right|_{V_M} = \frac{v_{out}}{v_{in}} = -g_{mn}(r_{on}||r_{op})$$

The transition region can be *much* steeper than for the resistor load, while the large DC drain current at V_M results in short propagation delays ... what more could be desired?

- DC power is wasted when inverter is in $V_{OUT} = V_{MIN}$ state ... need a "switchable" current supply to disconnect V_{DD} when output is low