IC Fabrication Technology

- History:

  1958-59: J. Kilby, Texas Instruments and R. Noyce, Fairchild
  1959-70: Explosive growth in US (bipolar ICs)
  1970-85: MOS ICs introduced, RAMs, microprocessors, Japan catches up to US in volume
  1985-95: PC revolution, improved design software for complex CMOS integrated systems, US leads in micro-processors, Japan in RAMs
  1996-2000 > 10^8 devices/chip (= 1000 Mbit dRAM), US remains competitive -- even dominates -- sectors of the market; spin-offs from IC technology in MEMS (micro electro-mechanical systems) for sensing acceleration

- Key Idea: *batch fabrication* of electronic circuits

  An entire circuit, say 10^6 transistors and associated wiring -- can be made in and on top of a single silicon crystal by a series of process steps similar to printing.

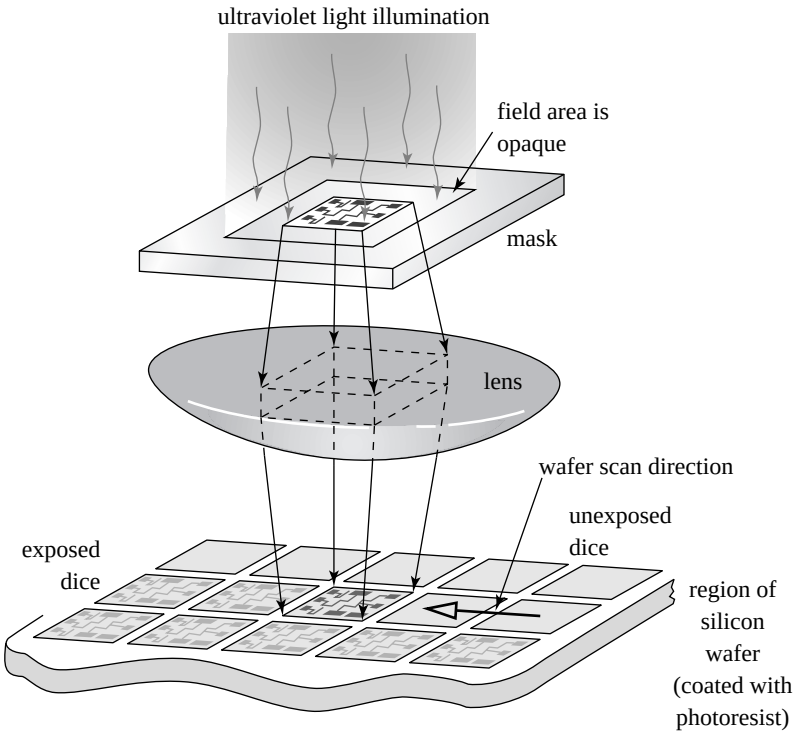
  The silicon crystal is a thin disk about the size of a small dinner plate (ca. 1996) called a *wafer*. More than 100 copies of the circuit are made at the same time.

- Results:

1. Complex systems can be fabricated reliably
2. Cost per function drops as the process improves (e.g., finer printing), since the cost per processed wafer remains about the same

Photolithography

- The essential process step: makes possible the transfer of a series of patterns onto the wafer -- all aligned to within 0.1 μm
- Process "Tool" -- *wafer stepper*



- UV-sensitive film is called *photoresist.* Regions exposed to UV dissolve in developer (for *positive* photoresist -- the type we will consider)

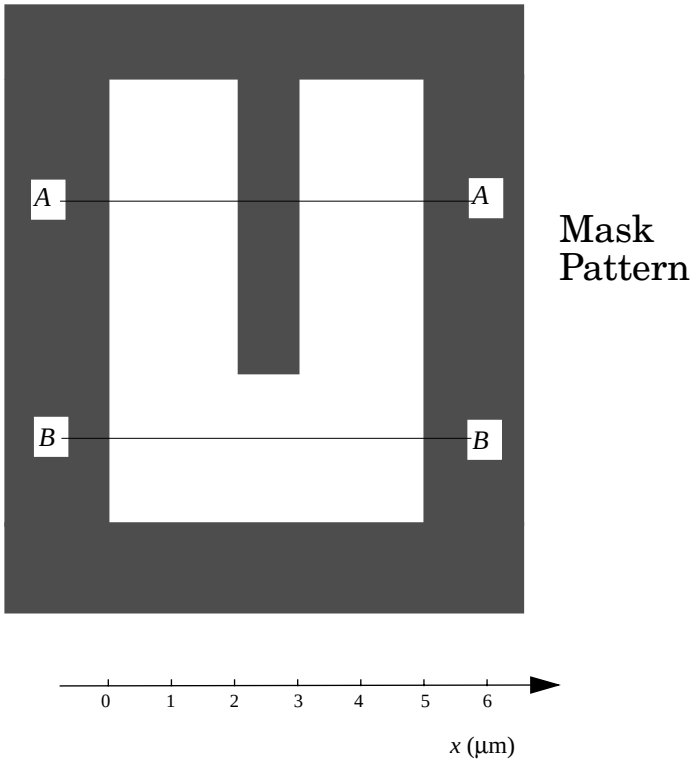
Exposure, Development, and Pattern Transfer

- Simple example of a *layout* and a *process* (or *recipe*)

  * *Layout* is the set of mask patterns for particular layers (one in this case)

  * *Process* is the sequence of fabrication steps

- Visualize by generating *cross sections* through the structure as it is built up through the process



Process Flow in Cross Sections

- Process (simplified)

  0. Clean wafer in nasty acids (HF, HNO_3, H_2SO_4, ...) --> wear gloves!

  1. Grow 500 nm of SiO_2 (by putting the wafer in a furnace with O_2

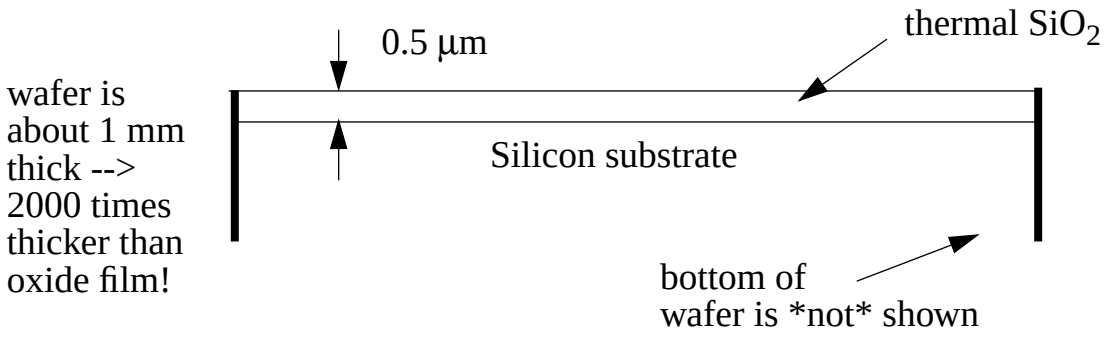
  2. Coat the wafer with 1 μm of photoresist

  3. Expose and develop the image and bake the resist to get rid solvent and to make it tougher

  4. Put wafer in a plasma etcher -- fluorine ions in plasma etch SiO_2 much faster than underlying silicon -- and etch off exposed SiO_2

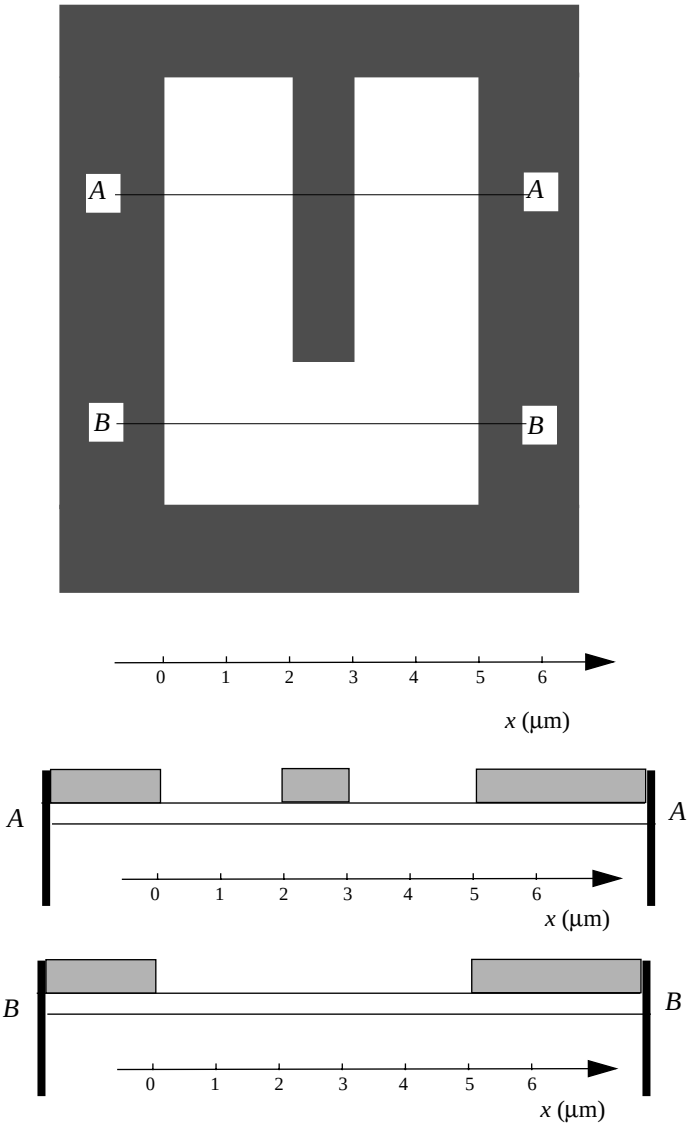
  5. Put wafer in a plasma stripper -- oxygen ions remove photoresist and leave SiO_2 untouched.

- After Step 1 (SiO_2 growth):



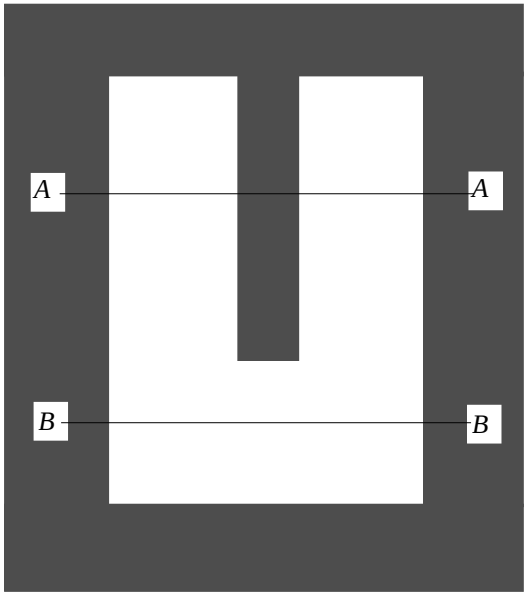
Process Flow (cont.)

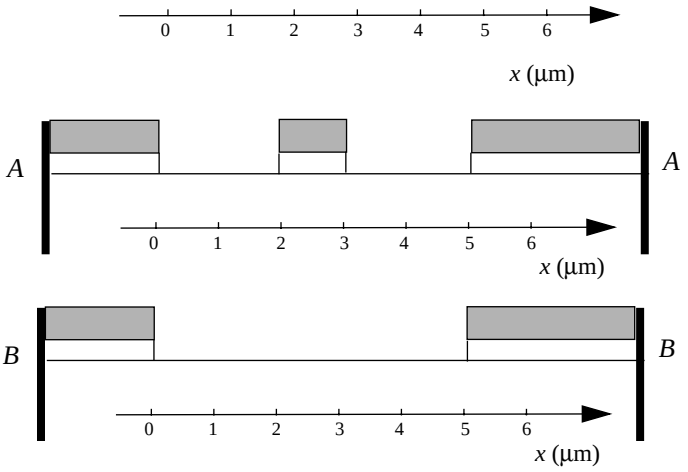
- After Step 3: photoresist has been developed from clear areas of the mask



Process Flow (cont.)

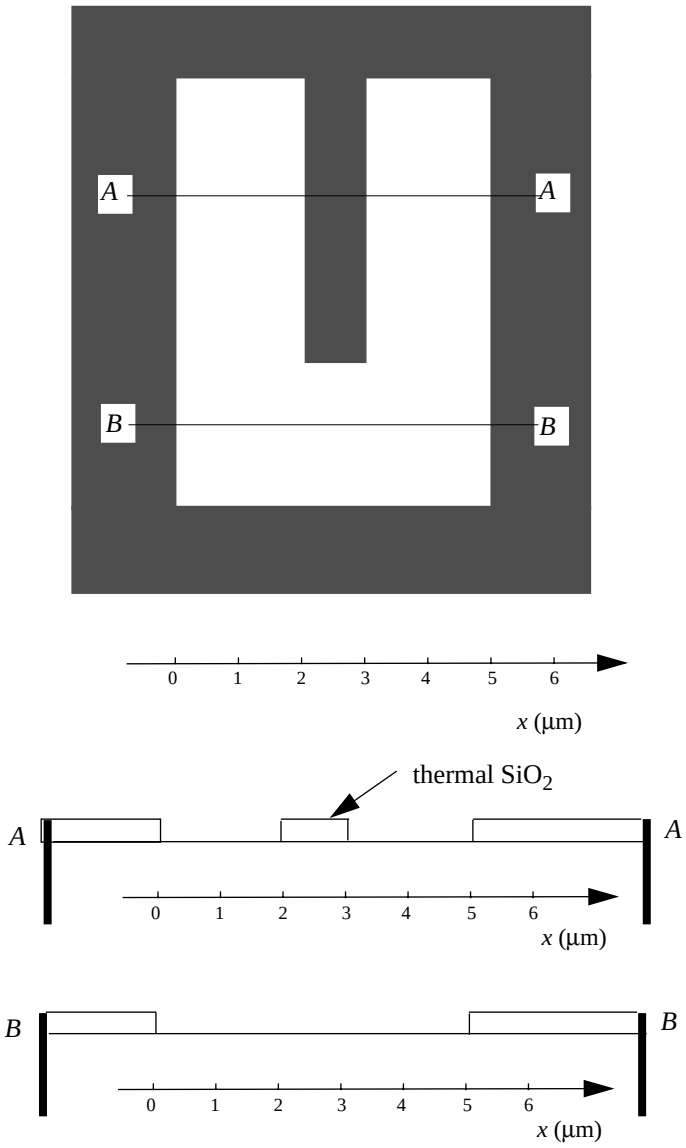
- After Step 4: oxide is etched in the fluorine plasma, without etching of the underlying silicon





Completed Structure

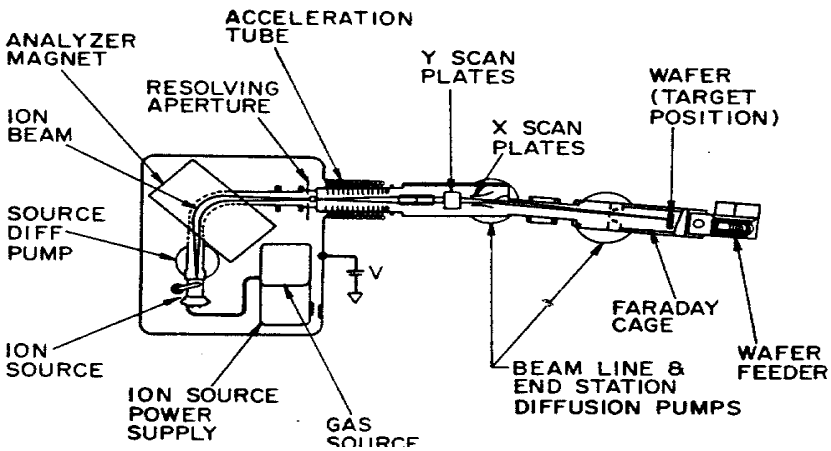
- After Step 5: oxygen plasma strips (i.e., etches) the photoresist



IC Fabrication Processes

- Ion Implantation

  ions are accelerated to energies of 20 keV - 3 MeV and bombard the silicon wafer in a collimated beam



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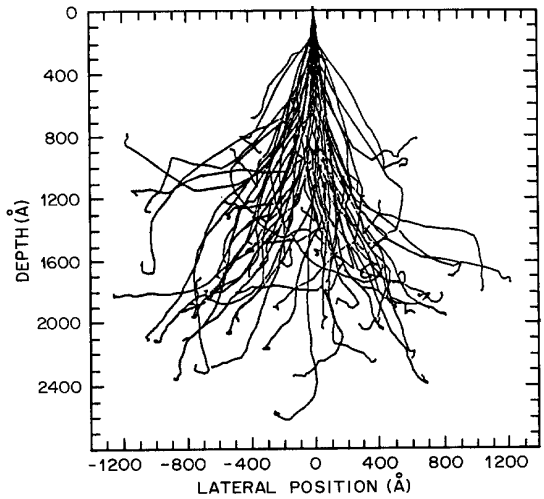
ion tracks in the silicon crystal (simulation)



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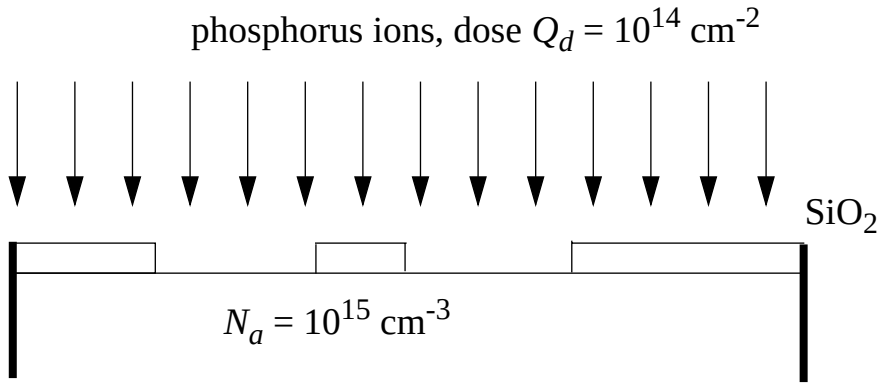
damage from implantation can be *annealed* by heating the wafer in a furnace to $T > 900\ ^{o}C$.

Doping by Ion Implantation

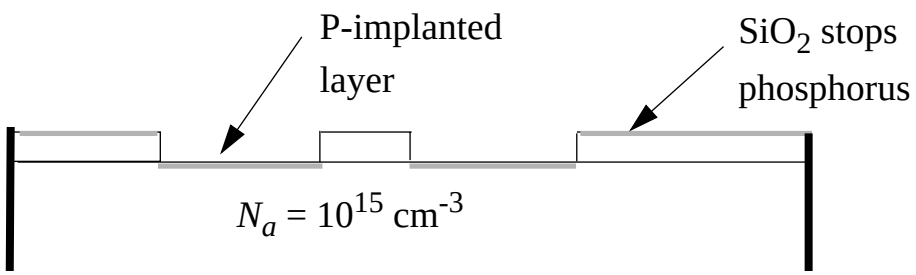
- *Dose* = ion beam flux (# cm^{-2} s^{-1}) x time for implant ... units # cm^{-2}

  Example:



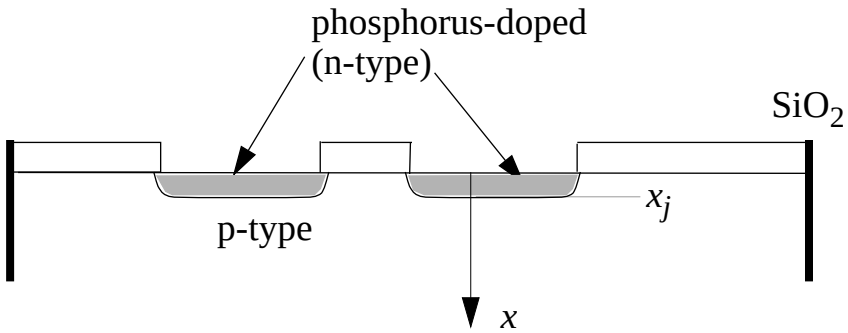
  SiO_2 film masks the implant by preventing ions from reaching the underlying silicon (assuming it's thick enough)

  > after implantation, the phosphorus ions are confined to a damaged region near the silicon surface :



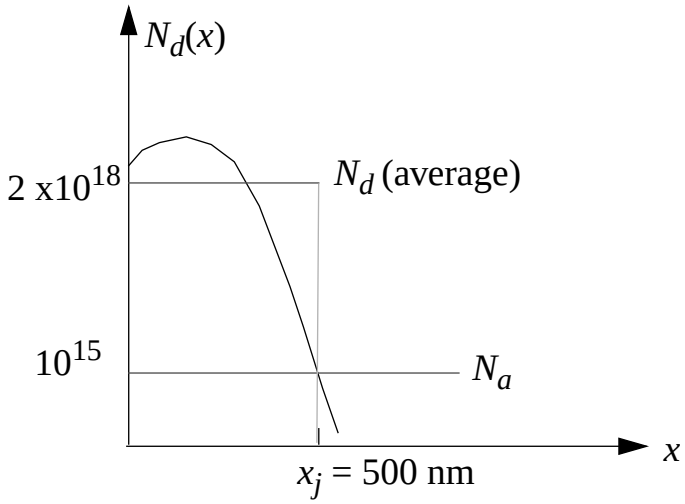
Doping by Ion Implantation (cont.)

- Annealing heals damage and also redistributes the ions (they diffuse further into the silicon crystal)



x_j is the *junction depth* and is the point where $N_d = N_a$

- Details of $N_d(x)$ ... later in an advanced course. We will use the average concentration in the n-type region for a given junction depth here.



- Average donor concentration in n-type layer = $N_d = Q_d / x_j$

IC Materials and Processes

- *Polycrystalline silicon (polysilicon)*: silicon deposited from a gas at temperatures around 600 ^{o}C, made up of small crystallites (grains), so-so conductor when heavily doped with phosphorus, but can survive very high temperatures. Useful for making micromechanical structures

- *Deposited oxides*: silicon dioxide deposited from a gas at temperatures from 425 ^{o}C to 600 ^{o}C, boron and phosphorus are sometimes added to allow it to flow. These oxides are known as "CVD" oxides for "chemical vapor deposition."

- *Metals*: aluminum is the standard "wire" for ICs and is usually deposited by "sputtering." Tungsten (grown from a gas reaction) is sometimes used, with increasing interest in copper.

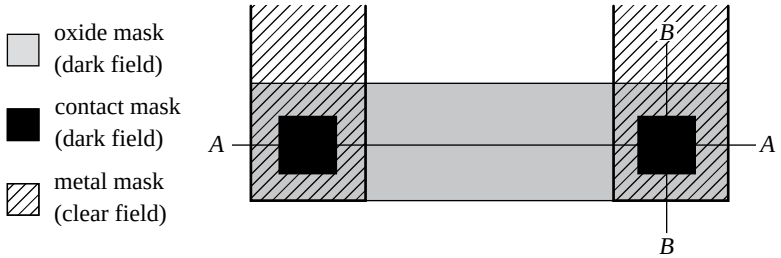
In order to make an IC, we need

1. the mask patterns (the *layout*)

2. the sequence of fabrication steps (the *process* ... or *recipe*)

Process Flow Examples

- Three-mask layout:



(a)

- Process (highly simplified):

1. Grow 500 nm of thermal oxide and pattern using oxide mask

2. Implant phosphorus and anneal

3. Deposit 600 nm of CVD oxide and **pattern using contact mask**

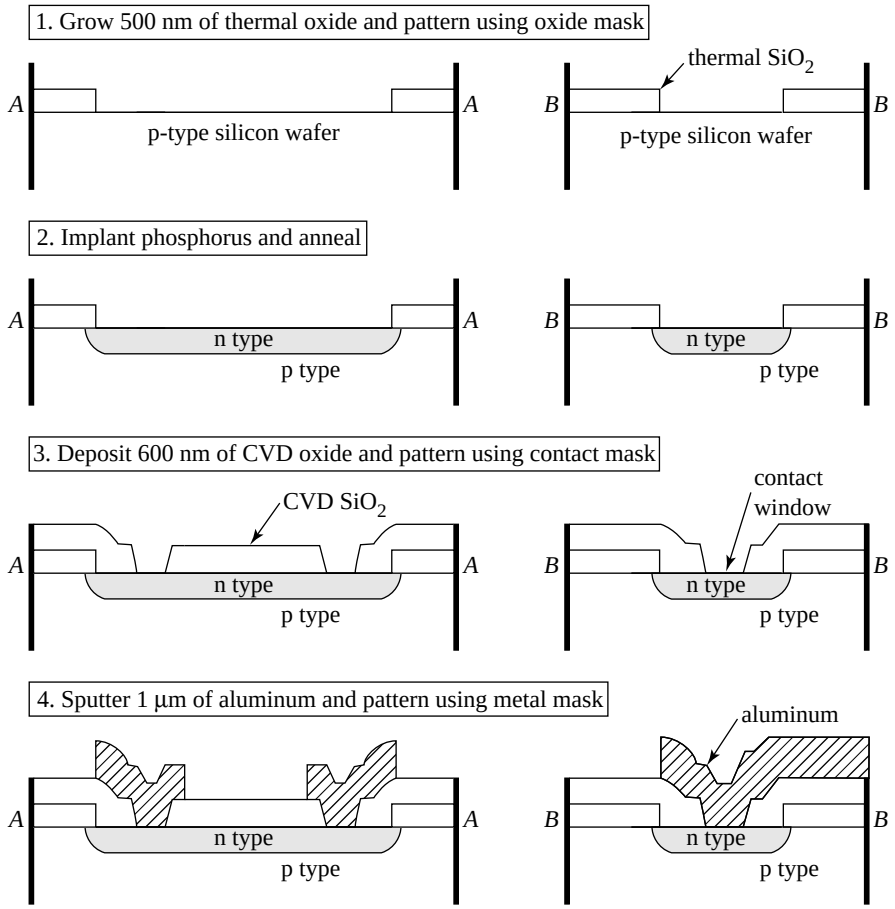
4. Sputter 1 μm of aluminum and pattern using metal mask

** note that **pattern using xxx mask** involves photolithography (including alignment to earlier patterns on the wafer), as well as etching using a plasma or "wet" chemicals, and finally, stripping photoresist and cleaning the wafer.

- 1996 IC fab: nearly 30 masking steps for some dRAM processes!

Cross Sections

- Shown on layout; only draw top few μm of the silicon wafer
- Technique: keep track of dark/light field label for each mask and be careful to be consistent on what is added or etched in each step

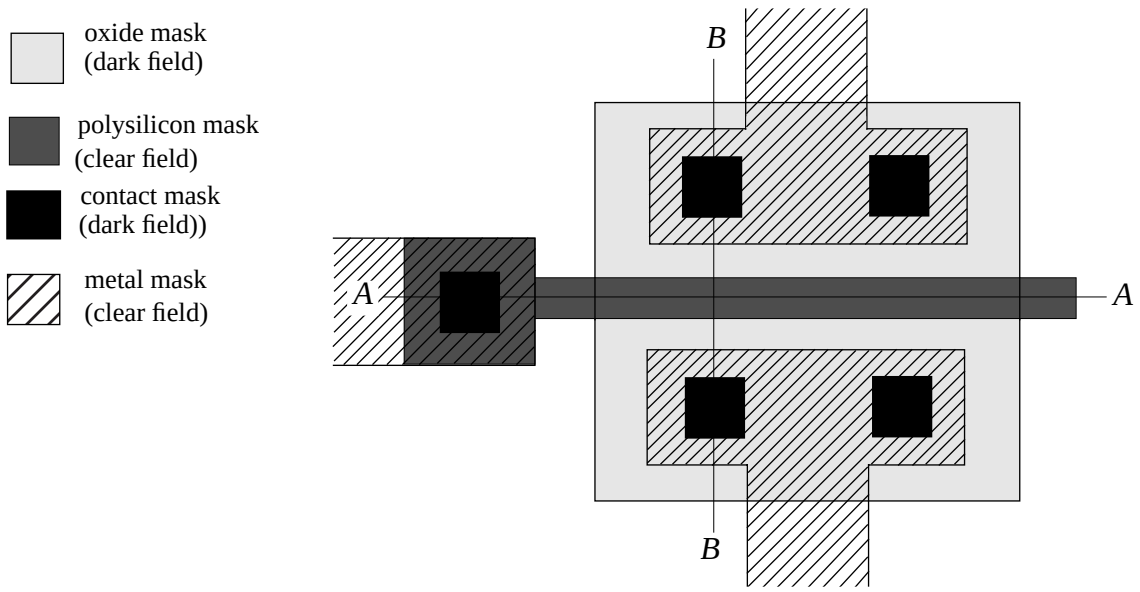


(b)

MOSFET Fabrication

- This device, the subject of Chapter 4, has made possible the revolution in digital electronics. It can be made in only 4 masking steps (one of its advantages)

- Layout



Process Flow (Simplified)

1. Grow 500 nm of thermal SiO_2 and pattern using oxide mask

2. Grow 15 nm of thermal SiO_2

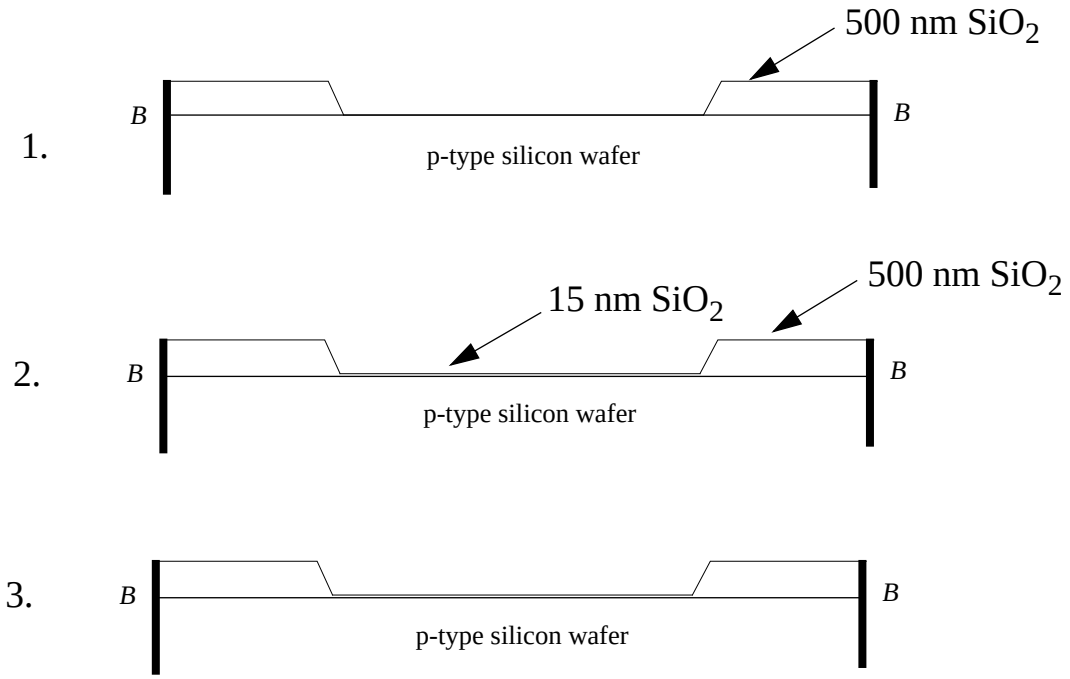
3. Deposit 500 nm of CVD polysilicon and pattern using polysilicon mask

4. Implant arsenic and anneal

5. Deposit 600 nm of CVD SiO_2 and pattern using contact mask

6. Sputter 1 μm of aluminum and pattern using metal mask.

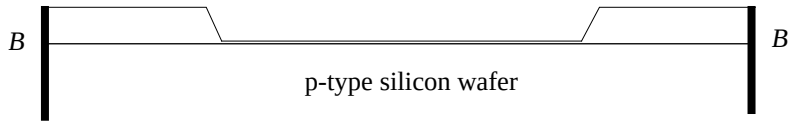
- Cross sections along *B-B*



MOSFET Cross Sections

- Arsenic implant/anneal, CVD oxide, and metallization steps: (incomplete)

4.



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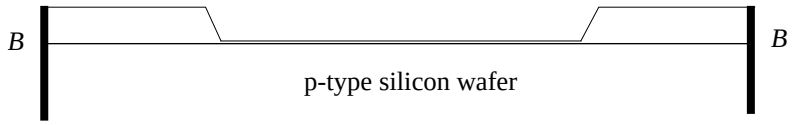

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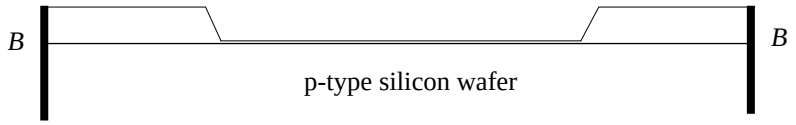


Ohm's Law for Silicon

Bulk silicon: uniform doping concentration, away from surfaces

n-type example: in equilibrium, $n_o = N_d$ and $\rho = 0$.

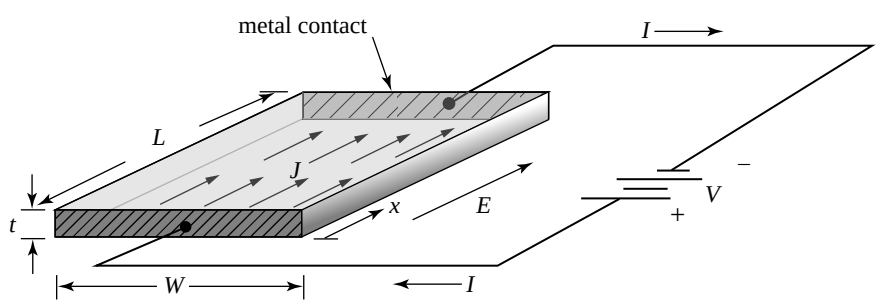
When we apply an electric field, $n = N_d$ and $\rho = 0$ ... n

Currents in n-type bulk silicon with an applied electric field E:

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx} \cong q\mu_n N_d E = \sigma_n E$$

where σ_n is the *conductivity* [Units: S/cm = 1 / (Ω cm)]

note: holes contribute almost nothing to the conductivity of n-type silicon.



Doped Silicon Resistors

***** Find the current density in the resistor:

$$J_n = \sigma_n E = \sigma_n \frac{V_A}{L}$$

assumption: field is less than $E_{sat} = 10^4$ V/cm, so no velocity saturation

* Current is current density times cross sectional area:

$$I = \sigma_n \left(\frac{V_A}{L}\right) A = \left(\frac{\sigma_n A}{L}\right) V_A$$

$$R = \frac{V_A}{I} = \left(\frac{1}{\sigma_n}\right)\frac{L}{A} = \rho_n \frac{L}{A}$$

where ρ_n is the resistivity [units: Ω cm]

* *Silicon resistivities*:

500 Ω cm to 5 mΩ cm for doping concentrations from 10^{13} to 10^{19}cm^{-3}

Sheet Resistance

- Rewrite the resistance equation to separate (L / W), the length-to-width ratio ... which is the number of "squares" $N_{\square}$ from $R_{\square}$, the sheet resistance = $(\sigma_n t)^{-1}$

$$R = \frac{L}{q\mu_n N_d W t} = \left(\frac{1}{q\mu_n N_d t}\right)\frac{L}{W} = R_{\square}\,(L/W) = R_{\square}\,N_{\square}$$

The sheet resistance is under the control of the *process designer*; the number of squares is determined by the layout and is specified by the *IC designer*.

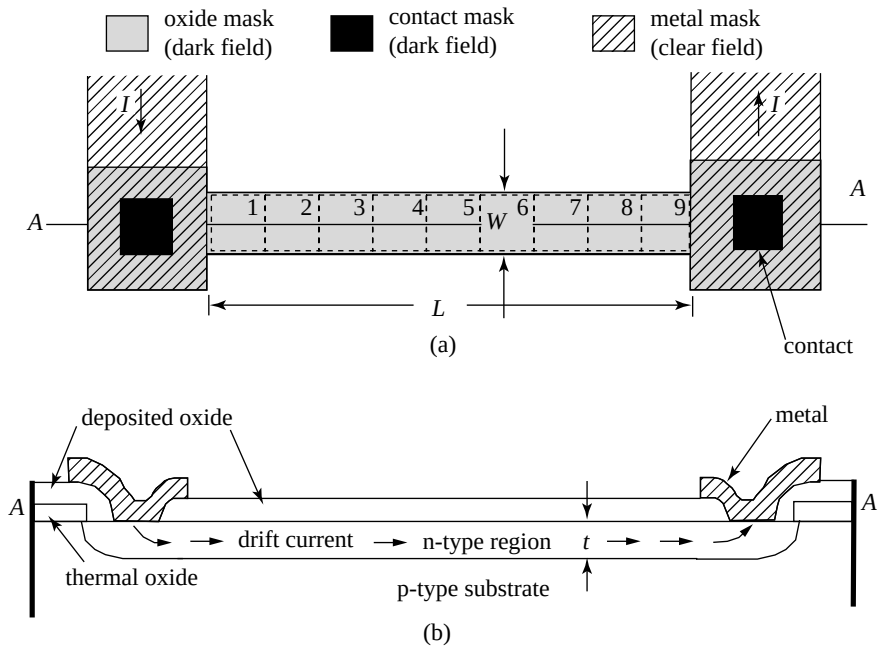
For average doping levels of 10^{15} cm^{-3} to 10^{19} cm^{-3} and a typical layer thickness of 0.5 μm, the sheet resistance ranges from 100 kΩ/❒ to 10 Ω/❒.

Other conducting materials: (MOSIS 1 μm CMOS process

	Ω / ❒
n^+ polysilicon (t =500 nm)	20
aluminum (t = 1 μm)	0.07
silicided polysilicon	5
silicided source/drain diffusion	3

Integrated Circuit Resistors

- Fabricate an n-type resistor in a p-type substrate using the process described in Chapter 2.



- Given the sheet resistance, we need to find the number of squares for this layout

  L / W = 9 squares

Uncertainties in IC Fabrication

The precision of transistors and passive components fabricated using IC technology is surprisingly, *poor*!

Sources of variations:

- ion impant dose varies from point to point over the wafer and from wafer to wafer
- thicknesses of layers after annealing vary due to temperature variations across the wafer
- widths of regions vary systematically due to imperfect wafer flatness (leading to focus problems) and randomly due to raggedness in the photoresist edges after development
- etc., etc.