

Análisis y diseño de circuitos Digitales
Práctico N° 1

A) Teniendo en cuenta los parámetros de MOSIS para AMI 1.5
(<http://www.mosis.com/Technical/Testdata/ami-abn-prm.html>)

A.1) Calcular la resistencia serie de una línea de 100um de largo, y ancho mínimo del proceso, hecha en los siguientes niveles:

1. difusión N
2. difusión P
3. poly
4. poly2
5. M1
6. M2
7. M3

A.2) Calcular la capacidad de dos líneas de M1-M2 (de ancho mínimo) de 100um de largo que corren una arriba de otra. Calcular la capacidad de dos líneas similares de M1 que corren en paralelo.

B) Repetir si el proceso es AMI 0.5
(<http://www.mosis.com/Technical/Testdata/ami-c5-prm.html>)

C) Responder:

¿Que sucede con cada una de ellas cuando se muda de un proceso a otro de tecnología más pequeña?

MOSIS file ami-c5/t61f-params.txt

MOSIS WAFER ACCEPTANCE TESTS

RUN: T61F
 TECHNOLOGY: SCN05
 microns

VENDOR: AMIS
 FEATURE SIZE: 0.5

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM Vth	3.0/0.6	0.78	-0.95	volts
SHORT Idss	20.0/0.6	457	-240	uA/um
Vth		0.67	-0.92	volts
Vpt		10.0	-10.0	volts
WIDE Ids0	20.0/0.6	< 2.5	< 2.5	pA/um
LARGE Vth	50/50	0.69	-0.97	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		57.2	-18.9	uA/V^2
Low-field Mobility		460.51	152.16	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

(um)	Design Technology	XL (um)	XW
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0.00	SCMOS_SUBM (lambda=0.30)	0.10	
0.20	SCMOS (lambda=0.35)	0.00	

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FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2
UNITS							
Sheet Resistance	82.8	106.9	23.0	1041	43.0	0.09	0.09
ohms/sq							
Contact Resistance	62.1	156.6	16.4		27.9		0.81
ohms							
Gate Oxide Thickness	139						
angstrom							

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	843	837	ohms/sq
Contact Resistance	0.87			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W
UNITS								
Area (substrate)	429	734	86		32	17	11	39
aF/um ²								
Area (N+active)			2478		37	17	12	
aF/um ²								
Area (P+active)			2397					
aF/um ²								
Area (poly)				928	58	17	10	
aF/um ²								
Area (poly2)					52			
aF/um ²								
Area (metall1)						37	14	
aF/um ²								
Area (metal2)							35	
aF/um ²								
Fringe (substrate)	312	238			70	52	38	
aF/um								
Fringe (poly)					63	40	29	
aF/um								
Fringe (metall1)						55	35	
aF/um								
Fringe (metal2)							53	
aF/um								
Overlap (N+active)			207					
aF/um								
Overlap (P+active)			230					
aF/um								

CIRCUIT PARAMETERS		UNITS	
Inverters	K		
Vinv	1.0	2.00	volts
Vinv	1.5	2.26	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.44	volts
Gain	2.0	-20.02	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		91.42	MHz
D256_WIDE (31-stg,5.0V)		147.99	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.47	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		0.98	uW/MHz/gate

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS			
MINIMUM Vth	4.8/3.2	0.86	-1.15	volts			
SHORT Vth	9.6/3.2	0.84	-1.11	volts			
LARGE Vth	28.8/28.	0.86	-1.10	volts			
K' (Uo*Cox/2)		20.9	-6.5	uA/V^2			
FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS			
Vth	Poly	>15.0	<-15.0	volts			
BIPOLAR PARAMETERS	W/L	NPN		UNITS			
2X1 Beta	2X1	133					
V_early		40.2		volts			
Vce,sat		---		volts			
2X2 Beta	2X2	133					
V_early		39.9		volts			
Vce,sat		---		volts			
2X4 Beta	2X4	134					
V_early		39.6		volts			
Vce,sat		---		volts			
2X8 Beta	2X8	134					
V_early		39.2		volts			
Vce,sat		---		volts			
BVceo		7.2		volts			
BVcbo		7.2		volts			
BVebo		6.8		volts			
PROCESS PARAMETERS	N+	P+	POLY	POLY2	PBASE	M1	M2
UNITS							
Sheet Resistance	54.5	78.3	26.1	22.6	2323.9	0.05	0.03
ohms/sq							
Contact Resistance	57.1	41.8	25.0	15.8			0.05
ohms							
Gate Oxide Thickness	310						
angstrom							

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PROCESS PARAMETERS	N_W	UNITS					
Sheet Resistance	1676	ohms/sq					
Contact Resistance		ohms					
CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	N_W
UNITS							
Area (substrate)	282	302	38	38	24	14	126
aF/um ²							
Area (N+active)			1115	714	52	26	
aF/um ²							
Area (P+active)			1097	706			
aF/um ²							
Area (poly)				577	46	22	
aF/um ²							
Area (poly2)					47	23	
aF/um ²							
Area (metall)						37	
aF/um ²							
Fringe (substrate)	101	176			31	--	
aF/um							
Fringe (poly)					59	44	
aF/um							
Fringe (metall)						54	
aF/um							
Overlap (N+active)			173				
aF/um							
Overlap (P+active)			196				
aF/um							
CIRCUIT PARAMETERS			UNITS				
Inverters	K						
Vinv	1.0		1.76	volts			
Vinv	1.5		2.08	volts			
Vol (100 uA)	2.0		0.40	volts			
Voh (100 uA)	2.0		4.37	volts			
Vinv	2.0		2.29	volts			
Gain	2.0		-13.25				
Ring Oscillator Freq.							
DIV64 (31-stg,5.0V)			42.86	MHz			
Ring Oscillator Power							
DIV64 (31-stg,5.0V)			1.54	uW/MHz/gate			